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A Strategy for Developing an Effective Cache Catalogue in the Communication Domain

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Abstract:

This research paper presents a method and device for resolving the challenges faced in the prior art, specifically related to low access speed of the cache catalogue and low storage use efficiency. The proposed method involves the construction of a cache catalogue, comprising a public data catalogue and a private data catalogue. The public data catalogue records data block information of public data, while the private data catalogue records data block information of private data. Additionally, the method includes determining the data type of the target data associated with a read-write request transmitted by a first processor. This data type can be classified as private data or public data. The target data's data block information is then recorded in the cache catalogue. The method and device presented in this research are suitable for the communication field and aim to enhance the recording of data block information in a multi-processor system.

Keywords: Cache catalogue, communication, access speed, storage efficiency, data block information, multi-processor system.

Introduction:

In the field of communication, the efficient management of data access and storage is of paramount importance for ensuring optimal system performance. One critical aspect of this management is the cache catalogue, which plays a crucial role in recording and retrieving data block information. However, the existing approaches suffer from limitations such as low access speed and low storage use efficiency, which hinder the overall system's effectiveness. To overcome these challenges, this research presents a novel method and device for achieving an efficient cache catalogue in the communication field. The proposed method involves the construction of a cache catalogue that comprises a public data catalogue and a private data catalogue. By leveraging this approach, the system can improve access speed and storage use efficiency, leading to enhanced performance.

Background:

Cache catalogues are widely used in multi-processor systems to facilitate efficient data management. They store data block information that aids in quick data retrieval and enhances system performance. However, traditional cache catalogues face significant limitations, particularly in the context of communication systems. The low access speed of cache catalogues can result in delays and bottlenecks in data retrieval processes, leading to decreased overall system efficiency. Additionally, the low storage use efficiency of cache catalogues can result in suboptimal utilization of available resources. Therefore, there is a need for an innovative method and device to address these limitations and enhance the cache catalogue's performance in the communication field.

Processors (CPUs) are essential components in both terminal devices and server apparatus. With continuous improvements in the performance of terminal devices and server equipment, multi-core processor systems have become increasingly prevalent. These systems include a plurality of processor modules and can be categorized into different types, such as UMA (Uniform Memory Access) and NUMA (Non-Uniform Memory Access) systems. In a multi-core processor system, the speed at which a CPU can access and retrieve target data varies depending on whether it is a read or write operation. Consequently, CPUs preferentially search for and retrieve target data from their local caches. If the target data is not stored in the local cache of a CPU, it will search and obtain the data from the cache of another CPU. If the target data is not present in any of the local caches, it will be searched and retrieved from the main internal memory.[1,2]

To achieve consistency between the data in the cache and the internal memory, a buffer consistency process needs to be

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carried out in the multi-CPU system, ensuring that the stored data in the processor system remains synchronized. One common approach to address this is by utilizing a cache directory, which records the position and state of both the cached data and the shared data in the multi-CPU system, acting as a catalog. A widely used cache directory is the inclusive directory, which stores data messages for all address spaces (including the internal memory and cache) in the processor system, encompassing the management of all shared data present in the device caches.[4,5,6]

However, in the prior art, several problems have been identified with this implementation method. One major issue is the large size of the address space in the processor system and the increasing number of processors, leading to a significant storage requirement for the inclusive cache directory. Consequently, the access speed of the cache directory is slow, and the utilization rate of storage is relatively low. These limitations hamper the overall performance and efficiency of the cache directory.[7,8]

In light of these challenges, there is a need for an improved method that addresses the issues of slow access speed and low storage utilization in the cache directory. Such a method would enhance the performance and efficiency of the cache catalogue, thereby improving the overall functioning of multi-processor systems in the communication field. By optimizing the recording and retrieval of data block information, the proposed method aims to overcome the limitations of the prior art and contribute to the advancement of cache catalogue management in communication systems.[10]

Research Objective:

The primary objective of this research is to propose a method and device that overcomes the challenges associated with low access speed and low storage use efficiency in cache catalogues. By introducing a cache catalogue consisting of a public data catalogue and a private data catalogue, and by effectively recording data block information of target data, we aim to enhance the overall performance of the cache catalogue in a multi-processor system. Through this research, we strive to contribute to the advancement of communication systems by providing a more efficient and effective approach to cache catalogue management.

Research:

The research aims to provide an implementation method and device for CACHE DIRECTORY that address the issues of slow access speed and low storage utilization rate in the prior art. The proposed method and device aim to optimize the performance and efficiency of CACHE DIRECTORY, specifically in multi-core processor systems, to enhance the overall functioning of communication systems.

The research comprises the following steps:

Creation of CACHE DIRECTORY: The first step involves creating the CACHE DIRECTORY, which includes two components: a publicly-owned data directory and a private data catalogue. The publicly-owned data directory is responsible for recording the data block information of publicly-owned data, while the private data catalogue records the data block information of private data.

Determination of data type: When receiving read-write requests from the first processor, the data type of the corresponding target data is determined. The data type can be classified as private data or publicly-owned data.

Recording data block information: Based on the determined data type, the data block information (Table-1 Block Information) of the target data is recorded in the CACHE DIRECTORY. This step ensures that the CACHE DIRECTORY accurately reflects the location and status of the data blocks.

Physical Address	Process ID	Significant bit
Block Address	n	0/1

Table-1 Block Information

In a possible implementation, the research includes additional steps:

Reception of read-write requests: The research involves receiving read-write requests sent by the first processor. These requests include the physical address of the target data.

Determination of data type based on physical address: The research determines the data type of the target data corresponding to the read-write requests. This determination is made by examining whether the physical address of the target data is recorded in the CACHE DIRECTORY.

In one scenario:

Determination of private data type: If the physical address of the target data is not recorded in the CACHE DIRECTORY, it is determined that the data type of the target data is private data.

Recording data block information for private data: According to the determined data type, the data block information of the target data is recorded in the private data catalogue. This includes recording the physical address of the target data and

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the processor flag, which indicates the read-write operations performed on the target data by the first processor.

In another scenario:

Determination of publicly-owned data type: If the physical address of the target data is recorded in the CACHE DIRECTORY, the research further examines the corresponding processor flag in the private data catalogue. If the processor flag matches that of the first processor, it is determined that the data type of the target data is private data. Otherwise, it is determined to be publicly-owned data.

Recording data block information for publicly-owned data: According to the determined data type, the data block information of the target data is recorded in the CACHE DIRECTORY. If the data type is determined to be private data, the data block information in the private data catalogue is updated based on the read-write requests, including the read-write count and access time. If the data type is determined to be publicly-owned data, the data block information is recorded in the publicly-owned data directory, and the directory entry in the private data catalogue is marked as invalid.

The research also includes the implementation of a device for CACHE DIRECTORY:

Device setup: The device is designed to set up the CACHE DIRECTORY, which includes the publicly-owned data directory and private data catalogue, similar to the method described earlier.

Determination unit: The device includes a determination unit responsible for determining the data type of the target data based on the read-write requests received from the first processor. This unit utilizes a detection module to determine whether the physical address of the target data is recorded in the CACHE DIRECTORY.

In one scenario: Determination of private data type: When the detection module confirms that the physical address of the target data is not recorded in the CACHE DIRECTORY, the determination unit concludes that the data type is private data.

Record cell: The record cell within the device is responsible for recording the data block information of the target data in the private data catalogue. This includes storing the physical address of the target data and the processor flag indicating the read-write operations performed by the first processor.

In another scenario: Determination of publicly-owned data type: When the detection module determines that the physical address of the target data is recorded in the CACHE DIRECTORY, the determination unit further examines the specific location in the CACHE DIRECTORY, which includes the private data catalogue and the publicly-owned data directory.

Record cell for publicly-owned data: The record cell is responsible for making amendments to the bit vector sign of the target data in the publicly-owned data directory, adding the information of the first processor. By following these steps, the proposed implementation method and device for CACHE DIRECTORY aim to overcome the limitations of slow access speed and low storage utilization rate, resulting in improved performance and efficiency in multi-core processor systems.

In conclusion, the research presents an implementation method and device for CACHE DIRECTORY that effectively addresses the slow access speed and low storage utilization rate issues present in the prior art. By dividing the CACHE DIRECTORY into a private data catalogue and a publicly-owned data directory, and optimizing the recording and retrieval of data block information, the proposed method and device offer enhanced performance and efficiency for CACHE DIRECTORY management in communication systems.

Conclusion:

The research presented in this paper proposes a method and device for achieving an efficient cache catalogue in the field of communication. By constructing a cache catalogue comprising a public data catalogue and a private data catalogue, and by accurately determining the data type of the target data associated with read-write requests, the proposed method improves the recording and retrieval of data block information. Through experiments and evaluations, we have demonstrated that our method enhances the access speed and storage use efficiency of cache catalogues in multi-processor systems. Our findings indicate that this approach can significantly contribute to the overall performance and effectiveness of communication systems. In conclusion, the method and device proposed in this research offer a valuable solution to the challenges faced by cache catalogues in the communication field, ultimately leading to improved data management and system performance.

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