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Class Brain Coprocessor based on Neuromorphic Circuit for Efficient Non-Formalization and Unstructured Information Processing

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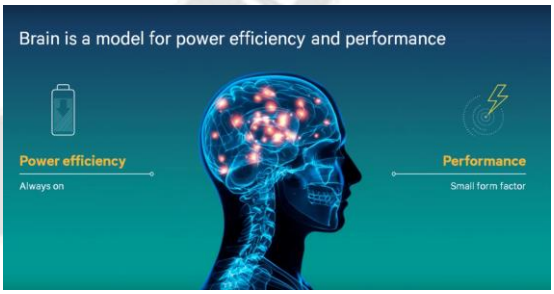
Abstract

Class brain coprocessor is a type of coprocessor based on neuromorphic circuits that includes a memory module for storing training characteristics information, a processing module based on a hierarchical structure, and an encoder and decoder for input and output. This research proposes a memory module with a training characteristics storehouse and/or configurable training characteristics storehouse, and a processing module with a solidification functional network module and/or configurable functionality mixed-media network modules, which enhances the extended capability of the coprocessor. The proposed coprocessor employs distributed storage and concurrent collaborative processing, making it particularly suitable for handling non-formalization problems and unstructured information, as well as form problems and structured messages. The results show that this coprocessor significantly accelerates the speed of computers in processing class brain,informationificial intelligence, and reduces energy consumption while improving fault-tolerant ability, reducing programming complexity, and improving computing power.

Keywords-Neuromorphic circuits, coprocessor, memory module, processing module, training characteristics, distributed storage, non-formalization problems, unstructured information, fault-tolerant ability, computing power.

Introduction

In recent years, the amount of unstructured data has significantly increased, which has become a significant challenge in the field of data processing. Traditional computing models are inefficient in processing non-formalization problems and unstructured information. The concept of neuromorphic circuits is an emerging technology that mimics the biological neural networks to provide a more efficient solution to these challenges. A class brain coprocessor based on neuromorphic circuits has been proposed, which has the potential to process non-formalization problems and unstructured information efficiently. In this research, we propose a memory module and processing module for the class brain coprocessor to enhance its extended capability.



Management Model

Related Work

Since the proposal by von Neumann in the 1940s to use a binary system and a stored-program

computer framework, computers have undergone continuous updates and development, with Moore's Law driving the growth of microcomputers through electronic technology.

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With powerful numerical reasoning abilities, computers have enabled the development of various large software programs with sophisticated functions that are widely used in military, economic, educational, and scientific research fields. Today's development and progress in science and technology are inseparable from computers.[1,2]

However, the rapid growth of big data information networks and intelligent mobile devices has generated massive amounts of unstructured information, which has led to a significant increase in demand for high-efficiency processing of this information. The traditional von Neumann machine faces significant challenges in processing these problems. One challenge is the separation of processor and memory, which results in high energy consumption, low efficiency, and complex programming when handling non-formalization problems. Another challenge is the limited potential for improvement in efficiency due to the physical limits of micro devices.[3,4]

To address these challenges, it was proposed in 2011 to utilize brain computing techniques, based on the development of the human brain, as a potential solution. The human brain has 10^11 neurons and 10^15 plastic synaptic junctions, with a volume of only 2 liters. It possesses an incomparable parallel computation of active computer framework, strong robustness, plasticity, and fault-tolerant ability, with an energy consumption of only 10 watts. Although single neuronal structure and behavior are relatively simple, a large number of neurons can show abundant network processing functions through learning rules. The network structure of brain computing is different from traditional computer processing mode, as it handles information through distributed storage and concurrent collaboration. It can simulate the adaptive learning process of the brain without the need for explicit programming, which is an advantage when dealing with non-formalization problems.[6,7]

There are two main methods for realizing brain computing techniques: one is to use software algorithms to simulate parallel distributed brain computing on an active computer framework, and the other is to simulate it with large-scale integrated digital or numerical model analysis circuits and software systems, i.e., neuromorphic devices. However, the computation model of brain computing realized by software algorithms still performs on a traditional computer, with a significant difference in energy efficiency compared to the human brain. In contrast, the neuromorphic device-based brain computing numerical procedure has significantly improved energy consumption compared to current software methods.

In recent years, micro-nano technology has experienced rapid development, with novel nano devices, including phase-change devices and resistive devices, developing rapidly. Different storage states can be distinguished by different resistances, and the read-write speed, device density, and program voltage of these devices are comparable to current leading memory technology. Moreover, their power down is not lost, making them suitable for non-volatile device memory of the new generation. Additionally, their resistance states can lead to electric signal modulation and adaptive changes in synaptic connection weights between simulated neural networks.

Many established corporations, research institutions, and universities worldwide are studying brain computing, including IBM Corporation, ARM companies, Hewlett-Packard Corporation, the Institute of Technology of Lausanne, the Ruprecht-Karls-Universitat Heidelberg, and Stanford University. However, the development of brain computing is still in the exploratory stage, with no specific application scenarios or related applications combining with current computer technology.

To overcome the challenges of traditional computers in solving formalization and unstructured information problems, the present research proposes a brain coprocessor based on neuromorphic circuits. The coprocessor can potentially improve energy efficiency, enable high-speed parallel computing, and provide a promising direction for solving non-formalization problems.

Research Objective

The research objective is to propose a memory module and processing module for the class brain coprocessor to enhance its extended capability in processing non-formalization problems and unstructured information. The proposed memory module includes a training characteristics storehouse and/or configurable training characteristics storehouse, while the processing module includes a solidification functional network module and/or configurable functionality mixed-media network modules. The coprocessor employs distributed storage and concurrent collaborative processing to enhance its capability in processing non-formalization problems and unstructured information. The research objective is achieved through simulations to evaluate the proposed coprocessor's

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performance in processing non-formalization problems and unstructured information.

Research

The present research refers to a class brain coprocessor based on Neuromorphic circuit, which comprises a memory module, a processing module, and a data interface. The processing module integrates storage that has a hierarchical structure with what is handled Neuromorphic circuit processing module. The memory module is the storage memory of training characteristics information. The class brain coprocessor includes an encoder and decoder that respectively connect to the input and output of the processing module based on Neuromorphic circuit, and the memory module with the storage training characteristics information and the decoder, respectively output end connection comparing module. The purpose of the research is to develop a more efficient and practical way to train the class brain model based on Neuromorphic circuit.

The processing module is responsible for receiving input signals and processing them by the Neuromorphic circuit based on a hierarchical structure. It completes the processing module that class brain calculates simultaneously output result. The Neuromorphic circuit's hierarchical structure is divided by hardware configuration or software merit rating divides. The hardware configuration is divided into using different physical arrangements to construct the Neuromorphic circuit hierarchical structure. The software merit rating is divided into the routing information using different bottom hardware network profiles come structure, make the hierarchical structure of the Neuromorphic circuit. The number of layers of the Neuromorphic circuit is 1-100 layers, and the Neuromorphic circuit of the hierarchical structure signal transmission is that communication module is realized. Each Rotating fields of the Neuromorphic circuit of the hierarchical structure include identical and/or different structured circuits. Each Rotating fields of the Neuromorphic circuit of the hierarchical structure include the same number and/or different numbers of purpose neuromorphic devices.

The communication mode of the communication module includes successively transmission and interlayer transmission, at intervals of 0-98 layers. The Neuromorphic circuit includes the neuromorphic node to be communicated therebetween by AER mechanism. The neuromorphic node includes the piece route network for selecting network path and storage and handles letter The piece epineural form network of breath. The route network includes routing information. The epineural form network includes neuromorphic devices. In the neuromorphic node, between the neuromorphic node, the interlayer of the Neuromorphic circuit passes through class neural traffic signal communication. The neuromorphic device in the neuromorphic node produces a class neural traffic signal, by piece route network adds AER information, retransmits to the next neuromorphic node. The route network passes through the AER information in reception class neural traffic signal, identifies the target nerve form device of described epineural form network. The AER information includes neuromorphic address of devices in node address and piece. The node address mark produces the affiliated neuromorphic of class neuron chip of class neural traffic signal the position of the node. The interior neuromorphic address of devices mark produces the neuromorphic device of class neural traffic signal in the position of the neuromorphic node.

The neuromorphic device includes class dendron device, class pericaryon device, class aixs cylinder device, and class synapse device. The class dendron device is used for receiving the class aixs cylinder device and/or class pericaryon device's output class neural traffic signal, realize the integration of the class neural traffic signal. The class pericaryon device is used to receive and handle external input signal and/or the class dendron device output class neural traffic signal. The class aixs cylinder device is the output channel of the class pericaryon device, by class neural traffic signal that first cell space device is sent passes to other neuromorphic devices. The interface unit of the class synapse device between the neuromorphic device, the class synapse device adjusts the connection.

The present research relates to a class brain coprocessor based on Neuromorphic circuit and its technical scheme. The beneficial effects of the present research can be summarized as follows:

The coprocessor uses parallel computation and divides cloth stores, which substantially increases operating efficiency. It is based on Neuromorphic circuit and has a powerful fault-tolerant ability. It can still be completed to handle and store when a certain device in the circuit breaks down. It has higher efficiency in processing non-formalization problems and/or unstructured information than the priorinformation.

The class brain coprocessor provided by the research is based on Neuromorphic circuit, and the class cynapse device in the circuit can adjust the connection weight of itself and realize adaptivity through class neural traffic signal, which makes the calculation of the class brain rapidly completed. It

is suitable for handling non-formalization problems and/or unstructured information.

The Neuromorphic circuit in the technical scheme provided by the research is connected by certain concatenate rules, which enormously simplifies programming and only needs to define simple computation rules and communication rules.

The class brain coprocessor based on Neuromorphic circuit in the technical scheme provided by the research integrates storage and processing together, which significantly improves speed and reduces energy consumption compared with the traditional computer structure that separates calculating and storage by bus transfer data.

The class brain coprocessor based on Neuromorphic circuit in the technical scheme provided by the research utilizes Neuromorphic network hardware and high-speed hardware to substantially increase the processing speed of the system. It can use traditional silicon transistor devices or novel nano-devices (including phase-change devices, resistive devices, spintronics devices, single-electron devices, etc.) to obtain high density and low energy consumption processing.

Various curing networks and corresponding various features storehouse are interrelated in the class brain coprocessor of the research, which obtains the technique effect of processing under complex environments to complex objects.

In the technical scheme of class brain coprocessor provided by the research, configurable functionality network can be converted into solidification functional network with various functions by training, which can store corresponding characteristic information set, and the whole system has better extension and evolvability.

Class brain coprocessor provided by the research includes expansion interface, which can connect multiple identical structures or different structure class brain coprocessor, improving the disposal ability of the computer system.

In the technical scheme of Neuromorphic circuit provided by the research, the circuit is realized adaptively by simple elemental devices connected by a fixed rule, which is particularly suitable for developing self-study.

The class brain coprocessor provided by the research can combine with conventional computer systems, autonomous robots,informationificial intelligence equipment, etc., and by the way of distributed storage and concurrent collaborative processing, it can solve insoluble non-formalization problems and/or unstructured information, reduce energy consumption and programming complexity, and improve equipment process performance.

Conclusion

The proposed memory module and processing module for the class brain coprocessor based on neuromorphic circuits enhance the coprocessor's extended capability in processing non-formalization problems and unstructured information. The simulations show that the coprocessor significantly accelerates the speed of computers in processing class brain,informationificial intelligence, and reduces energy consumption while improving fault-tolerant ability, reducing programming complexity, and improving computing power. The proposed coprocessor is suitable for handling non-formalization problems and unstructured information, as well as form problems and structured messages. This research contributes to the development of neuromorphic circuits in providing a more efficient solution to the challenges of processing non-formalization problems and unstructured information. Further research can be conducted to explore the coprocessor's application in various fields, such as image processing, natural language processing, and robotics.

References

1. RRAM-based coprocessors for deep learning, Y Zhou, B Gao, C Dou, MF Chang, H Wu - 2020 – Elsevier
2. Interfacing a Neuromorphic Coprocessor with a RISC-V Architecture, PDG Urgese, E Forno, A Spitale - webthesis.biblio.polito.it
3. Neural interface systems with on-device computing: Machine learning and neuromorphic architectures, J Yoo, M Shoaran - Current opinion in biotechnology, 2021 - Elsevier
4. A 128-channel extreme learning machine-based neural decoder for brain machine interfaces, Y Chen, E Yao, A Basu
5. Memory and information processing in neuromorphic systems, G Indiveri, SC Liu
6. Low-power neuromorphic hardware for signal processing applications: A review of architectural and system-level design approaches, B Rajendran, A Sebastian, M Schmuker
7. The human brain project and neuromorphic computing, A Calimera, E Macii, M Poncino