International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

Protection Scheme based on Artificial Neural Network for Fault Detection and Classification in Low Voltage PV-Based DC Microgrid

Ramaprasanna Dalai[1]*, Sarat Chandra Swain[2]
[1]Research Scholar,
KIIT University,
Bhubaneswar, Odisha, India,
Email: 1781047@kiit.ac.in
[2]Professor,
KIIT University,
Bhubaneswar, Odisha, India,
Email: scswainfel@kiit.ac.in

Abstract— With the expansion of the DC distribution market, protection, and operational concerns for Direct Current (DC) Microgrids have increased. Different systems have been investigated for detecting, finding, and isolating defects utilising a variety of protective mechanisms. It might be difficult to locate high-resistance faults and shorted DC faults on low-voltage DC (LVDC) microgrids. Therefore, in this study, a Field Transform Technique like Short-Time Fourier Transform (STFT) is proposed for detecting the Fault Current (FC). This method detects the faults Pole-ground (PG), pole-pole (PP), and Arc fault are the major fault types in the DC network with PG fault as the most common and less severe. One of the difficulties the DC system faces in the incidence of a malfunction is the protection of essential converters. During this fault, the diodes, being the most vulnerable component of the system, may encounter a substantial surge in current, which can potentially cause damage if the current surpasses double their specified capacity for withstanding. After the Fault detection (FD), a Taguchi-based ANN is presented to classify the detected faults. This method effectively classifies PV-based faults. Then, to safeguard the FC, the Improved Self-Adaptive Solid State Circuit Breaker (I-SSCB) is introduced. It safeguards the FC in the low-voltage PV-based DC microgrid (DCMG) and restricts FC in the DCMG. The suggested approach is evaluated using the Matlab software and the proposed method produces 400A current and 100 KW power during the PV temperature of 25°C. The output current of the ANN is then 1A for a duration of 0.3 to 0.4 seconds. The fault voltage and FC produced in this proposed work are 1900V and 1950A. Therefore, the proposed work's current and voltage values are 21 KV and 0.35 I. Therefore, the proposed method produces more power and limits the FC in the LV-DCMG. In future studies, the improved or modified neural network or machine learning (ML)-based techniques can be utilized which may improve the protection scheme of the work.

Keywords- DC Microgrid, Low Voltage PV, Fault Detection, Field Transform Technique, Short-Time Fourier Transform, Fault Classification, Taguchi-Based Artificial Neural Network, FC Protection, and Improved Self-Adaptive Solid State Circuit Breaker.

I. INTRODUCTION

Solar photovoltaic (PV) generation is the most popular renewable distributed energy source (DER) in a microgrid due to the lower cost and economic operation, and the abundance of solar energy available. Due to the operation of primary loads, DC power is a necessity and it is an electronic-based device. In today's world, PV-integrated DCMG is a viable option. However, major protection difficulties exist in PV-integrated DCMG because of the PV's irregular characteristics and unpredictable nature. Faults, nuisance tripping islanding phenomenon, etc. are serious protection concerns. For the system's effective operation, determining the kind of responsibility is crucial, therefore, fault protection is the most difficult challenge among these issues [1]. To retain electrical power deprived of trust on the main grid, DCMG is gaining popularity as a feasible option for consumers. In comparison to typical AC distribution systems (DS), a microgrid has a short distribution line length and covers a small geographical area. Protection is a crucial concern when it comes to the seamless operation and control of DCMG. PV arc faults or short circuit line-ground (L-G) and line-line (L-L) are the faults in a solar-PV-based DCMG system based on the topologies and system components [2].

Based on the PV array's series/parallel architecture, a PV-based DG is more prone to DC arcing issues. Series, parallel: intra-string, arcing ground and cross-string are the different types of arc fault events that are recorded for each PV structure [3]. DCMG has gained popularity as a result of the rise of photovoltaic renewable energy sources, DC electrical loads, and energy storage devices, making them a feasible option for AC microgrids. Modern power electronics (PE) and control algorithms enable the DCMGs' dependable functioning and effective installation. Improved dependability, transmission capacity, less complicated control, and power quality are the number advantages of DC systems over their AC counterparts. Because of the DC's nature, the security of DC systems is more difficult [4]. To adequately protect LVDC microgrids from DC faults, a protection mechanism in a DC environment obligation meet certain criteria. To avoid possible harm to microgrid components, the protection strategy obligation be as soon as you can and it is necessary to only detach the faulty portion without disrupting the process of the microgrid [5]. A few unique characteristics are presented in

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

the converter-dominated DCMG that has a lack of a suitable protection mechanism is the primary implementation challenge. Fault interruption and arc quenching are difficult when compared to its AC equivalent, the DC lacks natural zero crossing [6].

DC Microgrids

Due to the fewer stages of power conversion, DCMGs can allow more effective integration of distributed generators (DGs), such as electronic loads, solar PVs, and battery energy storage. For future power systems, DCMGs have emerged as an appealing option, with the new developments in smart homes/ buildings, vehicle-to-grid technology, renewable energy parks, the power sector, and hybrid energy storage. For the wide-scale custom of DCMGs, the lack of reliable FD methods in the usage of DC–DS is a considerable impediment [7]. Because of the current limiting nature of the DC-DC power converters, the nominal FC in the DCMG system can be actively reduced, increasing the difficulty of FD in the DCMG. Furthermore, during DC faults, through power converters, several sources are associated with the distribution bus and feed the fault. Based on the route resistance and fault location (FL), the algorithm calculates the FC's magnitude. During normal operation, the FC's magnitude may not be much different from the magnitude expected since the power converters limit current flow. As a result, detecting a DC fault in the system is extremely difficult. These insignificant disturbances are quite comparable to the current variance that occurs when load steps are changed, the source is changed, and supercapacitors are connected, among other things, [8]. Unit protection and non-unit protection are the two different forms of security measures for DCMG. Common DC buses, energy storage devices like batteries or supercapacitor banks, loads and power electronic converters, etc., are the designated areas of a DCMG to protect this, a unit protection method is implemented. In general, In the designated zones of DCMG, current deviations are estimated based on Kirchhoff's current law, and against the fault, the protected area is the only one in that zone. Differential protection methods are an example of this type [9].

For FD and location, the buses' capacitor current and voltage are essential, and recently for the DC network, a novel protection system has been patented. To detect fault without de-energizing the system, a probe power unit with a novel step is applied to propose a non-iterative fault-location technique. It detects and processes faults using intelligent electronic devices (IEDs) placed in the line [10]. There are issues with DCMG safety for there aren't strong rules for their protection [11]. In important applications like military bases, islands, and space stations, in microgrids, autonomous FL is vital for timely maintenance and restoration. It's also essential for networks with underground wires that can't be inspected visually. Boosting the microgrid's robustness, and early detection of the FL aids in early restoration. For FL identification, offline methods are exploited, and for immediate isolation, fast FD methods are employed [12]. In microgrids where distributed generation is connected to inverters, conventional fault detection (FD) systems often prove inadequate due to their dependence on large fault currents (FC).

J.Q. James *et al* 2017 [13] propose a deep neural network-based intelligent FD and wavelet transform technique for microgrids. This approach intends to provide service recovery and microgrid protection with fast phase, location, and fault type information. The dispersed wavelet transformation is utilized to excerpt the statistical structures for pre-processed protective relays which sampled the branch current measurements. Then, to build fault information, all accessible data is fed into deep neural networks. In an AC/DC hybrid distribution system (HDS), flexibly control transmission power which is enabled by the DCMG's application. During regular operation, it can assure efficient device access, and in an emergency, it can provide fast cross-region power assistance. There are numerous advantages to DCMG over the standard AC grid and it is rapidly expanding. The impact caused by a DCMG short circuit is more serious than that in an AC grid for the line impedance in opposed to an AC grid, DCMG is lower. It is more difficult to cut off the faulty line in the AC grid for zero-crossings are not present in the faulty current in the DCMG. Addressing fault protection in AC/DC HDSs has become a significant challenge with the emergence of DCmg development [14].

Converters for PE losses can be considerably decreased by using the LVdcmg. Increased power transfer capabilities, cost savings, improved power quality, increased efficiency due to fewer conversion stages, and higher reliability are the number advantages of the LVdcmg. Energy losses are reduced when deployed LVdcmg [15]. In this work, a field transform-based technique is presented to detect the FC in the PV-based DCMG system. It detects all the FC. After that classify this detected fault using ANN. Using the several fault kinds, it categorises the fault. Then protect the FC using I-SSCB which is utilized for the FC limit process in the low voltage PV-based DCMG. The remaining part of the document is well-structured as follows, section 2 depicts the literature survey of the study, and Section 3 illustrates the problem definition and motivation of the research. Then the proposed research's methodology is portrayed in section 4, the experimentation and the result discussion is established in section 5, and section 6 reveals the research conclusion, respectively.

II. Literature Survey

The study is the foundation for the literature review of FD and power protection in DCMG. This paper presented FD and classification methods like Field Transform-based STFT for FD. Then ANN for faults classification. This method notices and categorizes the faults, respectively.

N. Yadav *et al.* 2021 [16] offer an FD technique based on a unique short-circuit (SC) for low-voltage DCMG protection. SC the majority of things are flawed DC power system defects, and if not isolated, they can cause serious problems. A DCMG is dominated by a capacitor grid, hence the recommended method takes advantage of the current events of the filter capacitors. The application for implementing the suggested FD scheme is being built using an LV-DCMG system. A DC cable, solid-state relays, and DC-DC converter through active sources like batteries and solar PV are connected to passive loads. Both low and high-impedance defects can be detected using the proposed method.

FD and locating approaches for multi-terminal DCMG according to a local measurement were presented by Yang, Y, *et al.* 2021 [17]. This paper begins by defining and illustrating a novel notion known as pseudo voltage. Following DCMG problems, the line voltage's characteristics are analysed to determine the requirements for distinguishing between exterior and internal faults. Then, based on the pseudo voltage principle, an FD method is suggested. By depending solely on

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

specific capacities, the arrangement can secure the entire DC line without any communication. Meanwhile, this study introduces an FL technique that incorporates the placement of an additional capacitor on the inner side of the DCCB. The test system utilises a DCMG model with five terminals. The consequences display that the suggested method can swiftly locate the careful area of the problem and identify the DC line fault fragment.

In MVDCMG, classify, locate and detect various dc fault types, a new travelling-wave (TW)-based approach is proposed by Saleh, K.A., *et al* 2017 [18]. Unlike previous TW-based FL and protection approaches, the suggested strategy (i) when a fault occurs, usages the earliest locally measured TW, and (ii) focuses on the TW's polarity and waveform characteristics rather than its arrival timing. As a result, it requires no connection, and the offered solution is faster than alternative approaches. As a result, both primary and secondary defences function effectively.

In such DCMG, Subramaniam, K, *et al.* 2019 [19] suggested a new cost-effective defense method for selective isolation, fast identification, and system recovery from short circuit and high impedance failures. There is no SSCB in custom, and it is performed by coordinating the output of foundation converters with clever three-tie contactor switch units (ICU). At each source contactor and converter, high-impedance defects are discovered using a multi-resolution analysis of locally recorded current signals using a DWT and a classifier based on K-nearest neighbours. The set by the Programmable relay devices deployed at each ICU node in the system provides the selectivity set to adaptive resistance time curves.

Wang, T, *et al* 2020 [20] proposed an FDI method using the SDOC regularity information for damages. The coherence between the single characteristic in the SDOC and the short-circuit defect in DC lines is first proven and applied to FDI as the article's main contribution. In addition, a stationary wavelet transform (SWT)-based singularity identification method is presented. Based on only local current measurements, this FDI approach can achieve fault-type classification in addition to fault isolation. A 5-kV three-terminal DCMG model hardware test based on dual-active-bridge (DAB) converters was utilized to check the efficiency of this FDI approach under real-time (RT) numerous fault scenarios are simulated. To various topologies and converters in damages, this FDI approach can be applied.

A new line-to-line fault and earth fault with a low resistance protection technique for multi-terminal DCMGs was presented by Chauhan, R.K., *et al* [21] in 2020. The scheme separates the DCMG from the faulty part. As part of a system of ring main DC buses, healthy parts work without interruption, and supply stability is preserved. Current sensors are put on DC bus segments to track the currents entering and exiting at various nodes. To ascertain the current differential between together ends of the service mains, current sensors are positioned at equal ends of the mains for measurement purposes. The circuit breakers are opened and the current differential is detected by the controller.

Gashteroodkhani, O.A, *et al.* 2019 [22] proposed a new microgrid defense strategy founded on the Time-Time (TT) alter. To compute the TT matrices, currents in the bus are first administered through the TT transform. Generated a suitable index based on TT-matrix z-score vector and the fault patterns are determined. Faults are categorised and identified using a threshold a few cycles after they occur in both islanded and grid-connected modes. The low signal-to-noise ratios (SNRs) are accommodated based on the unscented transformation (UT) which is utilized for the threshold selection strategy. For two separate microgrids (MGs), PSCAD/EMTDC software is applied to test the protection mechanism through extensive simulations. Reliably classifying and detecting faults by this approach is verified in the results. Under highly noisy conditions, this method performs well and to changes in fault parameters, this method is robust.

Salehi, M., et al. 2019 [23] describe a protection approach for LVDCMGs with ring-bus which employs SSCBs and IEDs. The design of the plan is based on this calculation. In the amount of momentary issues, the protection plan includes a reclosing strategy to restore the isolated zone in addition to a backup security plan in case the SSCB fails. Within microgrid lines, the suggested technique can detect and categorise PG and PP faults. For high-impedance FD, it is effective, and for load laterals and distributed energy resources, it consists of defence mechanisms.

Montoya, R., et al. 2022 [24] offer a travelling wave (TW)-based approach for DCMG rapid-tripping protection. Those with a high frequency of DC FC are calculated using a DWT in this study. At various frequency ranges, TW components are detected utilising multiresolution analysis (MRA) with DWT. This trained decoder is then utilized to categorize the responsibility type and estimate the location of the defect on the DC cables. Shamsoddini, M., *et al* [25] provide a swift and targeted protection scheme in 2020, which provides the LVDCMGs required tripping. The FC's inherent features served as the foundation for this protection approach and the first and second derivatives of the FC were employed to generate thresholds for differentiating between faulty and unflawed circumstances. Compensating gains have been added to the threshold definition to strengthen the protection scheme's FD capacity, and to line current amplitude, making the thresholds flexible. Instantly identify any kind of defect; no communication link is required; additionally, every measurement is local.

A localization, classification, and fault detection approach was presented by Hong *et al*., in 2020 [26] and is based on a Taguchi-founded artificial neural network (ANN) and a MRA of the discrete wavelet transform (DWT). As a result, the RX 62T microcontrollers demand more ROM space than those required for the suggested technique and the decision tree. For all three techniques, the RAM and package data requirements are essentially the same. The combination of a reciprocal HSSCB with a self-acclimate DC diminutive existing regulator, an ultra-fast switch, and a power electronic switch was the topic of Yaqobi *et al*., 2021 [27] study. The primary aim of this investigation is to speedily and effectively vibrate faults using HSSCBs and self-adapting FCL circuits. The DC fault authorization time will be faster, and it might not negatively impact the LV DC system's regular operation. It has been determined from simulation results and system configuration analysis that the type and arrangement of protective devices affect the speed of DC fault detection and interruption.

III. Research Problem Definition And Motivation

Due to the requirement for ultra-high-speed fault identification and isolation, protecting DCMGs is a challenging task. Due to the time window and limited data,

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

this makes system restoration and FL much more difficult. One of the hindrances and roadblocks to the LVDC's implementation of microgrids is the nonappearance of sufficient FD techniques for overall protection. For protection schemes, the LVDC system's control and operation principles provide significant issues. In an LVDCMG, both the fault level and the pace of FC growth are very high, for the power electronic converters, which causes severe damage. Swiftly detecting and isolating errors by the protection schemes. Another difficult issue is DG integration into the DCMG using the converters to limit the FC. Additionally, the inherent difficulty in protecting DCMGs arises from the absenteeism of points, which are crucial for arc interruption in DC power systems. PP and PG problems are the most frequent ones in a DC microgrid. At the middle of the negative and positive poles, the fault route of a PP fault lies, PG faults, instead, develop when the fault path passes between these poles and the ground.

In DCMGs, grounding is critical for FD, lowering common-mode voltage, and minimising leakage currents for personal safety. Different fault characteristics result in different types of grounding, which affects relay settings and protection design. DCMG is still a difficult task that needs to be improved for designing the best grounding system. There is a need to develop the DCCBs based on solid-state technology with the current-limiting abilities and the design of fast-acting grounding devices, to find the solution for these issues. Appreciation of the nonappearance of touching elements, SSCBs can swiftly switch within microseconds without any contact erosion or arc formation. Because the gate requires less power to operate and is widely employed in commerce, IGBTs are frequently exploited. The steady-state power loss is increased by on-state resistance. Furthermore, due to their low blocking voltage, SSCBs are not appropriate for high-voltage applications. SSCBs are most frequently employed in MVDC and LVDC systems, which operate at medium and low voltages, respectively. This motivates us to present an architecture that is best suited as a solution to different challenges raised by grounding, zero crossings, converter configuration, and imbalanced current, to protect the system from different faults and disturbances.

IV. Proposed Research Methodology

Due to their advantages in terms of increased power transmission capability, high efficiency, compatibility with DERs, and decreased losses, DCMGs have recently attracted a lot of attention. However, because of the difficulties of developing a trustworthy protection strategy, the adoption of DCMGs has been constrained. Faults in DC systems put forth different operational characteristics to its system parameters and short circuits existing in the DC buses. Usually, it increases at an earlier rate to an abnormally high value in comparison to the AC microgrid counterpart. To perform reliably, the traditional system fails because of the different topologies and characteristics of the DCMGs Due to this many issues arise and to handle these challenges, need for further improvement. A rapid and efficient FD technique, proper grounding design, proper DCCB, and an FC limiting method are all desired to handle the issues of DCMG protection. Therefore, a robust, reliable system is required to make DCMG faults prove efficient along effective.

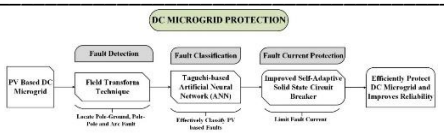


Figure 1. Proposed work block diagram

The work of the suggested technique is exposed in figure 1. It shows a DCMG system based on photovoltaics. While protecting the DCMG system, classification and FD are important processes. A field transform technique is proposed for detecting the faults, it locates the PG, PP, and arc faults. Then the detected faults are classified using the Taguchi-based ANN, which effectively classifies PV-based faults. After that, an improved self-adaptive SSCB is presented for FC protection. This will limit the FC, and the proposed method efficiently protects the DCMG and improves reliability.

A. Structure of DC Microgrid

An array of parallel-connected PV systems in a Multi-Terminal DC Network (MTDC), a variety of DC loads, in this investigation, an AC-DC rectifier and diesel generator with an AC utility interface and a VSC was exploited. The proposed approach in this exploration takes into account the DC side network. During a steady-state power flow solution, DC cables are often resistive. In terms of shunt capacitive reactance and series inductive reactance, transient performance is expressed, when a DC wire suddenly fails. When the DC arc liability has a high reactance path, and when calculating PG faults, this reactance is significant. The system's connection to PV, DC arc responsibility is a phenomenon where PV arrays or modules are not grounded properly and DC cables adjacent to that system are subjected to PG fault. For DC microgrids are intended to be utilised as a first line of defence against unstable power supplies rather than as long lines, the distance between the DC cable-based distributing terminals is anticipated to be 3 km. These feeders include DCCBs and hall sensors built into both of their ends, which are where the current enters and exits. Fastness in this DC network unit protection is due to non-iterative calculation, involvement of high-frequency switching for PE converters (DC-DC, VSC) and high FC as compared with AC networks. When a fault occurs and the fault detection (FD) threshold is reached, the circuit breaker's switching action will rely on the measurement of the differential current. The positions of the internal and external zone faults are X and Y, respectively.

B. DC Circuit Breaker

The absence of well-defined protection standards poses significant challenges to the defence of DCMG. DC breakers are studied less as associated with AC breakers for distribution-level applications. Using DCCB as an execution unit, fault lines can be disconnected, making it a crucial part of DC system protection. Swiftly turning off and isolating the FC is difficult for the DCCB, because of the nature of the DC. The protection zones for DCMG systems are motionless in the initial stages of development, primarily due to the limited availability of DC Circuit Breakers (CBs) that can handle the required current and voltage ranges. To ensure that DC microgrids operate trustworthily, there is a bidirectional O-shaped impedance connection circuit breaker available.

1. Bidirectional O-Z-Source Circuit Breaker

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

The new z-source circuit breaker is simple, reliable, and inexpensive and can interrupt large DC voltages and currents under the natural commutation principle. When a transient error occurs, the Z-source breaker generates a zero crossing by connecting an SCR in series with various LC circuit topologies. When zero crossing occurs the SCR is naturally commutated off before the FC exceeds the turn-off capability and the fault is removed from the source. Without the custom of an additional control mechanism that first detects the issue before sending a signal to fix it, natural commutation aids in fault evaporating. There are three main topologies of a z-source breaker. In this work, are using the series topology of the Z- cause breaker.

This topology offers several advantages, including the presence of ground availability between the source and load, besides the additional benefit of lower reflected fault current on the source compared to the parallel z-source breaker architecture.

Circuit Modeling and Component Sizing

In this section, breaker responses under various load conditions including severe short-circuit faults, less severe faults with a detectable fault ramp rate, and normal step-load changes are mathematically modelled. The resulting equations are extremely helpful in directing the usage of the suggested OZSCB. The leakage inductances, internal resistances, and SCR ON-state voltage dips are all disregarded to streamline the analysis. To enhance the design of the breaker, the capacitor is modelled with an equivalent series resistance, which should be taken into account if additional resistances are required to dampen resonances.

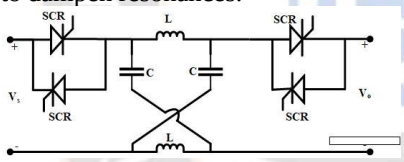


Figure 2. Z-source bidirectional circuit breaker

As the most severe DC circuit fault, a short circuit at the output will force the output voltage sharply to zero. At this moment, the transformer winding T_1 withstands the source voltage V_s, and the capacitor is uncharged. According to Kirchhoff's voltage law (KVL), one can obtain,

$$\left\{\begin{array}{l} V_s = v_{T_1}(t) \\ V_s = \frac{1}{C}\int_0^t i_{T_2}(\tau)d\tau + r i_{T_2}(t) + v_{T_2}(t) \end{array}\right\} \quad (1)$$

The terminal equations of the two-winding transformer can be entirely determined by its inductance matrix as

$$\begin{bmatrix} v_{T_1}(t) \\ v_{T2}(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{T_1}(t) \\ i_{T_2}(t) \end{bmatrix} \quad (2)$$

Where L_{12} are the connected inductors' mutual inductance, and L_{11} L_{22} are the self-inductance primary and secondary ranges. By failing to consider the connected inductors' leakage inductances, the mutual inductance can also be derived as

$$L_{12} = \sqrt{L_{11} L_{22}} \quad (3)$$

Substituting (2) into (1) and eliminating i_{T_1} yields

$$\left(L_{22} - \frac{L_{12}^2}{L_{11}}\right)\frac{d^2 i_{T_2}(t)}{dt^2} + r\frac{d i_{T_2}(t)}{dt} + \frac{1}{C} i_{T_2}(t) = 0 \quad (4)$$

From (3), the coefficient of the second-order term in (4) equals zero, simplifying it into a first-order differential equation. Solving (4) with transformer turn ratio n, one obtains

$$i_{T_1 2}(t) = \frac{(n-1)V_s}{nr} e^{\frac{1}{rC}} \quad (5)$$

Then, the current of T_1, i.e., the SCR current, can be similarly derived as

$$i_{T_{11}}(t) = \frac{V_s}{R_L} + \frac{V_s}{L_{11}} t - \frac{(n-1)V_s}{n^2 r} e^{-\frac{1}{rC}} \quad (6)$$

Where R_L represents the load resistance

To reliably trip the SCR, $i_{T_{11}}(t)$ should remain negative until the SCR finishes its reverse recovery. Typically, the time necessary for the reverse recovery is slightly shorter than the rated SCR turn-OFF time t_q. Since the derivative of (6) concerning time retains positive when $n>1$, which indicates an increasing tendency $i_{T_{11}}(t)$, the reliable turn-OFF of the SCR can be guaranteed by

$$i_{T_{11}}(t_q) = \frac{V_s}{R_L} + \frac{V_s}{L_{11}} t_q - \frac{(n-1)V_s}{n^2 r} e^{-\frac{t_q}{rC}} \le 0 \quad (7)$$

From (7), $i_{T_{11}}(t_q)$ is a responsibility of n, r, C, and L_{11}, which all remain to be determined. Making expenditure of the partial unoriginal of (7) concerning r, the minimum $i_{T_{11}}(t_q)$ can be found when

$$r = \frac{t_q}{C} \quad (8)$$

Then, substituting (8) back into (7) yields

$$C \ge \frac{n^2 t_q e}{n-1}\left(\frac{1}{R_L} + \frac{t_q}{L_{11}}\right) \quad (9)$$

According to (9), a higher normal load generally necessitates a superior capacitor. Increasing the transformer inductance will decrease the capacitance, which will unfavourably result in a larger transformer volume. A shorter turn-off time allows a considerably smaller capacitor along with faster tripping; thus, a fast recovery SCR is preferred for a compact OZSCB.

Furthermore, a partial imitative of (9) n indicates that the minimum capacitance obligatory for short-circuit protection is

$$C_{\min} = 4e\left(\frac{t_q}{R_L} + \frac{t_q^2}{L_{11}}\right) \quad (10)$$

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

When $n=2$.

In dc microgrids, step-load changes can be common during normal operation and this guarantees the reliable operation of dc microgrids.

C. FD and Classification in DC Microgrid

A DC microgrid's power electrical equipment may experience overcurrent during short circuit faults. For DC bus schemes that cannot handle high FC, a robust DC line protection solution is necessary. Arc failures put DCMG at constant risk of fire, and solar PV is an essential part of a DC microgrid. When the responsibility is not discovered promptly, it not only ruins the microgrid nonetheless also poses a significant risk to the operator's safety. A rupture connection or increased connectivity between two nearby bare cables frequently results in a series arc fault. In Low-Voltage-DC-microgrid (LVDCMG), FD and location issues have been introduced in this study due to improvements in Artificial Intelligence (AI) and the appropriate performance of AC microgrid's smart protection methods. Subsequently, the research work proposed the Field Transform technique and ANN for FL and classification in DC microgrids. The main bus voltage and the feeder current are measured to accomplish the FD and location.

1. FD Based on Short-Time Fourier Transform (STFT)

The STFT is a field transform technique. The strength of each component is calculated and Fourier analyses have broken down a signal into its frequency constituents. The information about the time of the frequency event is not provided by the Fourier analysis. When Fourier transform is applied to a discrete-time signal the result is not always as theoretically expected. The anticipated transform output in the situation of a sinusoidal wave is a glance at the matching frequency bin. Across the frequency spectrum, causing the wave's frequency response to be dispersed which is caused by spectral leakage. At the observation interval's boundaries, this is discontinuity. For it has a discontinuity, a periodic expansion of the signal is incorrect.

Spectral leakage is limited by using the window functions. These routines try to lessen the order of discontinuity at the border by signal smoothing at the interval's conclusion. The signal is brought to zero at the boundary. There are numerous window functions accessible, each with its own set of properties. The 3 dB bandwidth, side lobe fall-off, and highest side lobe level are examples of merit figures. The flat-top window can be utilised to calculate the largeness of the frequency spectrum components.

At the limits (accept the rectangle), every window function decreases to zero. Windowing the signal at regular intervals will cause some of the data to be lost, and windows essentially overlap. The equation for the STFT of a discrete-time domain signal $l(p)$ is:

$$STFT(p,r)=\sum_{p=0}^{N-1} l(p)x(p-qI)e^{-j\frac{2\pi}{P}rp} \quad (11)$$

Where p is the sample index, r the frequency index, P the interval length, $x(p)$ the window function, q the window position and I the distance between each window's hops.

The frequency components of the current signal are separated. The DC is nearly flat when the system is functioning normally. As can be seen, the primary lobe (The measurement signal's DC component) is where the power is focused. The power focused in the main lobe during current transients (faults or load fluctuations) diffused over the entire frequency spectrum, i.e., Expanding the distance of the side lobes. As a result, an FD method can leverage this existence.

In this enquiry, according to references [26], the Hanning window function was exploited, which is defined below:

$$Hann(d)=\frac{1}{2}+\frac{1}{2}\cos(2\pi d/\sigma) \quad (12)$$

In which, $n=0,1,\ldots,U-1$ and U represents the window length equal to the amount of points in the window. The analytic signal $l(m)$ is defined as follows

$$l(m)=t(m)+jH[t(m)] \quad (13)$$

Where, $t(m)$ is a real signal and $H(m)$ represents the Hilbert transform [27]. The Hilbert transform is stated as follows:

$$H[t(m)]=1/\pi S\int_{-\infty}^{\infty}\frac{t(\sigma)}{(m-\sigma)}d\sigma \quad (14)$$

In this situation, the Cauchy Principal Value is denoted as S. A fixed-time window requisite be utilized when performing the rapid Fourier transformation. Throughout all transitions, the function's extension $h(m)$ is consistent. In general, this extension is proportional to half of the function $h(\rho)$ and is self-governing of the centre frequency. The function $h(\rho)$ is the Fourier transformation result $h(m)$. The STFT function was the first to be suggested for processing signals simultaneously in the period field and frequency domain. In terms of time-frequency distribution, STFT is linear. One disadvantage of the linear time-frequency distributions is the inescapable correlation between spectral and temporal resolutions [28].

As a result, this work utilizes the second power of STFT called a spectrogram. The following equation is the responsibility of a spectrogram:

$$L_l(m,\rho)=\left(\sum_{p=0}^{N-1} l(p)x(p-qI)e^{-j\frac{2\pi}{P}rp}\right)^2 \quad (15)$$

Analytic and spectrogram signals are represented by sub-script l and upper-case L, respectively [29, 30]. Utilizing this STFT method, the faults are detected and the detected faults are classified based on the ANN, which is detail elucidated in the following sub-section.

2. ANN

Construct a simple ANN that can organize the faults and identify the faulty location within or outside the microgrid. For the ANN, the differences between the wavelet entropies of any two phases of input data are utilized for this no complex ANN structure is required, improving the accuracy of organization and location. The Taguchi method's (TM) orthogonal array (OA) is employed to generate a limited set of training data for the ANN, eliminating the need for a very large number of random data to train the ANN. This will reduce the cost and time of developing an ANN.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

The effects of numerous factors on the growth of an arrangement are the emphasis of the experiment's design (DOE). The DOE improves the production process design of the system. If all blend of the different factors is considered, then full factorial experiments will be conducted to achieve the design. The TM considers only orthogonal experiments to decrease the quantity of research to be performed. Restated, OAs are exploited in the TM to analyse the output reply of a scheme using a minimal amount of investigation. This experimental approach is a slight factorial design, which considers combinations of various factors at different levels. The symbol for an OA is $U_a\left(b^c\right)$, where a, b, and c are the numbers of experiments, levels, and factors, respectively. As summarized in Table I, the OA$U_4\left(2^3\right)$ consists of two factors (X, Y, and Z) and each factor has two levels; in total, only four orthogonal experiments U_1-U_4 need to be performed if the inputs are fixed. However, if a problem has three factors and each factor has two levels, then $\left(2^3\right)\left(8\right)$ full factorial investigations are required. That is, the remaining 4 experiments are dependent on the essential nine experiments summarized in Table I.

TABLE I. ORTHOGONAL ARRAY

Experiments	X	Y	Z
U1	1	1	1
U2	1	2	2
U3	2	1	2
U4	2	2	1

An "OA" in the TM meets the following two properties.

- The number of different columns with varying levels is the same: for example, the 2nd–4th columns in Table I individually consist of two 1 s and two 2 s. Accordingly, the influence of each level of an issue on the output is the same.
- All combinations of levels in any two columns appear an equal number of times. Specifically, in Table I, when considering factors, X and Y, combined levels 1-1, 1-2, 2-1, and 2-2 appear U_1-U_4, respectively. When Z and Y are considered, combined levels 1-1, 2-2, 1-2, and 2-1 appear U_1-U_4, respectively.

For various levels and numbers of variables, Taguchi presents a variety of OAs. These arrays offer the advantage of minimizing the required number of tests and simplifying the data analysis process. There are about requests of the TM, e.g., multi-scenario design and machine design. The OA in this inquiry is applied to produce substantial and constrained datasets for the training of the ANN. The TM requires the following five elements,

- The system is the mechanism that produces the response; the microgrid is the system herein.
- The input is the driver of the system; the fault inside or outside the microgrid is the driver.
- The output is the system response; the three-phase voltages and currents near the static switch are the output.
- The noise affects the output response to the input; fault types (balanced or unbalanced faults) are considered herein.

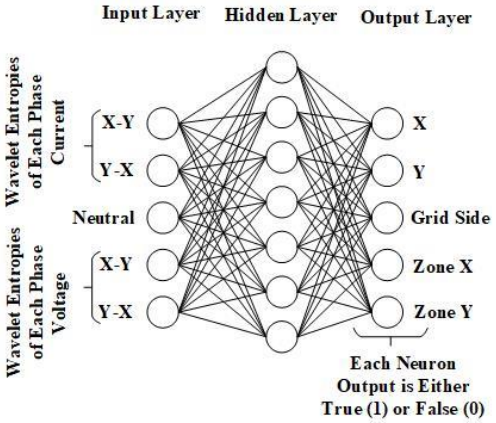
The variables impact the system's output. The load level (kVA), solar irradiance $\left(W/m^2\right)$, and short-circuit capacity (MVA) at the utility grid side are the factors herein. These elements are referred to as elements X, Y, and Z, in that order.

Specifically, the fault types are balanced three-phase to the ground or three phases shorted and unbalanced two-phase to ground, phase-to-phase, or one-phase to ground. In all, 11 types of faults may occur at each FL. Three fault locations occurred at Zone X, Zone Y, and the utility or grid side are considered. The next step in selecting the Ois to decide how many levels there will be of each factor and the value of each level. Since all factors may have a range of values, maximum, medium, and lowest values for each factor are set as three levels.

Artificial Neural Network

To implement an ANN in a chip, the structure of an ANN needs to be simple and effective for solving the problem. The ANN is implemented because it has learning capability. The ANN applied in the paper is a three-layered network with the following five inputs: the differences between the added wavelet entropies at scales two and three of each phase voltage $\left(V_{X-Y}\right)$, the differences between phase currents $\left(I_{X-Y}\right)$, and the wavelet entropy of the neutral current $\left(I_n\right)$. The ANN has one hidden layer and an output layer. Many neurons are concealed was determined to ensure a satisfactory root-mean-squared error while training the network. The neural network's framework is obtainable in Figure 4.

The neural network can recognise 11 different fault types, including those that occur at the grid side, Zone X, or Zone Y (single-phase-to-ground, unbalanced two-phase, and balanced faults). As exposed in figure 2, there are five neurons at the output layer: two for phases (denoted as X, Y), and three for locations (grid, Zone X, or Zone Y). For example, an output [0 1 1 1 0 1 0] implies that an unbalanced two-phase-to-ground (BCG) fault occurs at Zone A. An output [11101 0 0] implies that a balanced three-phase fault occurs at the grid side. An output [0 0 1 1 0 0 1] implies that a single-phase-to-ground (CG) fault occurs at Zone B. The specified zones in a microgrid are very small, and the characteristics of fault voltages and currents are very similar in a zone, which is usually defined by isolation transformers.



International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

Figure 3. Artificial neural networks

The structure of the ANN (e.g., the number of covert layers) is decided generally by heuristics. More hidden layers tend to attain a good fitting nevertheless are most likely to be overfitting. This suggests that the ANN performs poorly on the testing set despite fitting the training set too well. The suggested ANN will be implemented on the microcontroller (Renesas RX62T in this case), which has finite memory, which is the fundamental justification for using just one hidden layer. An inexpensive nonetheless competitive chip is required in industry practice. The proposed ANN was trained by the Levenberg–Marquardt algorithm to minimize the MSE at the output layer by giving training datasets. Therefore, this Taguchi-based ANN can classify the detected faults, and the classified FC are limited by I-SSCB which is demonstrated in the following sub-section, respectively.

D. DC FC Limiting Method

Due to the FC's abrupt shift in amplitude and direction, the network needs to be secured. Protecting the network from these potential faults is a challenging undertaking for the DC FC does not zero-cross. As a result, the DC-DS's effective FC limitation is crucial. Therefore, an I-SSCB with the ability to limit the FC is proposed. This not only enables FC limitation to be achieved rapidly and effectively but also ensures the converter's continued operation and the sound network's ability to ride off faults after a DC fault.

1. Improved Self-Adaptive I-SSCB

Fault Current Limiting (FCL) is working as a series impedance with the DC distribution line. Theoretically, it is considered a normally closed switch with a parallel resistor. It is required to have a high operation speed and automatically reappearance to standard and recovery state after the responsibility permission. Therefore, a suitable FCL circuit with a DC breaker essential has the following characteristics: (a) Fast FC restriction capabilities; (b) Minimal influence on the system's regular operation; (c) High efficiency; (d) Low price and maintenance cost. It may contribute to extending the life of system components, reducing high voltage fluctuation, and obtaining lower mechanical and electrical pressures.

The proposed self-adapt SSCB in this study is suggested for an LV DC-DS with small damping. It is capable of FC restriction for two-way protection applications revealed in figure 3. It will act with the highest speed to maintain safety for sensitive devices and enhance the fast recovery of the whole system. Comparatively, with previous work, the breaker in this study achieved a higher operation speed, efficiency, and configuration. The FCL circuit is capable of efficient self-compatibility during different situations. The energy which is stored in parasitic components will be quenched by a Metal Oxide Varistor (MOV), and due to the clamping characteristics of MOV, the voltage on SSCB clamps to v_o. The maximum current of HSSCB $(i_{\max})$ and voltage on the inductor (v_f) can be achieved by the following equations respectively:

$$I_{\max} = I_f + \frac{v_o - v_{dc}}{F} \tag{16}$$

$$v_f = v_o - v_{dc} \tag{17}$$

Where, I_f and v_{dc} are inductor current and system-rated voltage respectively. The FCL- I-SSCB operation process in this investigation has the following characteristics.

- In a normal situation, for stability and high-efficiency purposes, the FCL circuit will be disconnected automatically and the current will flow through the ultra-fast MB.
- In the incident of a fault, the Fault Current Limiter (FCL) promptly connects to effectively limit the growth and spread of fault current throughout the entire system. This ensures safe operation, isolates the protective devices, and maintains system integrity.
- After the fault permission, the system is rapidly recovering, and safety measures will be in place for the subsequent unforeseen short circuit recurrence.
- For the system's fast recovery purposes and temporary fault situation, FCL will be disconnected.
- The energy which is saved in the inductors and accumulated DC fault energy will be quenched and dissipated by the parallel MOV.

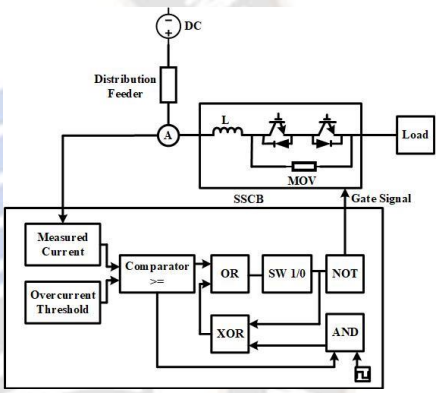


Figure 4. Self-adaptive solid-state circuit breaker

After a DC short circuit occurs in any part of the system, the capacitor of all converters will be discharged along the faulted circuit causing a large current to follow through the short circuit point. Consequently, the sum of the lines' and power electronic converters' discharge current is the DC short circuit current. It is quite significant to distinguish that the scheme parameters calculation, transient feature, and converter types are the most affecting factors during the fault condition. For a DC fault analysis, the type of DC distribution line, system configuration, capacity, feeder length, fault types, and location are the essential topics that should be considered. Due to the direct effect of the fault position and feeder length on the current value, the equivalent fault impedance will not have the same value in a different location. It will affect the rate of current rise and peak value. Thereby, the desired FCL unit for each circuit is required to be arranged by DCCB interrupting current. The restriction current of each FCL branch can be found by the following equation:

$$i_f = \frac{1}{g} + i_k \tag{18}$$

Where i_k is the maximum interrupting the current of the DC breaker, g is the number of discharge circuits in a possible faulted branch and i_k is the desired limiting current of the FCL circuit. The high speed, self-adaptability, high

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

efficiency, fast recovery and multi-short FC limiting make it capable of handling the LV DC distribution during fault situations and giving better system stability. Moreover, the configuration and technology enable it for more flexible and optimized integration of DGs and clean energy sources.

V. Experimentation And Result Discussion

The suggested plan is verified on an LVDCMG modelled in the MATLAB/SIMULINK platform. The system configuration model for simulation is depicted in table 2. The version of Matlab employed for testing and evaluating the proposed method is R2021b. The operating system of the system is Windows 10 Home, and it has a 6GB DDR3 memory capacity. The Matlab processor employed for the simulation is a 3.5GHz Intel Core i5, and the simulation time for the suggested work is 10.190 Seconds, respectively.

TABLE II. Table Of System Configuration For Simulation

Simulation System Configuration	
MATLAB	Version R2021b
Operation System	Windows 10 Home
Memory Capacity	6GB DDR3
Processor	Intel Core i5 @ 3.5GHz
Simulation Time	10.190 Seconds

Figure 5 shows the Simulink model for the suggested low-voltage DCMG. The LVDC network is integrated with a PV with the irradiance of 1000 and 25º as PV temperatures. A maximum power point tracking (MPPT) supervisor is utilized in this grid using the incremental conductance and integral regulator technique. An upconverter is placed in this utility grid, which is employed to convert the solar power to the grid.

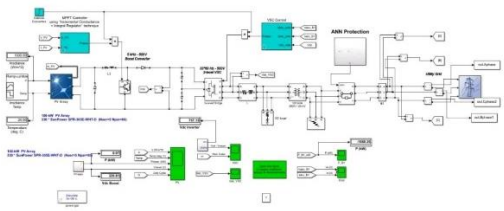


Figure 5. The proposed lvdcmg's simulink model

Then 3 3-level VSC is utilized, which acts as the three-level bridge, also inductance and the VSC control are utilized in this grid. After that, ANN protection is introduced in this scheme, to protect the FC, and it is employed in the DC microgrid. This protection scheme performs detection, classification, and limiting of the FC. Then the power is given to the utility grid. The utility grid consists of output parameters as output A phase, output B phase 1, and output Chase 2, respectively.

TABLE III. Lv-Dcmg System Components And Parameter Specifications

Parameters	**Specifications**
Switching Frequency	5000Hz
Initial Value for Duty	0.5
Cycle	
PV Temperature	25°C
PV Irradiance	1000
Sample Time	100µs
Ts_Power	1µs
Nominal Frequency	60 Hz
Nominal DC Bus Voltage	500 V

Table 3 describes the system components and parameter specifications utilized in the LVDCMG. It describes the switching frequency as 500 Hz, and the initial value of the duty series is 0.5. Then the temperature of PV is 25ºC, and PV Irradiance is 1000. The sample time is denoted as 100µs, and the Ts_Power is 1µs. The nominal frequency is 60 Hz, and the nominal DC bus voltage is 500 V, respectively.

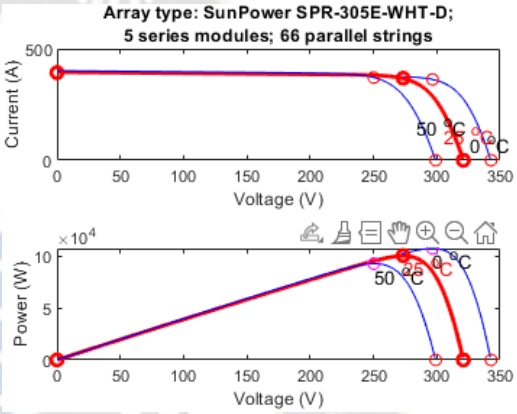


Figure 6. Current and power of pv arrays

Figure 6 describes the current and power of PV arrays, The array type of the PV is Sun Power SPR-305E-WHT-D, 5 series modules, and parallel strings as 66. During the temperature is 25°C, the current of the PV is approximately 400A and the voltage is nearly 325 V, then during the 50°C and 0°C, the voltage is nearly 300 V and 345 V, and the current is approximately 400A. Then the power values for PV at temperatures 25°C, power 100KW, when the temperature is 50°C and 0°C, the power of PV is 95KW and 120KW.

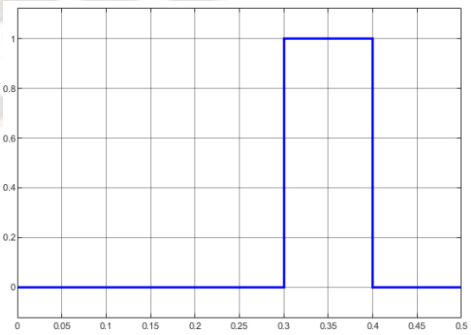


Figure 7. Output current of ann

The proposed ANN's output current, the current value of the suggested ANN produces 0 A when the time reaches up to 0.3 sec as publicized in figure 7. When the reaches 0.3 to 0.4 secs, the current of the proposed work reaches 1 A. Then the

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 September 2023*

current also reaches 0 A, when the time of ANN reaches 0.4 to 0.5 secs, respectively.

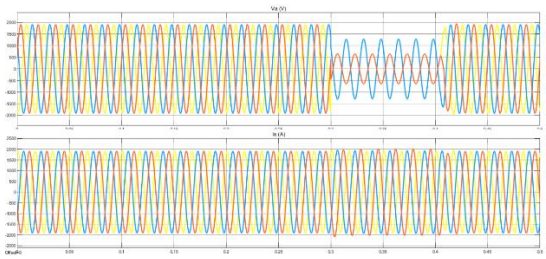


Figure 8. Fault voltage and the fc

The fault voltage and the FC of the proposed microgrid are depicted in figure 8. The fault voltage produced in this proposed work is approximately 1900V, during the time of 0.3 secs. When the time interval is between 0.3 to 0.4 secs, the voltage value is reduced. Then after 0.4 secs, the voltage reaches an actual value of approximately 1900V. Then the FC produced as 1950A when the time is 0.3 secs and the time interval is 0.3 to 0.4 sec, the FC produced by this proposed system is 2 KA, respectively.

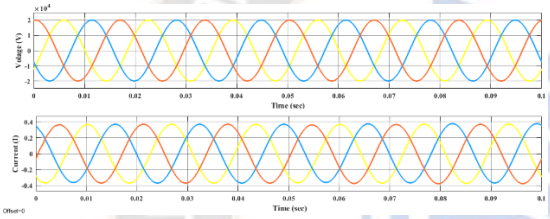


Figure 9. Voltage and current graph for proposed method without faults

The current and voltage levels of the suggested method are exposed in figure 9 without causing any errors. The voltage values for the proposed method without producing faults are 21KV, during the time of 0.1 sec. Consequently, the proposed work's current value is 0.35I, during the time as 0.1 sec, and the offset value is 0.

VI. Research Conclusion

Current expansions in PE and smart grids have persuaded academics that a low voltage DC (LVDC) microgrid is practical and excellent for the next smart grids. High efficiency, easy connecting through PE converters, numerous power sources, and enhanced transmission power capacity are demonstrated by the LVDCMG. As these grids offer a talented explanation for various applications such as shipboards, electrification of remote communities, grids with sensitive loads, and even space exploration, ensuring power quality becomes of utmost importance. In a DCMG, fast fault isolation and detection are also essential. To identify all flaws in the PV-based DCMG, a Field Transform Technique is provided in this paper. Then the detected faults are classified using Taguchi-based ANN, which classifies the detected faults in the MG. The suggested technique usages only energy and current signals close to the static switch. The TM reduces significantly the number of datasets needed to train the fully connected ANN. The suggested technique can successfully classify and locate the faults. After analysing and identifying the MG's flaws, an I-SSCB was introduced to limit the FC. It efficiently protects the DCMG and improves reliability. The suggested approach is tested and evaluated using MATLAB software.

- The current and the power values for the PV array are nearly 400A and 100 KW during the PV temperature of 25°C. The current produces approximately for the temperatures 50°C and 0°C, and the voltage for the PV temperature of 0°C, 25°C, and 50°C are 345 V, 325 V, and 300 V.
- The discharge current of the designed ANN is 0A for below 0.3 secs, and above 0.4 secs, nonetheless, between 0.3 to 0.4 secs, the current produced by this proposed ANN is 1A.
- The fault voltage and FC produced in this proposed work is 1900V for the time interval below 0.3 sec and above 0.4 sec, nevertheless in between it produces less value. Then the FC produced in this work is approximately 1950A during the time as below 0.3 seconds and above 0.4 seconds. In between 0.3 and 0.4 sec, the FC produces 2KA.

For the proposed work, the voltage and present standards are 21 KV and 0.35 I, respectively.

Hence, the proposed model effectively detects, classifies, and limits fault currents. The evaluation indicates that the recommended Taguchi-based ANN) offers superior performance in terms of providing an enhanced protection scheme. In future work, an improved Neural Network or other ML methods will be applied to correspondingly increase the effectiveness of the protective scheme.

References

[1] E.N. Prasad, and P.K. Dash, "Fault analysis in photovoltaic generation-based DC microgrid using multifractal detrended fluctuation analysis," International Transactions on Electrical Energy Systems, vol. 31, no. 1, pp. e12564, 2021.
[2] S. Augustine, M.J. Reno, S.M. Brahma, and O. Lavrova, "Fault current control and protection in a standalone DC microgrid using adaptive droop and current derivative," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 3, pp. 2529-2539, 2020.
[3] J. Naik, S. Dhar, and P.K. Dash, "Adaptive differential relay coordination for PV DC microgrid using a new kernel-based time-frequency transform," International Journal of Electrical Power & Energy Systems, vol. 106, pp.56-67, 2019.
[4] I. Grcić, H. Pandžić, and D. Novosel, "Fault Detection in DC Microgrids Using Short-Time Fourier Transform," Energies, vol. 14, no. 2, pp. 277.
[5] M. Shamsoddini, B. Vahidi, R. Razani, and Y.A.R.I. Mohamed, "A novel protection scheme for low voltage DC microgrid using inductance estimation," International Journal of Electrical Power & Energy Systems, vol. 120, pp.105992, 2020.
[6] M.R.K. Rachi, M.A. Khan, and I. Husain, "Current Derivative Assisted Protection Coordination System for Faster Fault Isolation in A Radial DC Microgrid," In 2020 IEEE Energy Conversion Congress and Exposition (ECCE) IEEE, pp. 292-1298, October 2020.
[7] D.K.J.S. Jayamaha, N.W.A. Lidula, and A.D. Rajapakse, "Wavelet-multi resolution analysis based ANN architecture for fault detection and localization in DC microgrids," IEEE Access, vol. 7, pp.145371-145384, 2019.
[8] N. Yadav, and N.R. Tummuru, "A real-time resistance based fault detection technique for zonal type low-voltage dc microgrid applications," IEEE Transactions on Industry Applications, vol. 56, no. 6, pp. 6815-6824, 2020.
[9] A. Abdali, K. Mazlumi, and R. Noroozian, "High-speed fault detection and location in DC microgrids systems using Multi-Criterion System and neural network," Applied Soft Computing, vol. 79, pp. 341-353, 2019.

[10] O.Y. Reddy, S. Chatterjee, A.K. Chakraborty, and A.R. Bhowmik, "Fault detection and location estimation for LVDC microgrid using self-parametric measurements," International Transactions on Electrical Energy Systems, vol. 30, no. 9, pp. e12499, 2020.
[11] S. Dhar, R.K. Patnaik, and P.K. Dash, "Fault detection and location of photovoltaic based DC microgrid using differential protection strategy," IEEE Transactions on Smart Grid, vol. 9, no. 5, pp. 4303-4312, 2017.
[12] A. Meghwani, S.C. Srivastava, and S. Chakrabarti, "Local measurement-based technique for estimating fault location in multi-source DC microgrids," IET Generation, Transmission & Distribution, vol. 12, no. 13, pp. 3305-3313, 2018.
[13] J.Q. James, Y. Hou, A.Y. Lam, and V.O. Li, "Intelligent fault detection scheme for microgrids with wavelet-based deep neural networks," IEEE Transactions on Smart Grid, vol. 10, no. 2, pp. 1694-1703, 2017.
[14] L. Kong, and H. Nian, "Parameters Selection Method of Circuit Breaker and Fault Current Limiter in Mesh-Type DC Microgrid," IEEE Access, vol. 9, pp. 35514-35523, 2021.
[15] N.K. Sharma, S.R. Samantaray, and C.N. Bhende, "VMD-Enabled Current-Based Fast Fault Detection Scheme for DC Microgrid," IEEE Systems Journal, 2021.
[16] N. Yadav, and T.N. Reddy, "Short-Circuit Fault Detection and Isolation Using Filter Capacitor Current Signature in Low-Voltage DC Microgrid Applications," IEEE Transactions on Industrial Electronics, 2021.
[17] Y. Yang, C. Huang, D. Zhou, and Y. Li, "Fault detection and location in multi-terminal DC microgrid based on local measurement," Electric Power Systems Research, vol. 194, pp.107047, 2021.
[18] K.A. Saleh, A. Hooshyar, and E.F. El-Saadany, "Ultra-high-speed traveling-wave-based protection scheme for medium-voltage DC microgrids," IEEE Transactions on Smart Grid, vol. 10, no. 2, pp. 1440-1451, 2017.
[19] K. Subramaniam, and M.S. Illindala, "Intelligent Three Tie Contactor Switch Unit-Based Fault Detection and Isolation in DC Microgrids," IEEE Transactions on Industry Applications, vol. 56, no. 1, pp. 95-105, 2019.
[20] T. Wang, and A. Monti, "Fault detection and isolation in DC microgrids based on singularity detection in the second derivative of local current measurement," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020.
[21] R.K. Chauhan, and K. Chauhan, "Smart protection system for identification and localisation of faults in multi-terminal DC microgrid," IET Smart Grid, vol. 3, no. 6, pp. 882-889, 2020.
[22] O.A. Gashteroodkhani, M. Majidi, M.S. Fadali, M. Etezadi-Amoli, and E. Maali-Amiri, "A protection scheme for microgrids using time-time matrix z-score vector," International Journal of Electrical Power & Energy Systems, vol. 110, pp. 400-410, 2019.
[23] M. Salehi, S.A. Taher, I. Sadeghkhani, and M. Shahidehpour, "A poverty severity index-based protection strategy for ring-bus low-voltage DC microgrids," IEEE Transactions on Smart Grid, vol. 10, no. 6, pp. 6860-6869, 2019.
[24] R. Montoya, B.P. Poudel, A. Bidram, and M.J. Reno, "DC microgrid fault detection using multiresolution analysis of traveling waves," International Journal of Electrical Power & Energy Systems, vol. 135, pp.107590, 2022.
[25] M. Shamsoddini, B. Vahidi, R. Razani, and H. Nafisi, "Extending protection selectivity in low voltage DC microgrids using compensation gain and artificial line inductance," Electric Power Systems Research, vol. 188, pp.106530, 2020.
[26] Y.Y. Hong and M.T.A.M. Cabatac, "Fault Detection, Classification, and Location by Static Switch in Microgrids Using Wavelet Transform and Taguchi-Based Artificial Neural Network," in IEEE Systems Journal, vol. 14, no. 2, pp. 2725-2735, June 2020.
[27] Mohammad Aman Yaqobi, Hidehito Matayoshi, Natarajan Prabaharan, Hiroshi Takahashi, M. Ashraf Hemeida, Senjyu Tomonobu, "Interconnected standalone DC microgrid fault protection based on Self-Adaptive DC fault current limiter with hybrid solid state circuit breaker," AIMS Energy, vol. 9, no. 5, pp. 991-1008, 2021.
[28] H.R. Ahmadi, N. Mahdavi, and M. Bayat, "A novel damage identification method based on short-time Fourier transform and a new efficient index. In Structures Elsevier, vol. 33, pp. 3605-3614, October 2021.
[29] A.K. Sahoo, S.K. Mishra, "Analytical fopid controller design based on bode's ideal transfer function for desired closed loop response," Journal of Advanced Research in Dynamical and Control Systems. Vol. 12, pp. 9–20, 2020. https://doi.org/10.5373/JARDCS/V12I5/20201683
[30] A.K. Sahoo, S.K. Mishra, "Design of Sliding Mode Controller using artificial delay," In: Proceedings of 2014 IEEE International Conference on Advanced Communication, Control and Computing Technologies, ICACCCT 2014, 2015.
[31] A.K. Sahoo, S.K. Mishra, D.S. Acharya, S. Chakraborty, S.K. Swain, "A comparative evaluation of a set of bio-inspired optimization algorithms for design of two-DOF robust FO-PID controller for magnetic levitation plant," Electr. Eng., 2023. https://doi.org/10.1007/s00202-023-01867-7
[32] S.A. Qadeer, M.Y.N.S. Khan, et al., "High resolution fuel indicating and tracking system," Microsyst Technol, vol. 25, pp. 2267–2271, 2019. https://doi.org/10.1007/s00542-018-4107-8
[33] G. K. Mahato, B. K. Mahatha and S. Samal, "Melting Heat Transfer on Magnetohydrodynamic (MHD) Flow of a Heat Radiating and Chemically Reacting Nano-Fluid past a Stretchable Surface," JP Journal of Heat and Mass Transfer, vol. 17, no. 2, pp. 379-398, 2019, 0973-5763. http://dx.doi.org/10.17654/HM017020379
[34] Tarun Kumar Kotteda, Manoj Kumar, Pramod Kumar, Rama Bhadri Raju Chekuri, "Metal matrix nanocomposites: future scope in the fabrication and machining techniques," The International Journal of Advanced Manufacturing Technology, 2022. https://doi.org/10.1007/s00170-022-09847-0
[35] Tarun Kumar Kotteda, Rama Bhadri Raju Chekuri, Naga Raju, Prasada Raju Kantheti, S. Balakumar, "Analysis on Emissions and Performance of Ceramic Coated Diesel Engine Fueled with Novel Blends Using Artificial Intelligence," Advances in Materials Science and Engineering, 2021. https://doi.org/10.1155/2021/7954488