International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
***Article Received:** 05 July 2023 **Revised:** 25 August 2023 **Accepted:** 15 September 2023*

Self-Clocked Shift Registers Utilizing 90 nm CMOS: Design, Analysis and Insights

[1] Jami Venkata Suman, [2] Eppili Jaya, [3] Venkataramana Guntreddi, [4] Swethapriya Aenikapati, [5] Kamatchi S, [6] Enerst Edozie

[1]Assistant Professor, Department of ECE, GMR Institute of Technology, Rajam, Andhra Pradesh, India
Corresponding Author: venkatasuman.j@gmrit.edu.in
[2]Assistant Professor, Department of ECE, Aditya Institute of Technology and Management, Tekkali, Andhra Pradesh, India
jaya.baratam@gmail.com
[3]Associate Professor, Department of ETCE, School of Engineering and Applied Sciences, Kampala International University, Uganda
gvramana@kiu.ac.ug
[4] PhD Student, Department of ECE, Amrita School of Engineering, Bangalore, Amrita Vishwa Vidhyapeetham, India
a_swetha@blr.amrita.edu
[5]Assistant Professor Selection Grade, Department of ECE, Amrita School of Engineering, Bangalore, Amrita Vishwa Vidhyapeetham, India
s_kamatchi@blr.amrita.edu
[6]Assistant Lecturer, Department of ETCE, School of Engineering and Applied Sciences, Kampala International University, Uganda
enerst.edozie@kiu.ac.ug

Abstract—This paper presents an efficient approach to designing and analyzing four bit shift register utilizing self-clocked D flip-flops as integral storage components. The use of internal clock generation within these flip-flops obviates the need for external clock synchronization. These specially designed flip-flops incorporate a reduced number of transistors in comparison to conventional designs, leading to notable enhancements in power efficiency, packaging density, and operational speed. The implementation of self-triggered D flip-flops facilitates the creation of various shift register configurations, including Serial in Serial out (SISO), Serial in Parallel out (SIPO), Parallel in Serial out (PISO), and Parallel in Parallel out (PIPO). These registers not only occupy a smaller die area but also exhibit diminished power consumption and heightened operational speed when contrasted with standard counterparts. The design and simulation procedures are executed using the Microwind tool and a 90 nm CMOS technology.

Keywords- Die area, self-clocked, CMOS, shift registers, power consumption.

I. INTRODUCTION

A register serves as a cohesive assembly of flip-flops with the primary purpose of collectively housing binary data. This collective entity finds its significance in various digital applications where the storage and manipulation of data are fundamental. Within this conceptual framework, it's crucial to grasp the essence of each individual flip-flop as a microscopic data container, capable of holding a solitary binary digit. By extrapolation, envisioning an n-bit register reveals a congregation of n of these flip-flops, harmonizing their efforts to accommodate and retain n discrete bits of data.

The landscape of registers gains depth through a dualistic classification: one that segregates them into two principal archetypes – buffer/storage registers and shift registers. Both of these incarnations share the core essence of data preservation, yet they diverge significantly in their operational nuances. Delving into the realm of buffer/storage registers, their cardinal function revolves around the safekeeping of data for deferred utilization. These registers lay the groundwork for efficient data management, facilitating the retrieval of information when the need arises.

On the flip side, shift registers emerge as an enthralling variant, imbued with the remarkable capability of not only safeguarding data but also orchestrating intricate manipulations of binary data via well-defined shifting operations. The architectural blueprint of shift registers unveils a symphony of interconnected flip-flops, meticulously arranged in a cascading sequence. This sequential arrangement is underpinned by a pivotal element – a shared clock signal, a metronomic heartbeat crucial for orchestrating the synchronous rhythm of the cascaded flip-flops. This synchronized choreography of clock-driven flip-flops constitutes the bedrock upon which the precision and efficacy of the shifting processes are crafted [1-3].

In this juncture, the crux of the matter pivots to the pivotal contribution offered by a scholarly paper, where innovation thrives and blooms. This scholarly gem propounds a trailblazing methodology for the design of shift registers. The kernel of this methodology lies in an ingenious pivot – the integration and harnessing of self-triggered flip-

flops. This innovation marks a departure from conventional paradigms, ushering in an era of enhanced efficiency and optimized performance in the realm of shift register design.

The very essence of a self-triggered flip-flop hinges on autonomy, rendering it distinct from its conventional counterparts. Conventional flip-flops are beholden to external clock signals for orchestrating their sequential transitions and operations. In stark contrast, the self-triggered flip-flops inculcate a degree of self-sufficiency, triggering their internal state transitions without an external clock's imperative. This autonomy, this liberation from the shackles of external synchrony, bestows upon these flip-flops a unique prowess the ability to operate seamlessly in scenarios where conventional clocking mechanisms might falter or waver.

The impact of this innovative design methodology reverberates across multiple dimensions. Efficiency, a paramount attribute in modern digital systems, receives a shot in the arm. The self-triggered flip-flops, by virtue of their self-contained triggering mechanisms, minimize the extraneous overhead introduced by conventional clocking schemes. This leaner overhead translates into swifter operations and an economy of resources, both of which collectively bolster the efficiency quotient.

Moreover, this novel approach unfurls a tapestry of opportunities for novel designs, each woven with threads of innovation and pragmatism. The canvas of digital design becomes broader and more expansive, beckoning designers to paint strokes of creativity unburdened by the limitations of yore. Concepts that once danced at the periphery of feasibility now pirouette center stage, enabled by the versatility of self-triggered flip-flops.

In essence, the crux of this paper's contribution rests not solely in the realm of digital design and technological advancement. It resonates as a harmonious chord with broader implications, echoing through the corridors of efficient resource utilization, enhanced design paradigms, and a symphony of possibilities previously untapped. The marriage of self-triggered flip-flops with the orchestration of shift registers constitutes a harmonious duet, a testament to the ever-evolving symphony of digital innovation. As this composition takes center stage, its echoes are bound to resonate across the digital landscape, ushering in an era where efficiency and creativity dance hand in hand [4-5].

The article presents an integrated hybrid low-dropout regulator (HLDO) with minimal dropout and improved transient response. It combines analog and digital LDOs through a residue-current-locked loop (RLL) for joint regulation, addressing quantization errors and enhancing power supply rejection. The prototype, using a 65-nm CMOS process, achieves remarkable load regulation and transient performance. The study introduces a self-clocked digital low-dropout regulator (SC-DLDO) with bidirectional shift registers, enhancing load transient response and efficiency in SoC power management. Achieved in a 65-nm CMOS process, the design showcases minimal dropout and rapid transient behavior [6-7].

Memristors offer an alternative to address CMOS scaling limitations. This paper suggests efficient memristor-only and hybrid CMOS/memristor shift registers, displaying superior speed, area, and power advantages over traditional designs. This study introduces an amorphous silicon thin-film transistor (a-Si TFT) high-voltage serial-in-parallel-out (SIPO) shift register, demonstrated through simulation and experimentation, with potential use in digital microfluidics at 20 kHz clock frequency. Utilizing cross-join pairs and Zech's logarithms, this paper derives nonlinear from linear feedback shift register feedback functions, enabling de Bruijn sequence generation [8-10].

A. Research Gaps

Shift registers play a fundamental role in digital systems. However, their dependence on external clock synchronization constrains their ability to fulfill modern needs. This synchronization not only adds complexity to design and implementation but also hinders progress in power efficiency, size reduction, and operational speed. Existing research has not sufficiently delved into incorporating self-clocked D flip-flops as essential storage components in shift registers, leaving the potential benefits of this approach largely unexplored.

B. Problem Statement

Contemporary digital systems necessitate efficient shift registers for tasks involving data storage, retrieval, and manipulation. However, conventional designs dependent on external clock signals to manage data shifting present integration, power consumption, packaging density, and operational speed challenges. These constraints are particularly pronounced in the context of escalating demands for compact, high-performance electronic devices.

C. Objectives

- The primary objective is to develop a novel approach that employs self-clocked D flip-flops as the building blocks of shift registers. By eliminating the need for external clock synchronization, this approach aims to simplify the design process and improve overall system performance.
- Conventional shift register designs often involve a high number of transistors, contributing to increased power consumption and limiting operational speed. The objective is to explore how self-clocked D flip-flops can incorporate fewer transistors compared to traditional

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
Article Received: *05 July 2023* ***Revised:*** *25 August 2023* ***Accepted:*** *15 September 2023*

designs, leading to enhanced power efficiency, higher operational speed, and improved packaging density.

- Investigate the versatility of the proposed self-clocked approach by exploring various shift register configurations, including Serial in Serial out (SISO), Serial in Parallel out (SIPO), Parallel in Serial out (PISO), and Parallel in Parallel out (PIPO). Determine the feasibility and advantages of these configurations in terms of performance and integration.
- Evaluate the proposed self-clocked shift register designs against their conventional counterparts. Analyze key metrics such as die area, power consumption, and operational speed to quantify the advantages of the new approach.
- Utilize the Micro wind tool and a 90 nm CMOS technology to design, simulate, and validate the performance of the proposed self-clocked shift register configurations. Ensure that the theoretical advantages translate into practical benefits under real-world conditions.

II. SELF TRIGGERED FLIP-FLOP

At the heart of shift registers lies a fundamental building block called flip-flops. Within this context, we introduce a novel method for designing shift registers by integrating self-edge-triggered flip-flops, which were initially proposed in reference. The self-edge-triggered flip-flop combines the features of a positive edge-triggered latch and a comparator, presenting a fresh approach to shift register architecture. This flip-flop's CMOS realization is depicted in Figure 3. Remarkably, the distinguishing feature of the self-triggered flip-flop is its capability to operate without relying on external clock pulses for synchronization, as it generates an internal clock signal for its triggering mechanism [11-12].

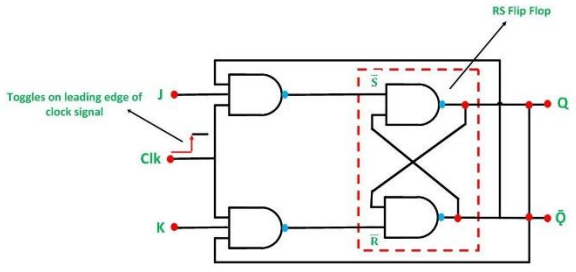

Figure 1. Autonomously Activated Flip-Flop Circuit

The setup comprises a level-triggered latch in conjunction with a comparator. The role of the comparator is to offer feedback control for the flip-flop. This setup takes advantage of the behavior of the D latch, which alters its state with a positive clock pulse only when there's a difference between the data input D and the latch output Q. On the other hand, if they are equal, the output remains unaltered. By utilizing this principle, instances where there are disparities between the data D and the output Q can be detected. This is achieved through the scrutiny of the current input against the prevailing output by a comparator. As a result, the comparator produces an output of 1 when there are distinct logical values between the data D and the output Q, and it generates 0 during all other occurrences [13].

The output of the comparator serves as a clock signal for the latch. The minimal delay in the transmission between the latch's input and output leads to a narrow pulse width for this clock signal. This pulse is available during both the ascent and descent of the data signals. The frequency of this clock signal varies based on the input data rate, rising as the data rates increase and decreasing as they decrease.

III. SERIAL SHIFT REGISTERS

A shift register falls under the classification of registers where data is shifted or transferred from one flip-flop to another. It performs a dual function of storing data and enabling data transfer. The operational dynamics of the shift register are dictated by how input is supplied and output is retrieved [14-15].

Shift registers are categorized into four groups according to:

1. Serial Input Serial Output Shift Register.
2. Serial Input Parallel Output Shift Register.
3. Parallel Input Serial Output Shift Register.
4. Parallel Input Parallel Output Shift Register.

The construction of a Serial in Serial out (SISO) shift register involves connecting of 4 flip-flops in a consecutive configuration, where the output of each flip-flop is linked to inputs of the subsequent flip-flop. It receives data in a serial fashion and the output is obtained serially from the last flip-flop's output [16-18]. The schematic structure depicting the SISO shift register is presented in Figure 2.

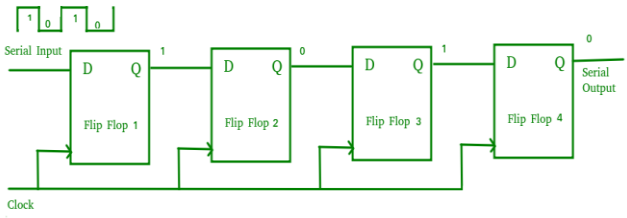

Figure 2. Single-Input Single-Output Shift Register

Operating in a serial input mode, the Serial In Parallel Out shift register sequentially receives data and generates a 4-bit output at each flip-flop. The arrangement of the SIPO shift register is visually depicted in Figure 3.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
Article Received: *05 July 2023* ***Revised:*** *25 August 2023* ***Accepted:*** *15 September 2023*

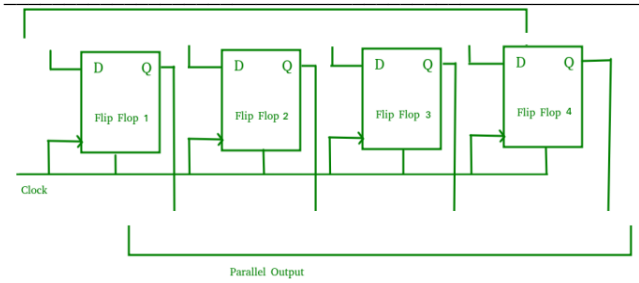

Figure 3. Single-Input Parallel-Output Shift Register

Within the Parallel in Serial out (PISO) shift register, input data bits are concurrently loaded into the input of individual flip-flops, with the output materializing at the final flip-flop's output. To execute loading and shifting operations as needed, a multiplexer is frequently employed. The schematic diagram depicting the configuration of the parallel in serial out shift register is displayed in Figure 4.

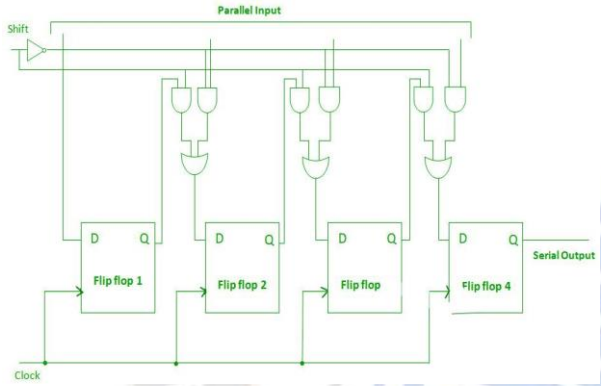

Figure 4. Parallel-Input Single-Output Shift Register

Functioning in a parallel input and output mode, parallel-in parallel-out (PIPO) shift registers concurrently feed input data bits to individual flip-flop inputs, resulting in parallel outputs synchronized by each clock pulse. Figure 5 offers a visual illustration of the PIPO configuration.

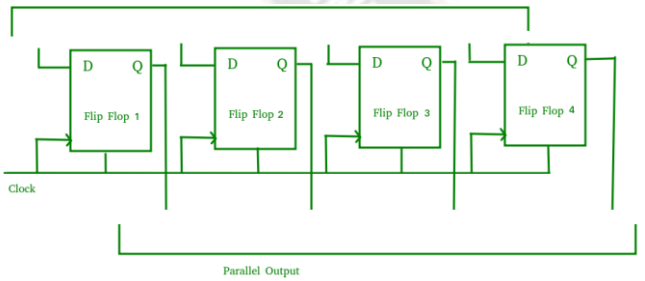

Figure 5. Parallel-Input Parallel-Output Shift Register

Shift registers have wide-ranging applications spanning various domains of digital logic. One of their primary roles is to act as converters bridging the gap between serial and parallel interfaces. Moreover, they serve as pulse extenders and are integral to the execution of shift instructions in microprocessors and microcontrollers. In the past, a substantial number of SISO shift registers found application as memory delay lines. Furthermore, these shift registers function as time delay components and sequencing elements. The duration of the delay relies on the shift register's stages and the clock frequency. These versatile components can manifest in various forms such as random pattern generators, ring counters, and Johnson counters [19-20].

IV. SIMULATION RESULTS

This paper introduces a proposition for designing and analyzing shift registers employing self-triggered flip-flops as put forth. The arrangement is created employing the backend design and simulation tool MICROWIND, utilizing a supply voltage of 1.20 volts and operating at a temperature of 27°C. The SISO shift register's layout is illustrated in Figure 6.

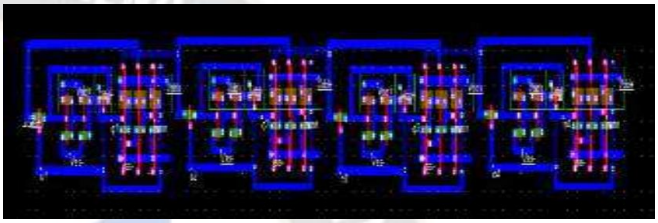

Figure 6. Arrangement of Single-Input Single-Output Shift Register

Figure 7 displays the simulation outcome of a 4-bit Serial In Serial Out shift register (SISO). The simulation of the SISO configuration is conducted employing 90nm CMOS technology, utilizing a step size of 0.09 picoseconds and a time scale of 50 ns.

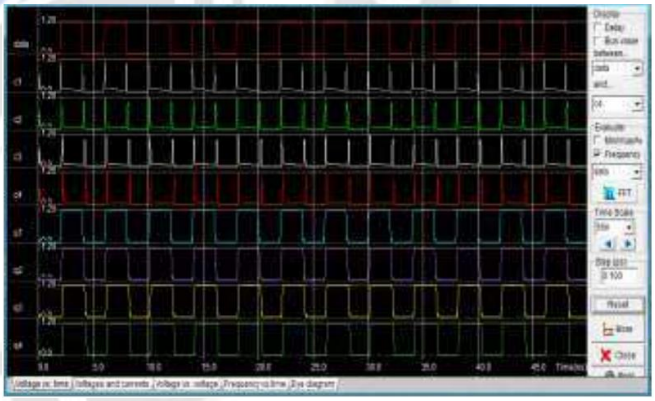

Figure 7. Outcome of Simulations for Single-Input Single-Output Configuration

The simulation takes place at a data frequency of 0.25 GHz, where the propagation delay between input and output is recorded at 255 picoseconds, along with an average power consumption of 109 microwatts. Moving on to the next configuration, we encounter the SIPO shift register. The graphical depiction of the SIPO layout is revealed in Figure 8. This layout is intricately designed to adhere to the specifications of 90nm CMOS technology. The process entails employing a precise step size of 0.09 picoseconds and an established time scale of 52 nanoseconds.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 9
Article Received: *05 July 2023* ***Revised:*** *25 August 2023* ***Accepted:*** *15 September 2023*

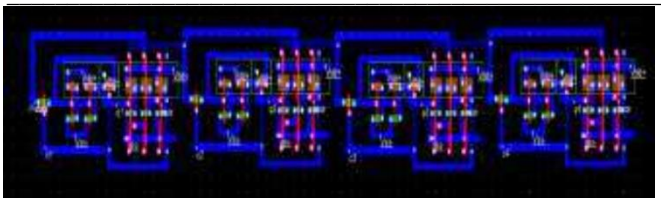

Figure 8. Arrangement of Single-Input Parallel-Output Shift Register

The provided configuration undergoes simulation through the employment of the Micro Wind simulation tool. The input data rate is established at 0.49 GHz, yielding an average power consumption of 181 microwatts. The graphical representation of simulation outcomes for the SIPO shift register is depicted in Figure 9.

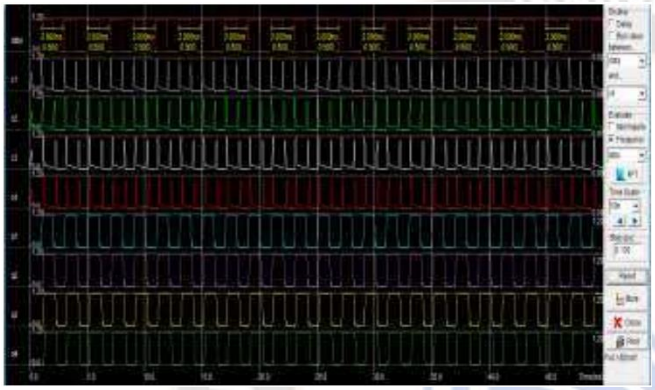

Figure 9. Simulation Outcomes for Single-Input Parallel-Output Shift Register

The following shift register variant is the Parallel In Serial Out (PISO) type, which accepts a parallel 4-bit data input and generates a serial output. The layout showcasing the PISO configuration can be observed in Figure 10.

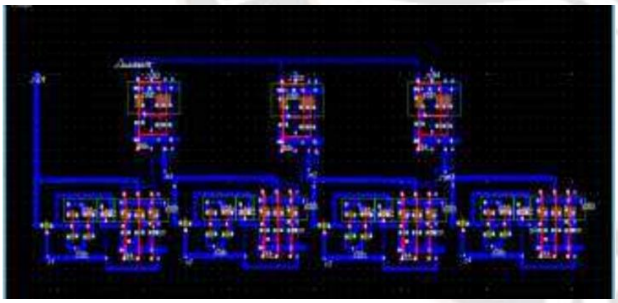

Figure 10. Configuration of Parallel-Input Single-Output Shift Register

Figure 11 presents the visual representation of the simulation results for the PISO shift register. The gathered simulation data unveils that the shift register consumes a total of 155 microwatts of power throughout a simulation period spanning 50 nanoseconds, utilizing a step size of 0.1 picoseconds.

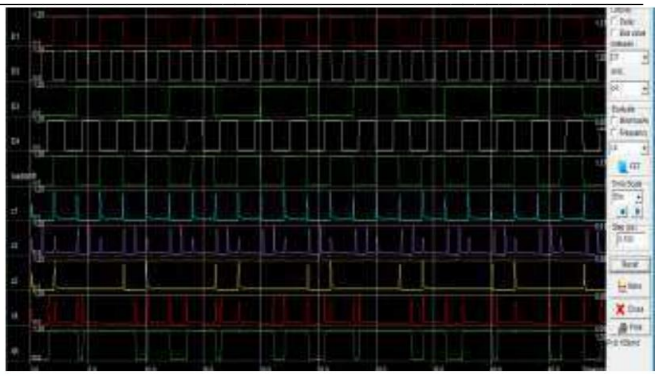

Figure 11. Simulation Findings for Parallel-Input Single-Output Shift Register

Figure 12 illustrates the CMOS layout showcasing the PIPO configuration, enabling simultaneous parallel input reception and output generation.

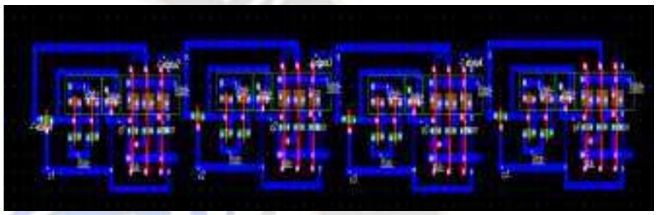

Figure 12. Design of Parallel-Input Single-Output Shift Register

The PIPO shift register undergoes simulation utilizing the Microwind tool, adhering to optimal standards. The simulation outcome, displayed in Figure 13, showcases the operational characteristics of the PIPO shift register.

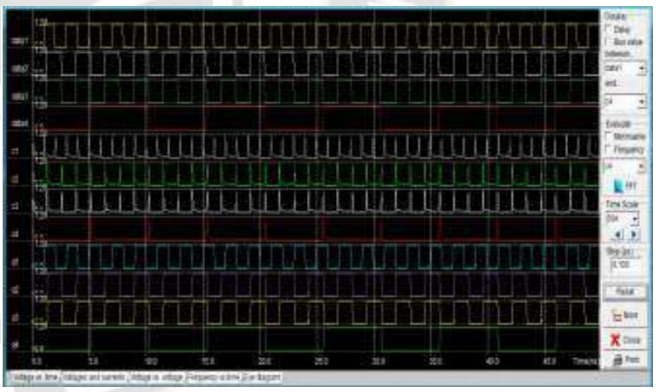

Figure 13. Configuration of Parallel-Input Parallel-Output Shift Register

The simulation outcomes provided elucidate that the circuit exhibits an average power consumption of 123 microwatts during a 50-nanosecond simulation interval, employing a step size of 0.1 picoseconds.

V. CONCLUSION

This research paper introduces an advanced shift register design that capitalizes on the capabilities of self-triggered flip-flops. The simulation is carried out within the Microwind software environment, employing 90nm CMOS technology. This innovative flip-flop design combines the advantages of

self-edge-triggered and double-edge-triggered flip-flops, as explained in reference. The analysis demonstrates the feasibility of constructing all shift register variations using this innovative self-triggered approach. Importantly, this design operates without the need for an external clock pulse, resulting in reduced power consumption compared to conventional methods. This provides evidence for the enhanced performance of the shift register using self-triggered flip-flops, demonstrating improvements in compactness, speed, and energy efficiency in comparison to traditional designs.

REFERENCES

[1] U. K. N. Ekkurthi, V. Dasari, J. Akiri and C. -C. Wang, "A 100 MHz 9.14-mW 8-Bit Shift Register Using Double-Edge Triggered Flip-Flop, "IEEE International Symposium on Circuits and Systems, Daegu, Korea, 2021, pp. 1-4.

[2] L. R. Thoutam, D. Alekya, C. C. Triveni, S. Shruthi, K. Varun and J. Ajayan, "Design and Analysis of Low-Power High Performance 4-Bit Parallel Shift Register using Retentive True Single Phase Clocked D-Flip Flop," IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience and Nanotechnology, Kottayam, India, 2022, pp. 1-5.

[3] L. Subha and A. Surya, "Low power conventional universal shift register using 4: 1 multiplexer, "International Conference on Innovative Research in Electrical Sciences, Nagapattinam, India, 2017, pp. 1-5.

[4] A. Rajaram, P. Premalatha, R. Sowmiya, S. Saravanan and R. Vijaysai, "Design and analysis of high speed shift register using Single clock pulse method," International Conference on Computer Communication and Informatics, Coimbatore, India, 2013, pp. 1-4.

[5] S. E. Razavi, J. Royaei and M. Bahadorzadeh, "Design a low current and high speed shift register based on D type flip flop," International Conference on e-Technologies and Networks for Development, Lodz, Poland, 2015, pp. 1-4.

[6] Y. -H. Hwang, J. Oh, W. -S. Choi, D. -K. Jeong and J. -E. Park, "A Residue-Current-Locked Hybrid Low-Dropout Regulator Supporting Ultralow Dropout of Sub-50 mV With Fast Settling Time Below 10 ns," in IEEE Journal of Solid-State Circuits, vol. 57, no. 7, July 2022, pp. 2236-2249, doi: 10.1109/JSSC.2021.3128815.

[7] M. A. Akram, W. Hong and I. -C. Hwang, "Capacitorless Self-Clocked All-Digital Low-Dropout Regulator," IEEE Journal of Solid-State Circuits, vol. 54, no. 1, 2019, pp. 266-276, doi: 10.1109/JSSC.2018.2871039.

[8] A. Sasi, M. Ahmadi and A. Ahmadi, "Low Power Memristor-Based Shift Register Design," IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, UK, 2020, pp. 1-4, doi: 10.1109/ICECS49266.2020.9294907.

[9] Y. Wei, D. Wang, S. Jiang, H. Ma and J. Yu, "A High-Voltage Serial-In-Parallel-Out Shift Register With Amorphous Silicon TFTs," in IEEE Journal of the Electron Devices Society, vol. 11, 2023, pp. 416-420, doi: 10.1109/JEDS.2023.3293232.

[10] J. Szmidt, "Nonlinear Feedback Shift Registers and Zech's Logarithms," 2019 International Conference on Military Communications and Information Systems (ICMCIS), Budva, Montenegro, 2019, pp. 1-4, doi: 10.1109/ICMCIS.2019.8842713.

[11] Y. Ohkawa and Y. Miura, "Dual Edge Triggered Flip-Flops for Noise Blocking and Application to Signal Delay Detection," IEEE Asian Test Symposium, Niigata, Japan, 2012, pp. 119-124.

[12] C. -C. Yu and K. -T. Chen, "A novel design of low power double edge-triggered flip-flop," International Conference on Bio Medical Engineering and Informatics, Chongqing, China, 2012, pp. 1363-1366.

[13] M. A. Sobhan Bhuiyan, A. Mahmoudbeik, T. I. Badal, M. Bin Ibne Reaz and L. F. Rahman, "Low power D flip-flop serial in/parallel out based shift register," International Conference on Advances in Electrical, Electronic and Systems Engineering, Putrajaya, Malaysia, 2016, pp. 180-184.

[14] A. C. Katageri, B. G. Sheeparamatti and V. B. Math, "Design of MEMS based 4-bit shift register," International Conference on Smart Structures and Systems, Chennai, India, 2014, pp. 103-107.

[15] R. R. Chavhan and R. Thakare, "Implementation of shift register using pulsed latches," International Conference on Innovations in Information, Embedded and Communication Systems, Coimbatore, India, 2017, pp. 1-5.

[16] H. Tanaka and Y. Tadokoro, "Shift Register with Coupled Bidirectional Bifurcation Amplifiers," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 3, 2022, pp. 1712-1716.

[17] S. Sengupta and A. Dastidar, "Evaluation of the performance metrics of a 4 bit universal shift register and its implementation in an arithmetic & logic unit," International Conference on Smart Technologies for Smart Nation, Bengaluru, India, 2017, pp. 1576-1579.

[18] Byung-Do Yang, "Low-Power and Area-Efficient Shift Register using Pulsed Latches", IEEE Transactions on Circuits and Systems-I, vol. 62, no. 6, 2015, pp. 1564-1571.

[19] Jami Venkata Suman, P Jyothi, A Vaani and YR Sekhar, "Design of Low Power and Area Efficient Hybrid Linear Feedback Shift Register", Journal of Critical Reviews, vol. 7, no. 11, 2020, pp. 2333-2345.

[20] P. Ghose, M. N. Rahman, M. M. Alam Polash and U. K. Acharjee, "Design of Reversible Shift Registers Minimizing Number of Gates, Constant Inputs and Garbage Outputs," International Conference on Advances in Computing, Communications and Informatics, Bangalore, India, 2018, pp. 752-758.