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A Novel Architecture of ADPLL Using Cordic Algorithm for Low-Frequency Application

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Abstract—All Digital Phase Locked Loop (ADPLL) has many applications in digital communication. It is difficult for low-frequency applications to achieve the lock state quickly. Therefore, proposed a novel particle swarm based ADPLL (PS-ADPLL) with Coordinate Rotation Digital Computer (CORDIC) algorithm to attain the lock state of the ADPLL for the low-frequency applications. In the proposed architecture, the D flip-flop matches the frequency and the phase of the output and reference pulses and produces an error signals up and down signal. The up/down counter removes the higher frequency part and produces a carry and the borrow signal. These carry and borrow signals are then fed into the increment decrement counters to produce the output signal matching the frequency of the reference signal. However, the time delay is increased for low-frequency applications, which is critical for the lock state. So, the delay line length is calculated by the CORDIC algorithm and is optimized by the particle swarm activated in the phase detector to match the output pulse with the reference pulse and make ADPLL into a locked state. The presented PS-ADPLL is tested in FPGA. Furthermore, the performance parameters are evaluated and compared with other current techniques to calculate the improvement score.

Index Terms—All digital phase locked loop, Coordinate rotation digital computer algorithm, Delay line, Low-frequency application, Particle swarm optimization

I. INTRODUCTION

In the past years, the Phase Locked Loop (PLL) has become the widest technique for stability and frequency generation. ADPLL is one of the PLL's designs, but its component's nature is fully digital [1]. It is used for advanced communication systems like demodulators, modulators, synthesizers and frequency generators, carrier clocks and recovery [2]. It spread rapidly among the researchers due to the advantage of minimum power consumption, effective phase error, minimal cost and small chip area [3]. ADPLL generates the output signal in which the frequency and phase are matched to the input signal. ADPLL lock step is that the output and input signal frequencies and phases remain the same [4]. It is a vital device that perfectly works on the control loops to track the voltage phase [5]. The main problem with the ADPLL is poor versatility and narrow lock range. Most ADPLL is application-oriented designs that respond only for specific ranges of certain application frequencies [6]. The basic design of the ADPLL is given in Fig. 1. Generally**,** the ADPLL is composed of three modules: Phase Detector (PD), Loop Filter (LP) and Digital Controlled Oscillator (DCO) [7]. The phase error signals are computed by PD, and the LF eliminates the error and produces the control reference for DCO [8].

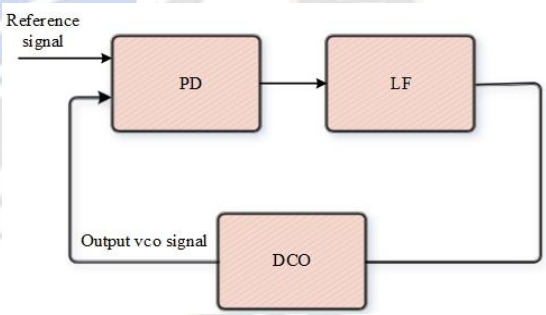

Fig. 1. Basic ADPLL architecture.

The first generated digital radio frequency processor was ADPLL, implemented on a Bluetooth radio that is fully compliant on a single chip [9]. The ADPLL efficiency depends on certain parameters such as used components, power consumption, frequency resolution, locking speed and jitter performance [10]. The ADPLL works at the availability of the true phase domain by distinguishing the DCOs' digital phase from the low-frequency reference phase [11]. In recent years, the cell-depend design flow has mostly been used for ADPLL for low-frequency applications. It comprises two architectures: Time-to-Digital Converter (TDC) based ADPLL and bang-bang detector [12]. Based on the applications, each system's operating frequency is developed [13]. However, in such applications, the battery's lifetime is limited [14]. The key specification for the frequency range is the faster lock-in time [15].

To improve the lock-in range of the ADPLL, oscillation tuning word is utilized for many research works by using the

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estimation and binary search algorithm for frequency search operation [16, 17]. Recently, frequency multiplier with injection-locked ADPLL received attention because of its low power consumption [18]. However, the design attains poor noise performance and maximizes power consumption, which becomes a structure limitation [19, 20]. So, the present work was motivated to implement the ADPLL with the CORDIC algorithm for using ADPLL in low-frequency applications.

The further description of the presented model was aligned as follows: Section II explains the related works. Section III presents the existing methodology. Section IV elaborates on the proposed method. Section V presents the details of experimental studies. Section VI concluded with the conclusion and future work, respectively.

II. RELATED WORKS

Few recent works of literature related to ADPLL architecture are described as follows,

Palaniappan *et al.* [21] proposed an ADPLL without TDC for medical implanting applications. Here, the ADPLL inhibits the modules such as PD, frequency controller, divider and ring oscillator for DCO with boosted capacity. The PD detects the difference between the output and reference pulse and the phase error signal that is up and down. The expected frequency, *N* times the frequency divider, provides the reference frequency. Here, the local oscillator is replaced with the frequency controller. It achieves a good jitter performance, small implementation surface and minimized power consumption. However, the requirement of the phase noise is not satisfied.

In power electronic applications, grid synchronization is critical through high-performance PLL. Therefore, Zhang *et al.* [8] proposed a unique single-phase ADPLL. Initially, the single orthogonal generator-based phase detector is utilized for extracting the phase error of the sine and cosine signal. The PD and DCO are operated by the response of the Direct Digital Synthesis block and the CORDIC block. To achieve higher accuracy and faster response, a new parameter optimization is employed to decrease the loop delay. Finally, the whole ADPLL architecture is tested on a Field Programmable Gate Array (FPGA). The robustness of the ADPLL is increased. However, its force of response for the phase jump and frequency step is slow, and voltage sag remains high.

Bissa *et al.* [22] presented the architecture of ADPLL concerning low-frequency applications (LFA-ADPLL) with optimum power and area. Here, the ADPLL design is built by four blocks: PD, LF, DCO and DDS. In the process of ADPLL, the distance of the delay line is computed by the binary search algorithm and is given to the DDS for the conversion of phase to amplitude. This method effectively reduced the area overhead and provided a top resolution. The binary search algorithm has succeeded in the faster lock-in range for every arbitrary frequency change; however, the DCO design glitches during the transition from one frequency to another.

The methods now used to increase locking range quickly take advantage of various overloaded modules. So an Optimal Sampling Digital PLL (OSDPLL) incorporating high Precision TDC and wide range high-resolution Dinesh and Marimuthu [23] thus introduced DCO. The locking range is enhanced, and the frequency resolution is raised. The redesigned bang band detector, employed as a phase detector, also lowers excessive power usage. However, unacceptably bad noise shape deterioration happens during fractional precision.

Kumm *et al.* [24] presented FPGA-based linear ADPLL (FPGA-LADPLL). It comprises three modules: detector, oscillator and loop filter. Initially, the analytical representation of the reference signal is created by the realization of the Hilbert transform in the PD module. Furthermore, the instantaneous phase of the signal is evaluated by using the CORDIC algorithm. It increases the ADPLL system's linear range and provides a fast lock-in time for the arbitrary frequency. However, it could increase the design time and complexity of ADPLL.

The key contribution of the presented model is,

- A novel architecture of ADPLL using the CORDIC algorithm has been designed with three modules: PD, LF and DCO.
- Input signals are applied in the PD. The PD computes the phase difference of two signals, and LF removes the higher frequency.
- The DCO signal is matched with the reference signal and put ADPLL into the locked state.
- Furthermore, the CORDIC algorithm is utilized to compute the length of delay line corresponding to the correct DCO frequency.
- Fast locking for arbitrary frequency changes is made possible by the CORDIC algorithm.

III. SYSTEM MODEL AND PROBLEM STATEMENT

The category of PLL in which all the circuits are executed by a digital approach is ADPLL. Initially, phase detection is carried out and implemented in this system. The delay line length of the VCO signal is calculated, and sine and cosine signals are created. To lessen the area overhead of low-frequency applications, the developed sine and cosine signals are transformed from phase to amplitude. It produces fewer glitches while converting one frequency to another and helps in reducing power dissipation. The system model is illustrated in Fig. 2.

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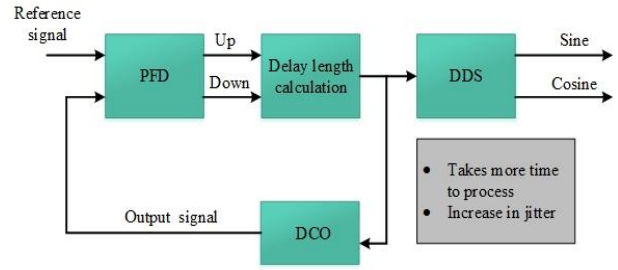

Fig. 2. System model with the problem statement.

However, due to the huge size of the capacitance, it needs some duration to recharge it from the previous phase. It increases the jitter and the output frequency. It has been described and formulated in several existing approaches. It has maximum shielding towards external environmental variations and reduced dissipation of power. Also, it guarantees a wide tuning range, little area and power efficiency. However, sometimes, for low-frequency relaying applications attaining the lock state in ADPLL is complex because of the maximum delay line. Hence, it should be minimized. This issue has motivated the present study.

IV. PROPOSED METHODOLOGY

A novel Particle Swarm based ADPLL (PS-ADPLL) using the CORDIC is proposed for low-frequency applications. The proposed PS-ADPLL uses the optimized phase detector to optimize the delay line of the feedback signal. The working procedure of the proposed methodology is illustrated in Fig. 3.

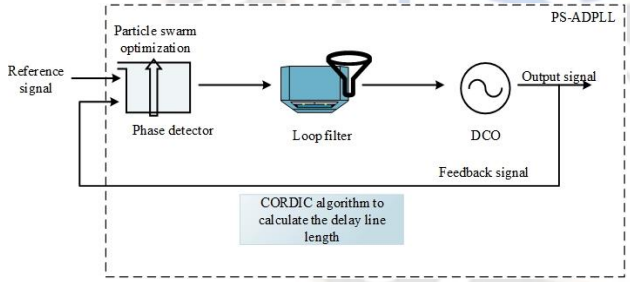

Fig. 3. Proposed methodology.

This architecture consists of three modules: PD, LF, and DCO. Initially, the feedback signal and the reference signal are given to PD to detect the phase difference, attain a lock state, and generate the up and down signal. These signals are then fed into the loop filter to create a carry and borrow signal and given to the DCO to generate the output signal. In the lower-frequency application, the delay line is increased in the output signal. So, to achieve a faster lock-in range, the delay line of the output signal is calculated by the CORDIC algorithm and optimized by the particle swarm optimization at the phase detector module.

A. Proposed PS-ADPLL

The proposed Particle Swarm based ADPLL (PS-ADPLL) was built with three modules: PD, LF and DCO. The entering of input reference signal to the PD initializes the process of ADPLL. In low-frequency applications, the waveform's delay line is higher, which is critical to achieving the lock state. Therefore, in the proposed ADPLL architecture, the phase detector works based on the CORDIC algorithm and particle swarm optimization for calculating and optimizing the delay line extend in the output signal for low-frequency applications. The objective function of the presented approach is to optimize the delay line that corresponds to the phase and frequency to match the output signal with the input reference pulse to make the ADPLL a lock-in state in a short period. The further explanations of the ADPLL functions are described as follows.

1) Digital phase detector

In the proposed model, the phase detector is implemented using D flip-flop. It distinguishes the frequency and phase of the input and signal produced at the output to attain a lock state, and the error signal is created as an up-and-down signal. The developed error signal is equivalent to the variation in frequency of the output and input signal. It is given in (1). The PD output contains both the frequency and phase components.

$$D(t) = g_D[\varphi_e(t)] \quad (1)$$

where $D(t)$ is the output signal of PD, g_D is the detector gain, and $\varphi_e(t)$ is the phase error signal. These generated up and down signals are then given to the loop filter.

2) Digital loop filter

The second module of the presented model is the loop filter. The loop filter is nothing but an integrator. In the proposed architecture, the 4-bit up/down counters that act as LF, and it is a simple filter. It comprises two independent counters: the up counter and the down counter. Both the counters range from 0 to 7. The up/down counters take up, down and clock pulses as input. It eliminated the greater frequency of the up and down signal and generated a borrow and carry signal. These borrow and carry signals are fed into the DCO.

3) Digital controlled oscillator

The increment decrement counter is used as a digitally controlled oscillator in this design. Depending on the output of the LF, the DCO changes the frequency of the generated signals. A pair of blocks is presented in the increment decrement counter. Here, the carry waveform is allocated as input of the DECR, and the borrow signal is designated as input of the INCR. Additionally, the ID clock signal is given to the counter for dividing the output of the counter. The clock pulse of the increment decrement counter is $2N$ times the multiple of the reference frequency.

4) Delay line length calculation

To attain the target frequency, the length of the delay line in the DCO output is calculated using the CORDIC algorithm

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[25]. The reduced output of the CORDIC algorithm indicates an increase in the DCO frequency. Similarly, the outcome of the CORDIC increased, indicating a reduction in the DCO output frequency. The delay line length calculation using the CORDIC algorithm is explained as follows. This method rotates the output coordinate vectors by a constant angle until the vector's angle is decreased to zero. The frequency resolution of the output waveform is added by one bit for each iteration, and N represents the total number of iterations. The coordinates of the output vector A are given as (X_a, Y_a, Z_a). Driving Z to 0, the CORDIC performs as assigned in (2),

$$\begin{bmatrix} X_a \\ Y_a \\ Z_a \end{bmatrix} = \begin{bmatrix} P(X_a \cos Z_a - Y_a \sin Z_a) \\ P(Y_a \cos Z_a + X_a \sin Z_a) \\ 0 \end{bmatrix} \quad (2)$$

At the end of the iterations, the above matrix can be transformed as given in (3) with the initial values $X_a = 1/P$, $Y_a = 0$ and $Z_a = \theta$.

$$\begin{bmatrix} X_a \\ Y_a \\ Z_a \end{bmatrix} = \begin{bmatrix} \cos\theta \\ \sin\theta \\ 0 \end{bmatrix} \quad (3)$$

For the calculation of the delay line, the CORDIC algorithm has been taken in its vectoring node. Here, to meet the requirement for the calculation of delay line, the coordinate *Y* is driven to 0 instead of Z, and the final vector lies on the x-axis by providing the Value of delay line length in (4).

$$\begin{bmatrix} X_a \\ Y_a \\ Z_a \end{bmatrix} = \begin{bmatrix} P(\sqrt{X^2 + Y^2}) \\ 0 \\ \tan^{-1}(Y/X) \end{bmatrix} \quad (4)$$

Here, neglecting the amplification factor *P*, X_a is the required delay line length, and Z_a is the corresponding phase value.

5) Optimization of delay line

The delay line length calculated output waveform from the CORDIC is then analyzed by the particle swarm at the phase detector module. The delay line is optimized using the expression described in (5),

$$f(t) = r(t) + \alpha + \beta \sum_{i=1}^{m} \min[0, X_a(t)] \quad (5)$$

Here the $f(t)$ represents the objective function, i.e. optimization of the delay line of the output waveform, $r(t)$ indicates the reference signal, α and β are constants, $X_a(t)$ is the delay line calculated signal. Thus, the proposed architecture minimizes the delay line making the ADPLL architecture suitable for low-frequency applications.

The steps and processes presented in the designed model were detailed in Algorithm 1. The Xilinx code was executed based on these step processes, and the results were verified. The algorithm incorporated all mathematical function parameters in the pseudocode format. These processes are given step by step in algorithm 1.

Algorithm 1: PS-ADPLL

Start
{
//input is the reference signal
Phase detector ()
{
//accepts reference signal and DCO signal as input
int $D(t), g_D, \varphi_i(t), \varphi_o(t)$
$D(t) \rightarrow \varphi_i(t) - \varphi_o(t)$
//up and down signals are generated
}
Up/down counter ()
{
Higher frequency parts of the signals are removed.
//carry and borrow signals are generated
}
Increment decrement counter ()
{
$I_{out} \rightarrow \overline{\text{toggle} + \text{IDc}lock}$
//output signal is generated.
}
Delay line length calculation ()
{
int X_a, Y_a, Z_a
$X_a \rightarrow P(\sqrt{X^2 + Y^2})$
//delay line of the output waveform is calculated
}
Optimization ()
{
int $Z_a(t)$
$\text{optimizati on} \rightarrow \min[Z_a(t)]$
//the delay line of the output waveform is reduced
}
}
stop

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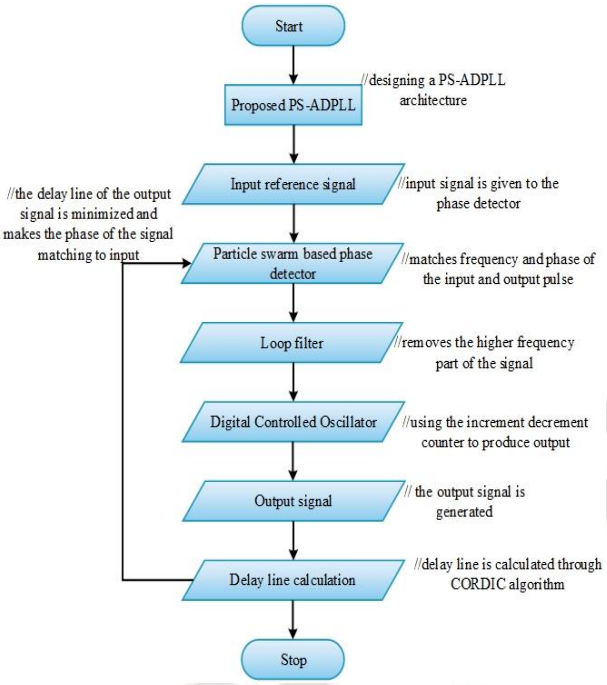

Fig. 4. Flowchart PS-ADPLL.

In the proposed architecture, the CORDIC algorithm was used at the feedback loop to calculate the delay line of the output signal sent to the PD. Furthermore, the PD activates the particle swarm to optimize the estimated delay line for making the ADPLL lock state suitable for low-frequency applications. The flow diagram of the suggested architecture is given in Fig. 4.

V. RESULTS AND DISCUSSION

The suggested PS-ADPLL comprises three modules: PF, LF and DCO. Here, the DCO generates the output signal with an excess delay line, which is common in low-frequency applications. Due to the increased time delay, it isn't easy to attain the fast locking state. Therefore, using the CORDIC algorithm, the length of the delay line is calculated using (4) and is optimized in the phase detector module. This makes the output signal phase match the reference signal to achieve the lock state for low-frequency applications.

The performance parameters such as power dissipation, power consumption, lock-in time, stability, and combinational delay are also calculated. In a comparative analysis, the evaluated power dissipation, power consumption and lock-in time are compared with various current approaches to estimate the improvement score. The designing parameters required for implementing the proposed model are tabulated in Table 1.

TABLE 1: DESCRIPTION OF IMPLEMENTATION PARAMETERS

Parameters	Description
OS	Windows 10
Platform	Xilinx ISE
Version	14.7

A. Case Study

A case study was conducted to study the efficiency of the designed system. Here, the initial input is the reference signal. The simulation results of the proposed PS-ADPLL at each block are described below.

In the proposed model, the reference signal and VCO signal are given as input to the PD, the first module of the ADPLL architecture. The PD compares the frequency and angle of the reference and VCO waveform. If the input signal rising edge leads to the VCO signals, then an up signal is generated. Similarly, if the standup edges of VCO signal exceed the reference signal, then the down signal is generated. The output of the phase detector is up and down signals, which are shown in Fig. 5.

The result of the up/down counter is shown in fig. 6. The up/down counter generated the carry signal as output. If the UP≥4, carry equals 1, and if the DOWN≥4, borrow equals 1. These generated carry and borrow signals are then given to the DCO to adjust the frequency.

The simulation result in ADPLL from the increment decrement counter before optimization, which is the NOR of toggle waveform and ID clock pulse, is given in Fig. 7. Here, VCO is the output signal obtained before the delay line calculation and optimization. The two different amplitudes are present in the output signal. The first amplitude is 1, and the second amplitude is 0. When the carry and borrow signals are divided by the clock pulse, the output signal changes concerning the input reference signal. That is 1 for the high input and 0 for the low intake.

The generated output signals are given to the CORDIC for the delay line calculation. They are optimized in the phase detector module, and the D flip-flop matches the output and reference signal to make the ADPLL into the locked state. The locked state of the proposed PS-ADPLL is given in Fig. 8. The proposed model achieves the lock state at 75.5 ns.

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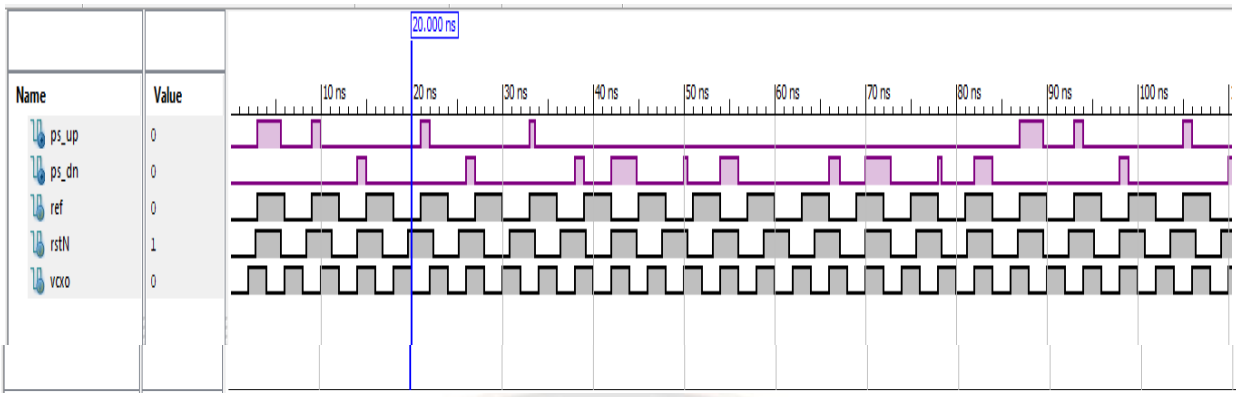

Fig. 5. Phase-detector output.

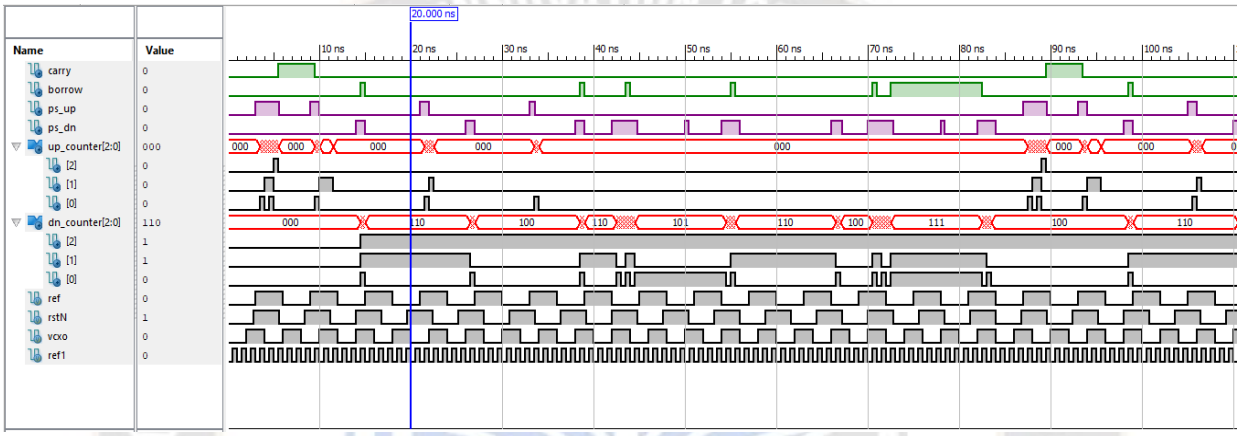

Fig. 6. Up/down counter.

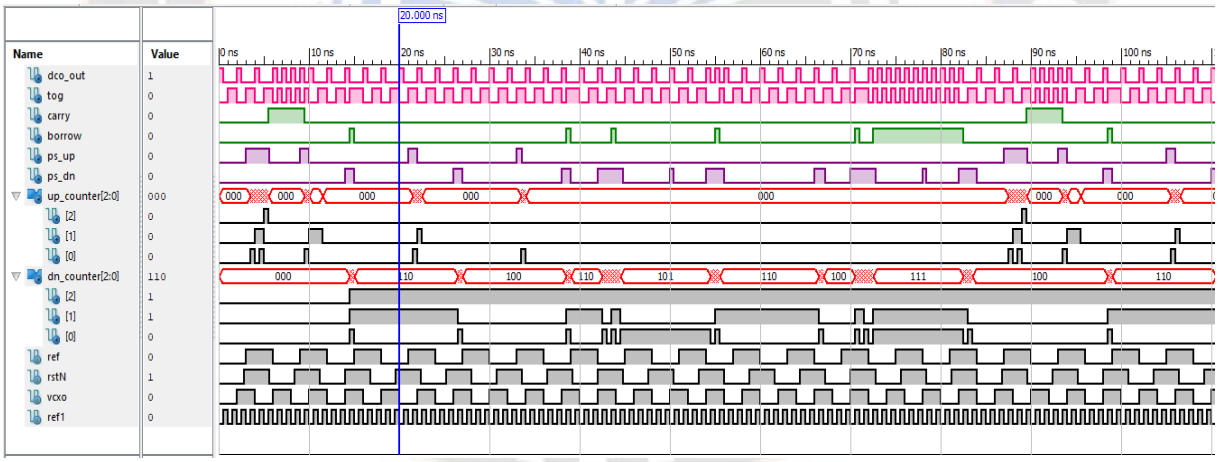

Fig. 7. Increment decrement counter.

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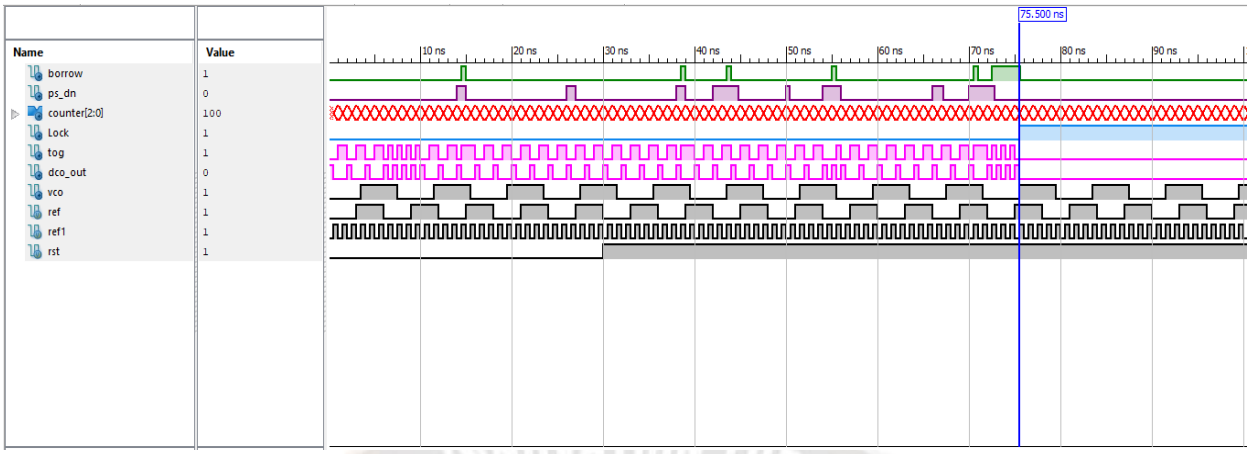

Fig. 8. Lock state of the PS-ADPLL.

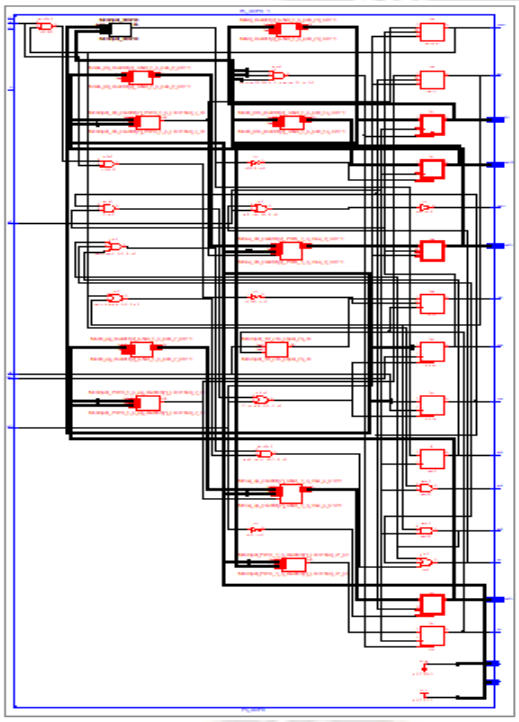

Fig. 9. ADPLL RTL Schematic.

After the simulation of the proposed PS-ADPLL, RTL is generated and synthesized, shown in Fig. 9. The proposed PS-ADPLL has been executed by Xilinx ISE 13.2.

B. Performance Analysis

The proposed PS-ADPLL with the CORDIC algorithm is developed on the Xilinx ISE version 14.7 running on the Windows 10 operating system. The presented model is designed using the Verilog HDL and tested on FPGA. The terms such as power dissipation, power consumption and lock-in time are computed to validate the efficiency of the suggested approach with existing models such as 2.4 GHz Low Power ADPLL (2.4 LPADPLL) [27], Variable Phase Accumulator (VPAC) [28], ADPLL with Optimized Digital Controlled Oscillator (ADPLL-ODCO) [29] ADPLL with Varactorless LC Digital Controlled Oscillator (ADPLL-VLCDCO) [30], Injection Locking Time to Digital Convertor based on Ring Oscillator (CFRO-ILTDC) [31], Fractional-N ADPLL (FNADPLL) [32], Bang-Bang Phase Frequency Detector (BB-PFD) [33] and Hybrid Phase Locked Loop (HPLL) [34].

1) Power dissipation

Power dissipation is evaluated by the ratio of the total power supplied to the real power loss. It is the maximum power that is dissipated under certain thermal conditions. It describes the loss or waste of energy in heat format during a certain process. It is calculated by the (6),

$$\text{powerdissipation} = \frac{\text{total powerSupplied}}{\text{powerloss}} \quad (6)$$

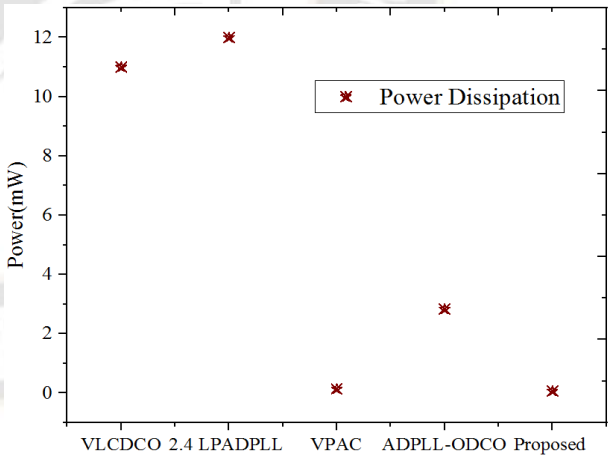

Fig. 10. Comparison of power dissipation with existing techniques.

The power dissipation of the current model, such as VLCDCO, scored 11mW, 2.4 LPADPLL scored 12mW, VPAC scored 0.141mW, and ADPLL-ODCO is 2.83mW. While the presented model scored power dissipation as 0.07mW, which is lower than the other existing models. The comparison of power dissipations with current models is given in Fig.10.

2) Locking time

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The locking time is when the ADPLL based circuits can achieve a lock state under various additional conditions. The lock-in time of the proposed architecture can be calculated by the expression in (7),

$$t_{lock} = \frac{\pi}{(2\pi / F_r)(\delta k_{vco} - F_0)} \quad (7)$$

Here, F_r is the reference clock frequency, F_0 is the initial frequency error and δ is the proportionality gain.

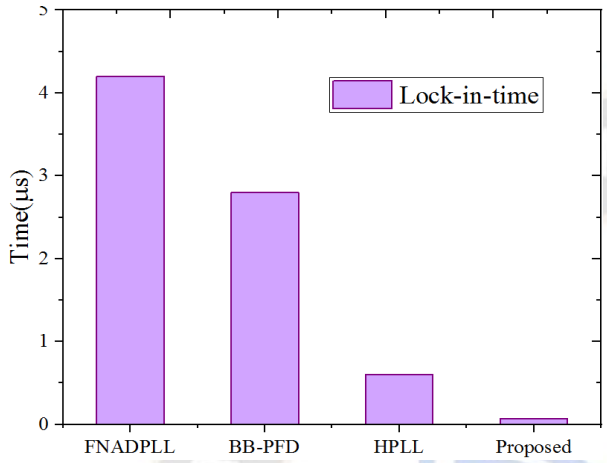

Fig. 11. Comparison of lock-in time with existing techniques.

The existing approaches, such as FNADPLL, achieved the lock state in 4.2 µs, BB-PFD in 2.8 µs, and HPLL in 0.6 µs. At the same time, the proposed ADPLL architecture reached the lock state at 0.07 µs. Comparing the other existing approaches, the proposed PS-ADPLL attains the lock state quickly. The comparison of lock time is illustrated in Fig. 11. This short time is achieved by activating the particle swarm in the phase detector module of the proposed ADPLL. It optimizes the delay line, which varies from the input signal to make it similar to the reference signal.

3) Power consumption

The total power consumed to implement the proposed ADPLL to achieve the lock state is power consumption. It is one of the important parameters in the digital system.

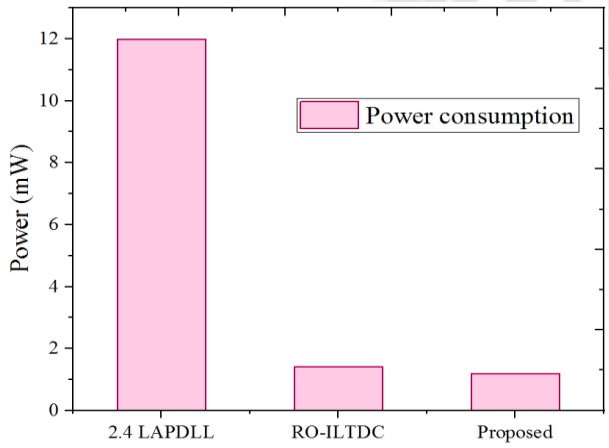

Fig. 12. Comparison of power consumption with existing techniques.

The existing models, such as 2.4 LPADPLL, consumed power ranges from 8 to 12mW, and CFRO-ILTDC consumed the power about 1.4mW. The proposed architecture consumes a power of about 1.2mW, which is lower than the other existing approaches. The power consumption comparison is displayed in Fig. 12. Due to the fast locking range, the proposed model consumes low power, and the power dissipation is also much less since it is an efficient and cost-effective method.

C. Discussion

Here, the delay line of the output signal present for the low-frequency application is calculated by the CORDIC algorithm before being it to the phase detector. The calculated delay line of the output is then optimized in the phase detector module by activating the particle swarm. After optimizing, the D-flip flop compares the reference and the optimized output signal to attain the lock state. The overall efficiency gained by the presented model is given in Table 2.

TABLE 2: OVERALL PERFORMANCE

Overall Performance statistics	
Stability	Good
Power consumption	1.2mW
Phase error	±1.2°
Power dissipation	0.07mW
Combinational delay	0.948ns
Maximum frequency	667.646MHz

In the proposed method, the power consumption is 1.2mW, and the power dissipation is only 0.07mW, which is lower than all other existing approaches. The combinational delay in the process of the proposed architecture is 0.948ns, which is very low. Hence, the lock state is achieved in less time. The maximum frequency range is 667.646MHz.

The comparison of the proposed work with a few existing approaches is depicted in Table 3.

TABLE 3: SUMMARY OF STATE-OF-THE-ART APPROACHES

Author	Method	Advantages	Disadvantages
Palaniappan *et al.*	TDC-less ADPLL	It produces a good jitter performance, little implementation area and reduced power consumption.	The requirement of the phase noise is not satisfied.
Zhang *et al.*	Single phase ADPLL	Accuracy and the robustness of the architecture are increased	The frequency step and phase jump response speed is slow.
Bissa *et al.*	LFA-ADPLL	The use of a binary search algorithm succeeds in the faster locking range for every arbitrary frequency changes.	The DCO design produces glitches during the transition from one frequency to another.
Dinesh and Marimuthu	OSDPLL	Minimizes the excessive power	Unacceptable bad noise shape

		usage	deterioration happens during the fractional precision.
Kumm *et al.*	FPGA-LADPLL	It increases the linear range of the ADPLL system and provides a fast lock-in time for the arbitrary frequency.	It could increase the design complexity and time of the ADPLL.
Proposed	PS-ADPLL	It attains a fast locking state and is applicable for low-frequency applications.	The hybrid system will enhance the method.

VI. CONCLUSION

A novel Particle Swarm based ADPLL (PS-ADPLL) with a CORDIC algorithm is proposed to make a locking state ADPLL, which is suitable for low-frequency applications. Initially, the reference waveform and VCO pulse are input to the PD to create an up-and-down signal by matching those two signals. Utilizing the generated up-down signal, the up-down counter provides the carry and borrow signal and is fed into the increment decrement counter to create the output signal. In low-frequency applications, the provided output signal contains a delay line. Therefore, the length of the delay line is calculated and optimized to achieve a faster locking state. Thus, the proposed model is suitable for low-frequency applications. The developed model attained a very low power dissipation of 0.07mW, which is lower than the other existing models. Also, the combinational delay of the designed circuit is 0.948ns. The power dissipation in the current method ADPLL-ODCO scored 2.83mW. So, the power dissipation in the proposed model is reduced by about 1mW. This model takes less time to attain the lock state. It is complex to design. In future, the hybrid system will enhance the ADPLL architecture.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Both the authors contributed equally.

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