A Dynamic Parallel and Pipelined Architecture for Intra Prediction in H.265 Standard

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***Abstract*—** In the present world where technology is growing faster, the video based applications are rapidly increasing and needs a technology which supports high resolution videos. High Efficiency Video Coding (HEVC) method is one which works on 4K and 8K video applications. In this work we have implemented the new parallel and a hardware accelerator which is highly efficient for the intra prediction blocks. Due to parallel and pipelined architecture, Intra Prediction speeds up the process of prediction and also minimizes the time required for accessing the data from the memory. The given architecture design reduces Area, Power and Delay elements. The results when compared with different FPGA versions shows that our architecture consumes 69 LUTs in ZYNQ FPGA for 4X4 pixels.

Keywords*-Coding Tree Unit, Video Coding, HEVC,Quadtree, Intra Prediction*

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I. INTRODUCTION

Inthe recent years due to rapid growth in internet technology and computers, video streaming applications are also growing rapidly. The new HEVC standard is the advancement in the video compression technique developed by Joint Collaborative Team on Video Coding (JCT-VC). HEVC is a new advanced technology which compresses the data into half of its predecessor H.264 and maintains the same level of video resolution or in other words, enhances the video with same bit rate. HEVC supports resolutions of upto 8192 X 4320 to 1920 X 1080 i.e., it supports 4K and 8K videos.

The improvements in HEVC are many. Firstly, the introduction of Coding Tree Unit (CTU)which is similar to macro blocks in H.264. The CTU is the basic processing element in HEVC which supports a variable size of 64 X 64 Prediction Units (PU) to support high definition video but in H.264 the frames were divided into 16 X 16 macro blocks. The second improvement is Intra Prediction coding which is one of the most efficient and important in coding the video standards, which is used in the prediction of pixels known as PU. It attains better efficiency compared to previous H.264 technique because HEVC supports 33 angular predictions and 2 non-directional predictions and also computes the frame into 64 X 64 PU's and it makes use of spatial redundancy in a single frame to get an efficient coding. All these developments in HEVC makes algorithm execution complex and unique. For all modes PU is chosen on least cost computed. HEVC prediction works with intensity and colour difference components like LUMA and CHROMA samples respectively.

When HEVC was first introduced many software and hardware implementations were proposed and developed to reduce the execution time, power, area and delay for real time processing of high resolution videos like 4K and 8K. In this paper we have concentrated on the most efficient novel architecture for intra prediction in HEVC.

II. RELATED WORK

Chao-Tsung Huang et al., [1] proposed an area efficient and high throughput VLSI architecture, which achieves a throughput of 246 samples/cycle. It consumes 27.0K gates and 4.9KB of Static RAM to store the pixel data using 40nm technology. The Automatic Place and Route (APR) core are used in 0.036mm^2 and the power consumed is 2011mW for full HD video applications.

Mateus Grellert et al.,[2] presented a theory in which a combination of hardware and software is used to minimize the complexity in intra prediction of HEVC for video contents. It provides highly probable coding configuration in software as the size and directions of the intra prediction in estimation for the prediction unit. In the hardware part specialized co-processors enhances the reusability and are used as accelerators. Depending on the video quality, software administrates the energy management of the hardware processors. Woo-Jin Han et al., [3] proposed the intra coding method that provides significant improvement in both subjective and objective quality of compression for still images and videos.

Grzegorz Pastuszak et al., [4] proposed the computationally scalable algorithm for intra prediction which encodes up to 2160 pixels at 30 frames/sec resolution and provides scalability between compression efficiency and throughput. It takes the advantage of simplified rate-distortion optimization architecture, the pre-selections of pixels based on prediction from the original pixels which uses same resources as regular processing.

Jing et al., [5] proposed a pipelined architecture for various pixels ranging from 4 X 4 to 64 X 64 with an operating frequency 204MHz.

The paper proposed by Kahn et al., [6] had a pipelined architecture to process the PE simultaneously for all size modes that achieve a frequency of 213MHz at a resolution of 1080 for 4K videos at 120frames/sec.

The paper is structured as shown: Section I and Section II gives the introduction and related work on HEVC respectively. Intra prediction in HEVC standard discussed in Section III. Section IV discusses the Propound hardware architecture and Section V shows the Results and its Discussions of the work. Lastly Section VI gives the Conclusion.

III. INTRA PREDICTION IN HEVC

The three steps included in the process of Intra prediction are,construction of the reference samples in an array, prediction of samples and processing of the final samples. High coding efficiency is achieved by the above 3 steps and computational requirements are minimized. The prediction modes in HEVC consist of various methods in content modelling which are found in video and still images.

The classifications of Intra prediction in HEVC are Angular, Planar and DC predictions. First one being the Angular prediction helps to predict the structures with directional edges which are used in codec. Planar method and DC prediction helps in calculating the smoothness of the image. There are totally 35 modes supported in HEVC which supports flexible coding.

A. Coding Technique in HEVC

Video partitioning in HEVC is described by Quadtree which is also known as coding tree as shown in the Figure 1. Division of frames into pixels are depending on the resolution and is shown in Figure 2. Quadtree block partitioning [8] which is more flexible and coded efficiently depending on the resolution of video. It is broadly divided into 4 levels Coding Tree Unit (CTU), Coding Unit (CU), Prediction Unit (PU) and Transform Unit (TU).CTU divides each frame into various pixels of size 4 X 4, 16X16, 32X32 or 64X64.

The LUMA component has one CTU and two Coding Tree Block (CTB) for Chroma component, and further CTU is sub-divided into CU, which again can be splitted into different square sized regions such as4 X 4, 8 X 8,16 X 16,32X32 and 64X64 depending on the picture resolution and CU can be further divided into PU.

The prediction unit is used for both inter block prediction and intra block prediction for variable sizes from 4X4 down to 64X64 depending on the types of mode decision, and also

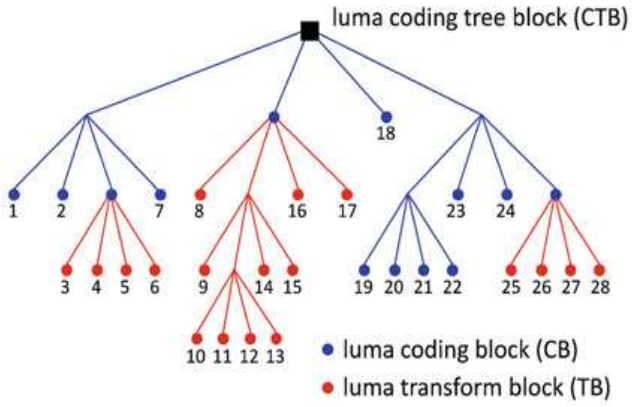

Fig. 1. Quadtree Structure.

transform unit for PU is suited for quantification and transformation. The coding unit acts as a processing unit for coding which is chosen by the encoder.

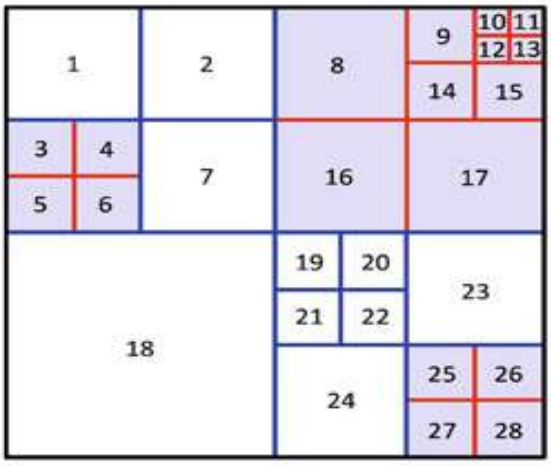

Fig. 2 The Division of a 64 X64 Pixels into Coding Tree Block.

B. DC mode

The DC mode is used in the images which have small changes in the adjacent pixels and is more suitable to generate the prediction of natural block. The mode is predicted from all neighboring horizontal and vertical pixels. The blocks of size 16X16 and even smaller, which is predicted using DC prediction mode and passes through a filtering process to soften the above and left edges of the block. The dc prediction is calculated using the equations (1) and (2) [7].

$P_{pred}(a, b)$ is the Predicted Pixel Sample value with (a, b) = 0-------N_t-1.

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P_{ref}(a, b) is the neighboring sample pixel value with (a, b) = 0-----N_t * 2 -1.

$$dc\_Value = (\sum_{a=0}^{Nt-1} P_{ref}(a,-1) + \sum_{x=0}^{Nt-1} P_{ref}(-1,b)) \gg (\log 2(Nt)+1) \quad (1)$$

Where N_t gives the transform block size

$$P_{pred}(0,0) = (P_{ref}(-1,0) + 2 * dc\_Value + P_{ref}(0,-1) + 2) \gg 2$$
$$P_{pred}(a,0) = (P_{ref}(a,-1) + 3 * dc\_Value + 2) \gg 2$$
$$P_{pred}(0,b) = (P_{ref}(-1,b) + 3 * dc\_Value + 2) \gg 2 (2)$$

C. Planar Mode

Planar prediction is used to overcome the issues of both DC prediction and angular prediction. They are used to eliminate the discontinuities by generating the prediction surface and are calculated by taking the average of both vertical and horizontal linear prediction samples.

Equation (3) is used to calculate Planar Modes for four sample reference pixels.

$$P_{pred}(a,b) = \big((N_t - 1 - a) * P_{ref}(N_t,-1) + Nt-1-b*Pref a,-1+bb+1*Pref-1,Nt+Nt \gg (\log 2(Nt)+1) \quad (3)$$

D. Angular prediction

Angular prediction modes are used for high frequency components and complex texture videos. It has 33 angular predictions and accuracy of 1/32 samples is shown in Figure 3, these 33 angles are designed to provide low computational requirements in different directions on neighboring pixels, out of these 2 to 18 are horizontal mode and 19 to 34 are vertical mode.

Angular prediction is calculated using

$$idx = ((a+1) * Intrapredictedangle \gg 5 \quad (4)$$

$$iFa = ((a+1) * Intrapredictedangle \quad (5)$$

$$perdSamp[a][b] = \big((32 - iFa) * ref(b + idx + 1) + iFa*refy+idx+2+16\gg5 \quad (6)$$

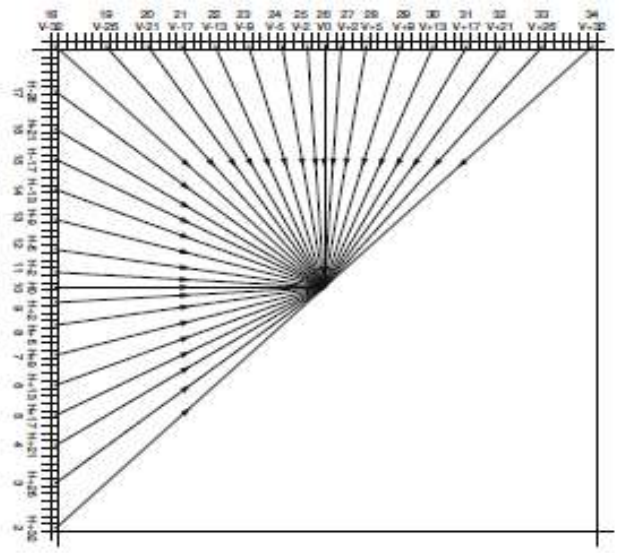

Fig. 3: HEVC Angular Representation of Intra Prediction for 2 to 34 Angles.

IV. ARCHITECTURE FOR INTRA PREDICTION

The work, A Dynamic Parallel and Pipelined Architecture for Intra Prediction (ADPPA) is as shown in the Figure 4. It has four major blocks with a Control Unit and a Register to store a final predicted value.

The First block is a dedicated memory block. In this architecture the neighboring pixel values of the image or video are loaded and stored in one part of the memory and the predicted pixel value is stored in other part.

The second block is DC intra prediction mode as shown in the Figure 6. It is comprised of adders and shifters to perform the calculations of equation (1) and (2). Any complexities in the computation of the equation can be made less by the block treatment.

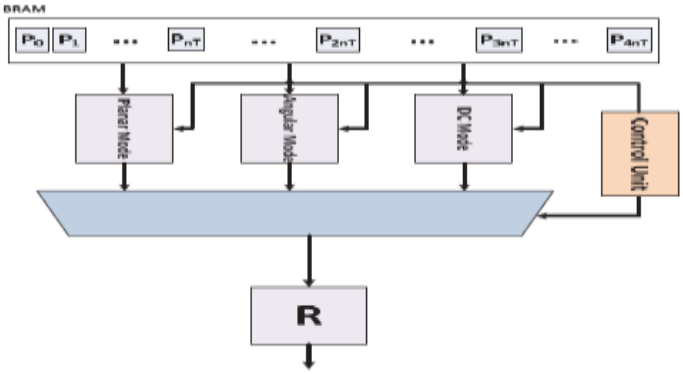

Fig. 4. Architecture for the Intra Prediction.

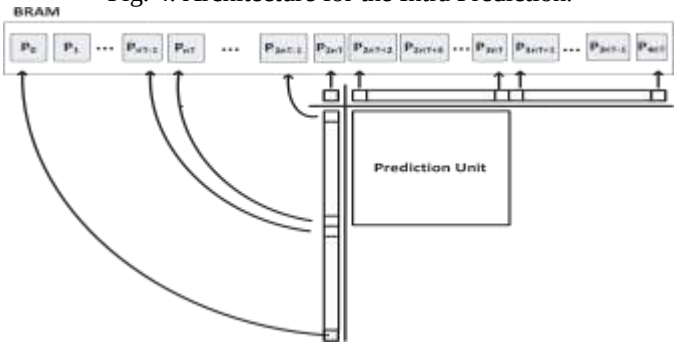

Fig. 5. Adjacent Pixels of Image Stored in the RAM Memory.

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The calculations for this architecture is based on equation (3) to (6) and it consists of multiplexers, adders [9] and processing elements. Neighboring pixels of the frame are given as the input for this, and *S2* and *S3* are the output results of the planar and angular mode.

All the reference sample pixels of the image are stored in a single array in the memory block RAM as shown in Figure 5. The first reference samples are vertical pixel values of the image that are stored in left side of the RAM and horizontal pixels are stored in the right side of the image that is in second part which are used for prediction.

The proposed parallel processing for 4X4 intra prediction block is shown in the Figure 6. It can be pipelined for bigger pixel values such as8X8, 16X16, and 64X64 and so on. With increase in the pixel values it utilizes more hardware resources for processing the data

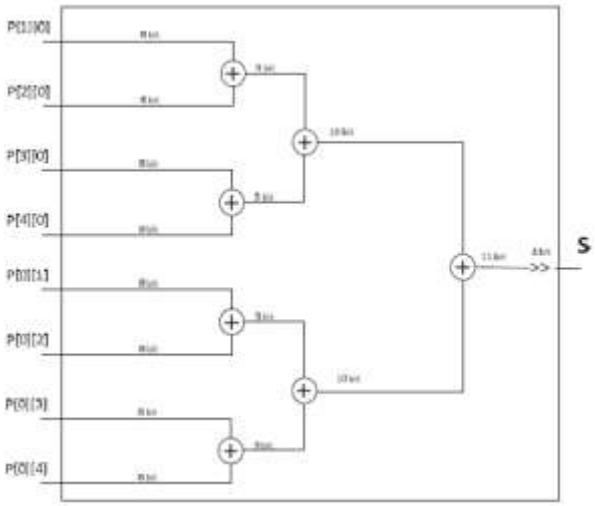

Fig. 6. Eight Input Samples for DC Intra Prediction Processing.

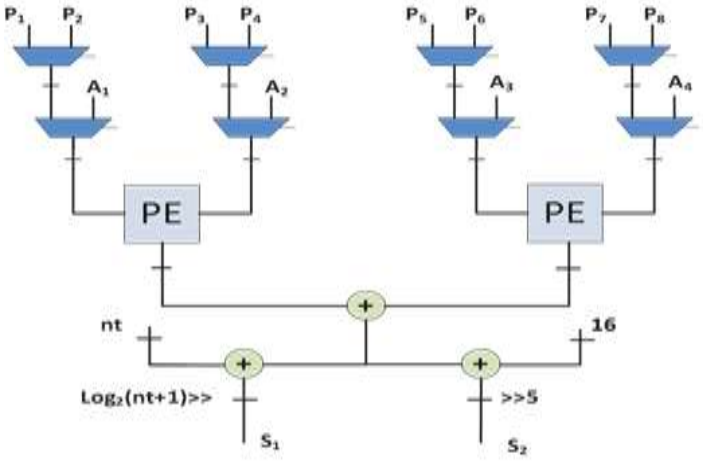

Fig.7. Hardware accelerator for both angular and planar mode

The processing element in Figure 7 is a 32bit unsigned multiplier relays on carry save adder. This hardware architecture is designed to work parallel with 4 sample levels and it is carried out by 8 sample clock cycle to load and store data between the external memories.

V. RESULTS AND DISCUSSION

The ADPPA for the intra prediction which has proposed is implemented using Verilog and it was simulated using MODELSIM simulators for4X4 blocks and the results of simulation are as shown in Figure 8. The proposed architecture can compute 90frames/sec for 4k videos. To achieve a resolution of 4K videos at 30fps with 4:2:0 sampling it requires (3840X2160X1.5X 30) that is 373.24 MSamples/sec as output. So the experimented outcome is higher than this value. The recommended architecture can be improved further.

The ADPPA architecture was synthesized using Xilinx for 4X 4 pixels. This architecture works by consuming 71 LUTs in SPARTAN 6 FPGA and 68 in ZYNQ FPGA. The comparison of synthesis results given importance to design area for various FPGAson are given in Table 1.

Table 1. Logic Utilization of FPGAs

FPGAs	ZYNQ	ARTIX-7	VERTEX-7	SPARTAN 6
Number of slice registers	68	69	69	72
Number of slice LUTs	159	168	168	162
Number of fully used LUT-FF pairs	67	67	67	67
Number of bonded IOBs	50	50	50	50
Number of BUFG/BUFGCTRLs	1	1	1	1

VI. CONCLUSION

We have propound an efficient parallel architecture for intra prediction using H.265 coding technique. When implemented on ZYNQ FPGA boards results shows which have a better performance compared to VERTEX-7 and ARTIX-7 FPGAs. Without any major modification in the algorithm it enhances the process of encoding in intra prediction, as it works parallel with pipelined architecture.

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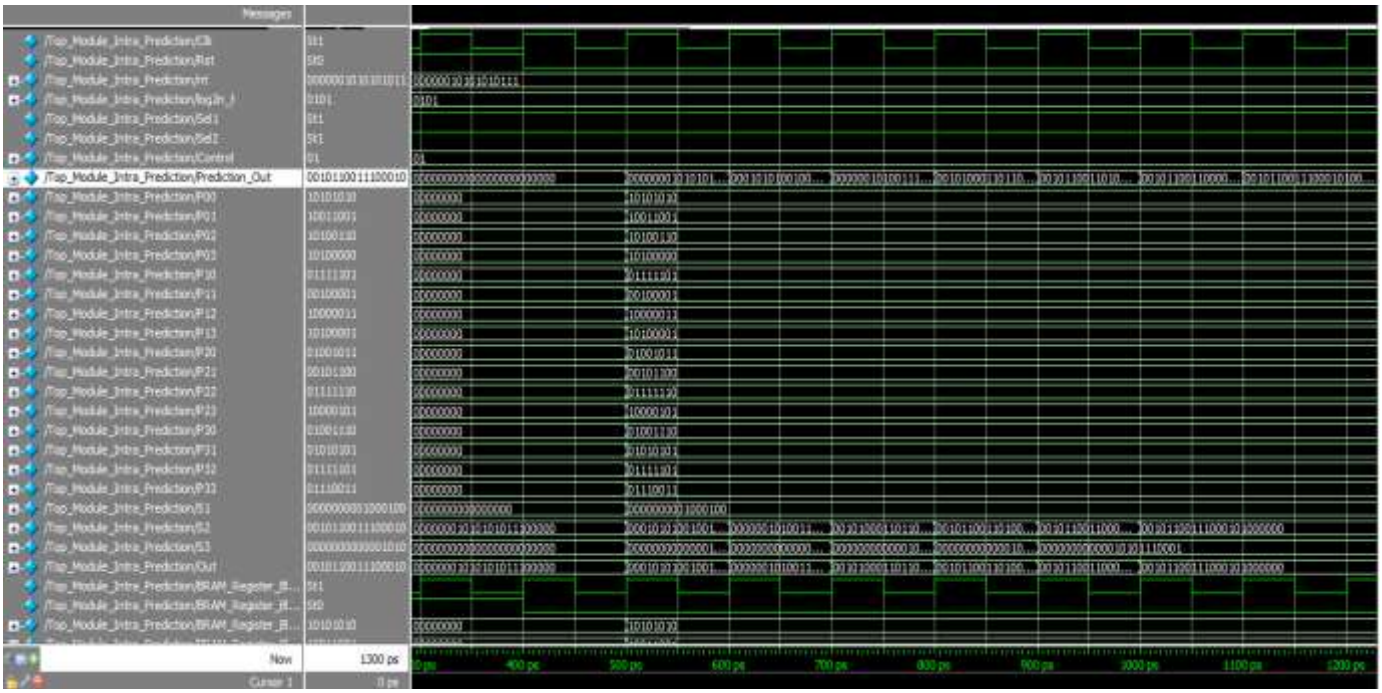

Fig. 8. Simulation Results for 4 X 4 Pixels.

REFRENCES

[1]. Chao-Tsung_Huang and Anantha P.Chandrakasan, "Memory-Hierarchical and Mode-Adaptive HEVC Intra Prediction Architecture for Quad Full HD Video Decoding", IEEE transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 7, July 2014.

[2]. Muhammad Usman Karim Khan, Muhammad Shafique, Mateus Grellert and Jörg Henkel, "Hardware-Software Collaborative Complexity Reduction Scheme for the Emerging HEVC Intra Encoder", Proceedings of Automation & Test in Europe Conference & Exhibition, 2013.

[3]. Jani Lainema, Frank Bossen, Woo-Jin Han, Junghye Min, and Kemal Ugur, "Intra Coding of the HEVC Standard", IEEE transactions on Circuits and Systems for Video Technology, vol. 22, no. 12, December 2012.

[4]. Grzegorz Pastuszak and Andrzej Abramowski, "Algorithm and Architecture Design of the H.265/HEVC Intra Encoder", IEEE transactions on Circuits and Systems for Video Technology, vol. 26, no. 1, January 2016.

[5]. W. Jiang, H. Ma, and Y. Chen, "Gradient based Fast Mode Decision Algorithm for Intra Prediction in HEVC", Proceedings of 2nd International Conference on Consumer Electronics, Communications and Networks (CECNet), pp. 1836–1840, 2012.

[6]. M. U. K. Khan, M. Shafique, M. Grellert, and J. Henkel, "Hardware Software Collaborative Complexity Reduction scheme for the emerging HEVC Intra Encoder", Proceedings of Design, Automation & Test in Europe Conference & Exhibition, pp. 125–128, 2013.

[7]. Vivienne Sze, Madhukar Budagavi and G. J. Sullivan, "High Efficiency Video Coding (HEVC) Algorithms and Architectures", Springer Cham Heidelberg New York Dordrecht London, 2014. Abdessamad. El Ansari, Ali. Ahaitouf, Anass. Mansouri, "An Efficient Hardware Architecture of Intra Prediction in HEVC Standard", Proceedings of 11th International Design & Test Symposium (IDT), pp. 319-322, 2016.

[8]. R.P.P. Singh, Praveen Kumar and Balwinder Singh, "Performance Analysis Of Fast Adders Using VHDL", Proceedings of International Conference on Advances in Recent Technologies in Communication and Computing, pp. 189-193, 2009.