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Expanded Noise Margin 10T SRAM Cell using Finfet Device

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Abstract : Static random access memory (SRAM) cells are being improved in order to increase resistance to device level changes and satisfy the requirements of low-power applications. A unique 10-transistor FinFET-based SRAM cell with single-ended read and differential write functionality is presented in this study. This cutting-edge architecture is more power-efficient than ST (Schmitt trigger) 10T or traditional 6T SRAM cells, using only 1.87 and 1.6 units of power respectively during read operations. The efficiency is attributable to a lower read activity factor, which saves electricity. The read static noise margin (RSNM) and write static noise margin (WSNM) of the proposed 10T SRAM cell show notable improvements over the 6T SRAM cell, increasing by 1.67 and 1.86, respectively. Additionally, compared to the 6T SRAM cell, the read access time has been significantly reduced by 1.96 seconds. Utilising the Cadence Virtuoso tool and an 18nm Advanced Node Process Design Kit (PDK) technology file, the design's efficacy has been confirmed. For low-power electronic systems and next-generation memory applications, this exciting 10T SRAM cell has a lot of potential.

Keywords: FinFET, low power, SRAM, stability, I_{on}/I_{off} ratio, Noise margin.

I. Introduction

Because of the growing popularity of portable electronics like PDAs, iPods, video games, and cell phones, low-power products are being developed at a breakneck pace. System on a chip (SoC) device density and performance have both increased dramatically as a result of process technology scaling. CMOS technology scaling, on the other hand, is fraught with challenges owing to advances in the fields of material and process technology (Frank et al., 2001). There are several issues that develop with scaling the CMOS technology beyond 45nm. These issues include: drain-induced barrier lowering (DIBL), sub-threshold leakage, gate dielectric leakage. These conditions cause leakage current to increase, which increases power consumption and decreases reliability (Farkhani et al., 2014).

FinFET transistors have been substituted for CMOS devices to address these concerns (King,2005) (Jain & Tomar,2022). In terms of switching speed and current density, the FinFET is a superior choice because it is non-planar. As opposed to CMOS devices, it has a lower supply voltage and a smaller leakage current.

Tayade and Lahukar (2022) suggested that Graphene could be used in a FET device for low power applications. Ensan et al. (2019) looked at a FinFET-based 7T SRAM cell that had better WSNM and performed well. To do this, during the write operation, the feedback path in cross-coupled inverters was taken away. Yang et al. (2015) looked into a 9T SRAM topology that was based on 22-nm FinFETs. The read performance of the cell gets better because it uses less power and takes up less space. Also, the hold power is kept to a minimum by cutting down on the leakage current below Vth. Chang et al. (2017) made a 6T SRAM cell at 7nm FinFET technology and simulated it. In this paper, the authors used a flying BL (FBL) and double WL (DWL) design to reduce the effect of the RC wire load on performance. All of the pull up, pull down, and access transistors in this cell are the same size so that they take up the least amount of space.

Guler and Jha (2019) proposed a 3-Da FinFET-based 8T SRAM cell that is all one piece. The authors of this cell used p-FinFETs as access transistors to get a small leakage current and good use of space. As pull-up transistors, independent-gate p-FinFETs also improve the cell's ability to write. In 2012, Ramakrishnan and Srinivasan carried out the soft error analysis of the double-gate common and independent FinFET-based 6T-SRAM cell. Independent gate devices perform much worse than common gate devices in terms of soft error performance. While the read/write stability of this cell has not changed, the access time has dropped. Leakage current was decreased by using an aid circuit. Turi and Delgado-Frias (2017) reported a FinFET-based 8T SRAM cell at full-Vdd and close to threshold

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with a shorted gate (SG) FinFET design. In this cell, read FinFETs with an SG configuration improve performance while reverse biassed inverter FinFET back gates cut down on leakage current. Kulkarni et al. suggested a novel Schmitt Trigger (ST)-based 10T SRAM cell with enhanced read and write stability in 2007. At lower supply voltages, this cell's data retention performance also increases.

Karamimanesh et al. (2021) wrote about a strong 12T-SRAM cell that uses less power. It stays stable at high frequencies and works well enough. A new technique that replaced the write bit-line during the write operation with supply voltage and control signals was used. When the size of a device gets smaller, things like short channel effects (SCE) happen, which have a big effect on how well it works when the supply voltage is low. Figure 1 shows how the threshold voltage changes as the width of the transistor gets bigger. It's interesting to see that as the width of a transistor grows, the threshold voltage goes up by 8–10% at 45nm CMOS technology node. Both Sachdeva (2021) and Santosh G. et al. (2023) it may have happened because of the opposite of the narrow width effect, which happens when the width of the transistor grows in the narrow width region. In 2011, Zhou J. et al. investigated how an inverse narrow width affected the threshold voltage at several technology nodes with various supply voltages. The threshold voltage was found to rise as transistor width shrank and practically hold steady as transistor width rose above 500 nm. In view of the aforementioned facts and difficulties, a 10T SRAM cell based on FinFET has been constructed and simulated to improve read stability while reducing power consumption. The simulation findings are contrasted with those of conventional FinFET-made 6T and 10T SRAM cells.

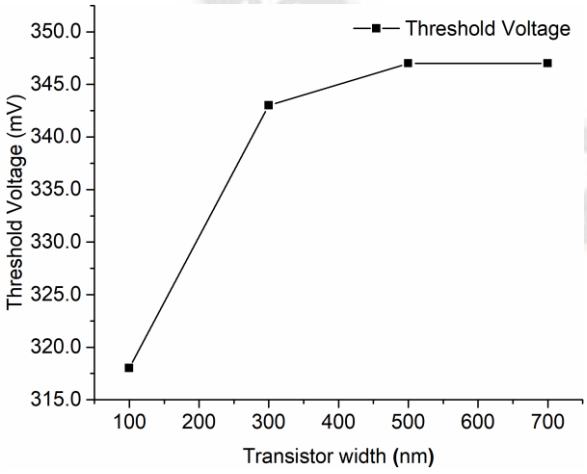

Figure 1. Threshold voltage versus transistor width plot (Sachdeva and Tomar 2021)

Table 1. Bit-cell topologies were taken into account for comparison

Cell features	10T SRAM cell with Low Power FinFET technology	FinFET based ST10T SRAM Cell (Kulkarni et al.,2007)	FinFET based 6T (A. Pavlov and Sachdev, 2008)
Read/Write mode	Differential, Single-Ended	Differential/ Differential	Differential/ Differential
Read/write bit-lines	3-BL/BLB/RBL	2-BL/BLB	2-BL/BLB
Control Signal	3-WL/RD/VGD	1-WL	1-WL

Novelty

This work introduces a ground breaking 10-transistor (10T) FinFET-based SRAM cell, designed to adapt to device-level changes and cater to low-power applications. The cell features single-ended read and differential write functions, ensuring versatility and efficiency. Impressively, it consumes only 1.87 and 1.6 units of power during read operations, outperforming the ST 10T and conventional 6T SRAM cells. Reduced activity during readings results in the power savings. The read and write static noise margins show notable improvements as well, increasing by 1.67 and 1.86 respectively when compared to the 6T SRAM. Additionally, a notable 1.96 reduction in read access time is made. Its effectiveness has been validated using the Cadence Virtuoso tool and 18nm PDK technology. In terms of next-generation memory and low-power electrical devices, this revolutionary SRAM cell shows considerable promise.

II. Materials and Methods

Schematic and Operation of a FinFET-Based 10T SRAM Cell

Figure 2 depicts the configuration of the FinFET-based 10T SRAM cell. The core latch's transistors PM1, PM2, NM1, and NM2 give it a 6T SRAM cell-like appearance. Access transistors NM3 and NM4 are coupled to both the BL and BLB bit lines, whereas NM5 and NM6 transistors are arranged in series with NM1 and NM2 transistors. By controlling the NM5 and NM6 transistors' gate terminals with both BL and BLB bit lines, loops are effectively broken. The proposed 10T SRAM cell includes a separate read port that is segregated from the access transistors to ensure greater Read Static Noise Margin (RSNM) without sacrificing write capability. Additionally, optimised loop-cutting transistor sizes lead to improved Write Static Noise Margin (WSNM). Further enhancing the cell's performance, a virtual ground signal (VGD) significantly reduces bit-line leakage current during a hold operation.

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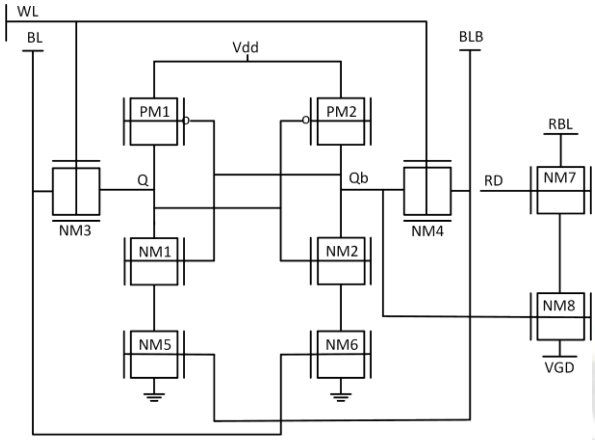

Figure 2. Schematic of a 10T SRAM Cell Based on FinFET

For the FinFET-based 10T SRAM cell, Table 2 details the precise state of the control signals in the read, write, and hold off operation modes. When in read mode, both bit-lines are already set to logic "1," and control signals like WL (Word Line) and RD (Read) are connected to logic 0 and logic 1, respectively.

Table 2. Status of the 10T FinFET-based SRAM cell's control signal

Signals	Operation read	Specify "1" in writing	write the number "0"	Hold state
RD	V_{dd}	GND	GND	GND
WL	GND	V_{dd}	V_{dd}	GND
VGD	GND	V_{dd}	V_{dd}	V_{dd}
BL	V_{dd}	V_{dd}	GND	V_{dd}
BLB	V_{dd}	GND	V_{dd}	V_{dd}
RBL	V_{dd}	GND	GND	V_{dd}

The VGD signal remains at logic 0 throughout a read operation. The data kept in the cell can be read via the read bit line (RBL) signal. The data value kept at storage node "Q" determines the condition of the RBL signal. The read logic '0' action is depicted in Figure 3. The initial assumption is that node Q stores the logic value "0" and node QB stores its complement. This activates the transistor NM8 and provides a drain path for the RBL and VGD signals. It returns a logic '0' to the RBL node. The transient waveforms in Figure 4 during the read "0" operation display all of the signals' current condition. Transistor NM8 remains in the off state because the gate terminal has a logic "0" in it. The RBL bit line reads "1" because it interrupts the flow of electricity between the RBL and VGD nodes.

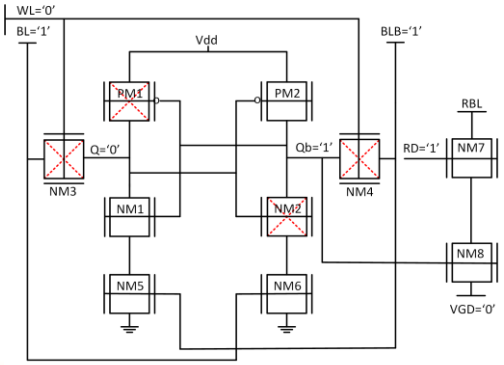

Figure 3. Schematic of a FinFET-Based 10T SRAM Cell for Read '0' Operation

During a write operation, the RD signal remains at logic "0," while the VGD and WL signals are both set to logic "1." The bit-lines are linked to ground (GND) or Vdd depending on the data that needs to be written into the cell. The circuit diagram for the write "1" operation of the FinFET-based 10T SRAM cell is shown in Figure 5. Node Q is initially assumed to contain the logic value "0." To write logic "1" at storage node Q, link bit-lines BL and BLB to Vdd and GND, respectively, as shown in Figure 5.

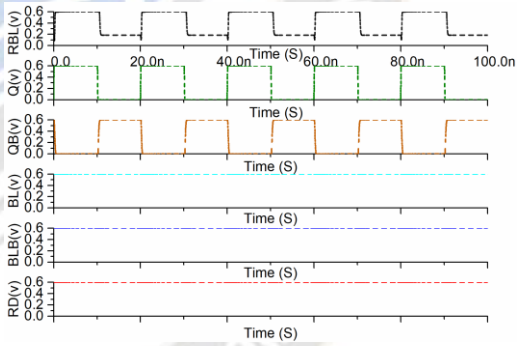

Figure 4. Waveform of a 10T SRAM Cell Based on FinFET Read

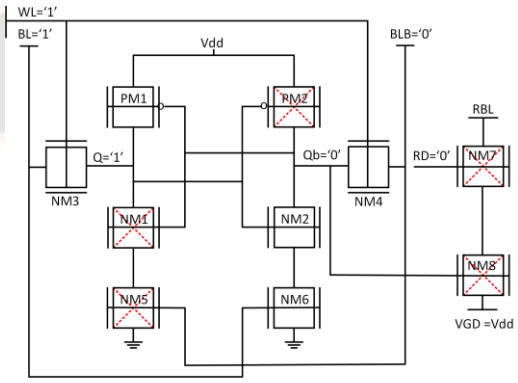

Figure 5. Schematic for a 10T FinFET SRAM Cell with Write-'1' Operation

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The presence of logic "1" on bit-line BL causes transistors NM2 and NM6 to switch on. By providing node QB with a way to discharge, logic "0" manifests there. The write "1" operation in Figure 6's transient waveform shows the current states of all the signals. During the '0' write operation, bit-line BL was connected to GND and bit-line BLB to Vdd. This energises the NM5 transistor and connects node Q to GND. Node Q receives logic 0 as a consequence, and its complement value is shown.

A schematic of the proposed FinFET-based 10 T SRAM cell in hold mode is shown in Figure 7. The VGD signal is connected to Vdd, the read data (RD) control signal is connected to GND. The data remains the same at the storage nodes despite the separation of the NM7 and NM8 transistors. To shorten the wake-up time, both bit-lines are linked to Vdd.

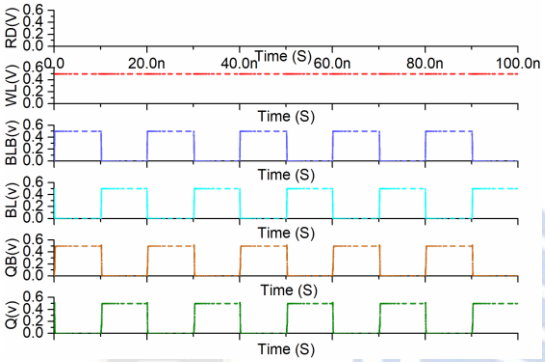

Figure 6. Write Waveform of 10T SRAM Based on FinFETl

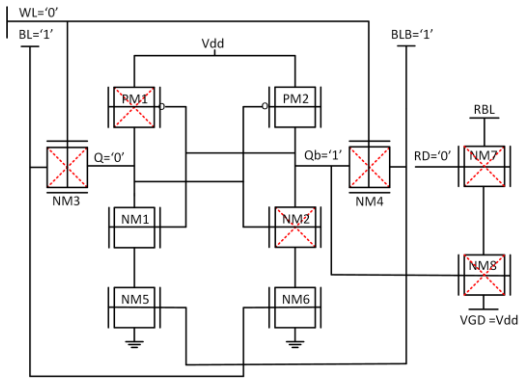

Figure 7. Schematic of FinFET Based 10T SRAM Cell for Hold Operation

Simulation Set-up

Simulations of the proposed FinFET-based 10T SRAM cell and the cells under consideration are performed using Cadence Spectre and an 18-nm advanced node PDK FinFET technology file. Thus, a fair and accurate comparison between the two cell types can be made. Using a variety of supply voltages from 0.3V to 0.6V, the results are compared and examined. Device size has a significant impact on the SRAM cell's performance in FinFET devices. The thickness of the fins limits the effect of the electric field as it travels from the drain to the source. With a reduction in fin thickness and an increase in threshold voltage, the quantum confinement effect becomes evident. Performance suffers and the device's consistency is reduced as a result. For the proposed 10T SRAM cell, the pull-up and access transistors require a bare minimum of 1 fin, but the pull-down transistors NM1, NM2, and loop-cutting transistors N5, N6 require a bare minimum of 3 fins. The transistors N7 and N8 are also sized with 3 fins to enhance read characteristics. Table 3 contains the parameters for the 18nm advanced node PDK FinFET technology, which are necessary to ensure accurate analysis and evaluation of the performance of the SRAM cell. In the course of the simulation, this table is consulted.

Table 3. 18-nm FinFET device specifications

1-fin FinFET device specifications	
V_{dd}	0.8V
L_{int}	30 nm
W_{fin}	14 nm
H_{fin}	35 nm
EOT	1.5 nm

III. Results and Discussion

Power dissipation

Recently, people have been paying a lot of attention to power dissipation, and it has become a very important parameter in low power applications.

Most static power loss happens when the device is in "standby" mode. It gets bigger as the size of the feature gets smaller. This is mostly the sum of leakage currents from below the threshold, from the gate, and from the junction. Leakage current is an annoying effect that can be lessened to some extent with leakage reduction techniques. Figure 8 shows the change in read power dissipation as supply voltages change. It's important to note that the read power of the proposed FinFET-based 10T SRAM cell is 1.87 and 1.6 less than that of ST10T and 6T SRAM cells at 0.6V supply voltage, respectively. Also, as Vdd goes down, read power goes down.

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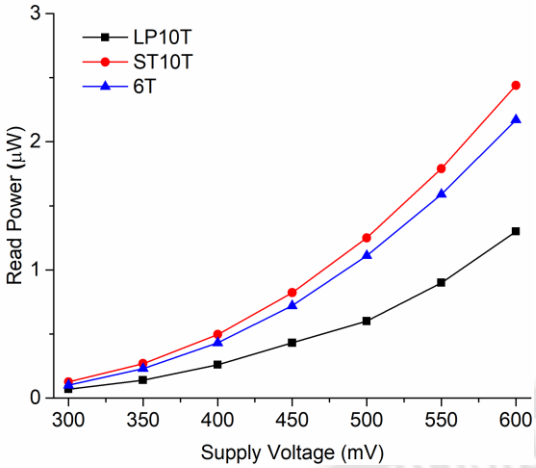

Figure 8. Read Power

The main reason for this drop in power is the single-ended read mode. Read: The ST10T SRAM cell loses the most power of all the cells we looked at. This is because the ST-based inverter circuit lets the voltage at the internal nodes swing more (Kulkarni et al., 2007). Figure 9 shows the write power of simulated topologies with different supply voltages.

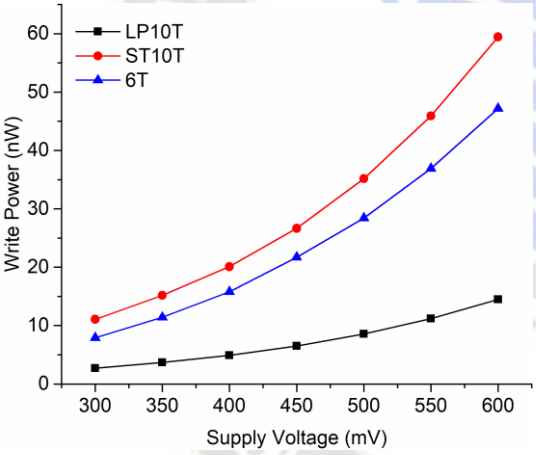

Figure 9. Write Power

It is clear that the write power has dramatically decreased by factors of 4.1 and 3.25, respectively, when comparing the ST 10T/6T SRAM cells running at a 0.6V supply voltage. The loop-cutting technique used, which weakened one of the inverters because of the NM5 and NM6 loop-cutting transistors, can be blamed for the reduction in writing power (Sachdeva and Tomar, 2021). In SRAM cell design, controlling leakage current has become a difficult task as technology nodes continue to get smaller. Static power usage during hold mode results from leakage current passing through multiple transistors. The fluctuations in power leakage with varying supply voltage are shown in Figure 10. This notable improvement can be attributed to the presence of two additional transistors, NM5 and NM6, which are connected in series with NM1 and NM2. This configuration effectively elongates the effective channel, resulting in a higher threshold voltage. As a consequence, the leakage power in the proposed FinFET-based 10T SRAM cell is further reduced.

Read current and I_{on}/I_{off} ratio

The on-state cell current (Ion) is another crucial factor in the design of SRAM cells. The transistors NM7 and NM8, which are employed while the cell is being read, determine the read current in the proposed FinFET-based 10T SRAM cell. Because the SRAM cell's read current (Ion) is higher, it can react quickly.

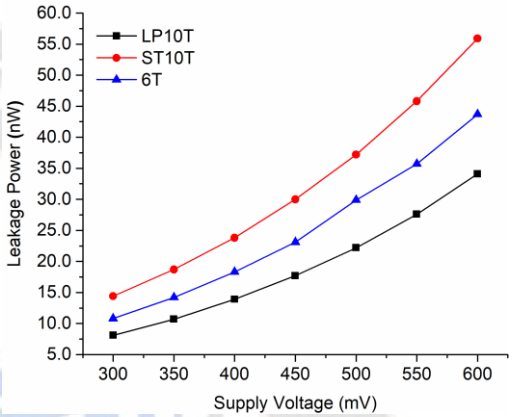

Figure 10. Leakage Power

For reference, Figure 11 displays the computed read current values for various supply voltages in the tested cells. As the supply voltage increases, the advantage in read current grows more linearly. The intended FinFET-based 10T SRAM cell reads data by directly measuring the current in each bit cell using a current sense amplifier. Figure 12 also shows the Ion/Ioff ratio for each of the investigated cells. Notably, the proposed 10T cell stands out among all the studied cells with the highest Ion/Ioff ratio. This result is enabled by the enhanced Ion/Ioff performance and low bit-line leakage current of the recommended cell.

Additionally, the Ion/Ioff ratio of the proposed 10T SRAM cell is 1.4/1.18 higher than that of ST 10T/6T SRAM cells. This indicates that an array with more bit cells can be created using the suggested FinFET-based 10T SRAM cell.

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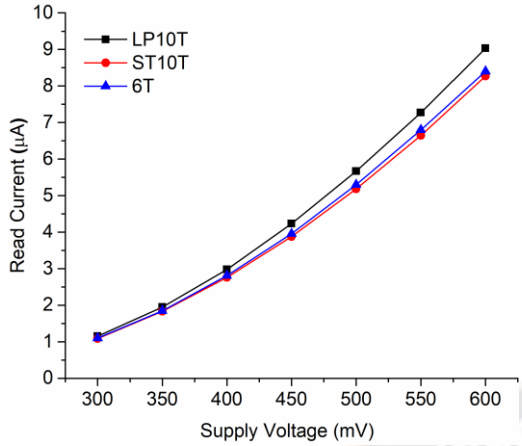

Figure 11. Read Current

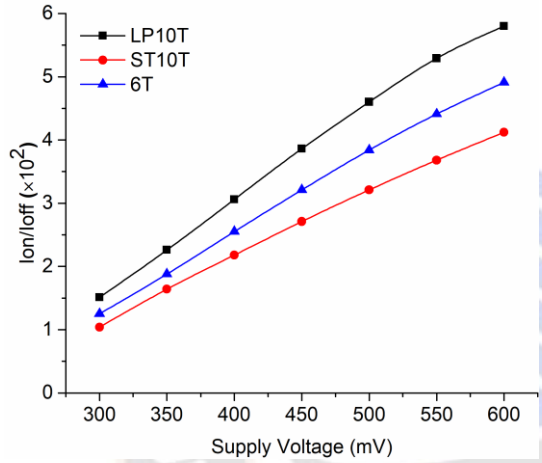

Figure 12. I_{on}/I_{off} Current

Write/Read lag

The read/write delay or access time of an SRAM cell is used to gauge its performance. The read access time in a single-ended SRAM cell refers to how long it takes for the pre-charged read bit-line to drop to 50 mV once the RD signal is activated. The read access time for a differential SRAM cell refers to the amount of time needed to fully discharge one of the bit lines, leaving a noticeable space between it and the other bit line once the read word line signal has been engaged. Figure 13 shows how changes in supply voltage affect read delay for the simulated topologies.

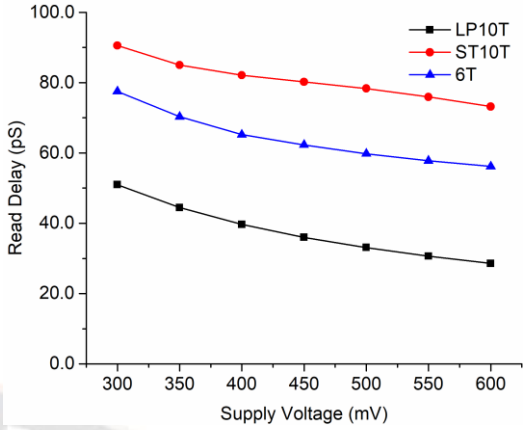

Figure 13. Read Delay

Similar to the decrease seen in ST 10T and 6T SRAM cells, it is expected that the proposed FinFET-based 10T SRAM cell's read access time will be cut by a factor of about 2.56/1.96. The duration of the read bit line's discharge after going via transistors NM7 and NM8 determines this. The proposed cell's read latency is also the shortest of all the simulated cells, and it gets shorter as the supply voltage rises. This might be as a result of the 10T SRAM cell with FinFET's higher read current. The size of the access and pull-up transistors affects how quickly an SRAM cell can be written to. In this study, pull-up and access transistors use the same amount of fins.

Whether the mode of operation is single-ended or differential has an impact on the write access time as well. Figure 14 illustrates how changing the supply voltages affects the write access time. Comparing the proposed cell's write access time to ST 10T/ 6T SRAM cells with a 0.6V supply voltage, the difference is 1.59/1.7. The 10T SRAM cell built on FinFET breaks the loops in such a way that it results in this. Even if the write operation was performed using differential structure in both topologies.

Product for Power Delay

The accuracy of the predicted power delay product (PDP) determines an SRAM cell's performance. A comparison of the Read PDP for simulated topologies at various voltages is shown in Figure 15. Figure 15 demonstrates that, of all the SRAM topologies examined, the proposed FinFET-based 10T SRAM cell has the lowest read PDP.

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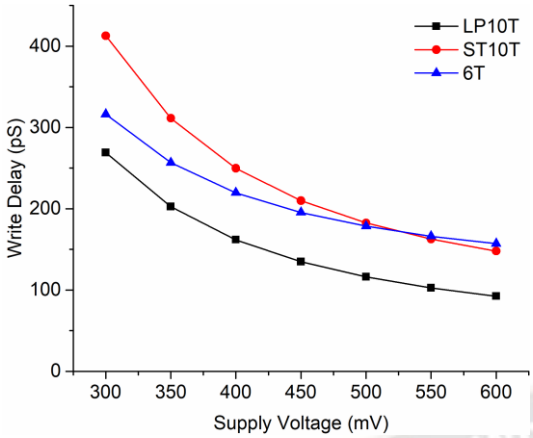

Figure 14. Write Delay

Compared to ST 10T/6T SRAM cells with 0.6V supply voltage, this is 4.8/3.27 less. It happens because the read bit-capacitance line's and swing voltage drop. Figure 16 shows the sum of the write power delay times all the topologies that were simulated.

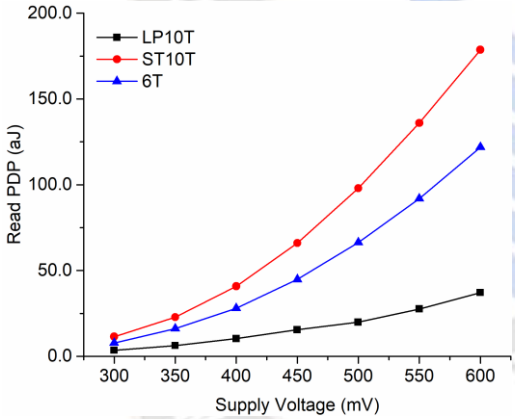

Figure 15. Read Power Delay Product

FinFET-based 10T SRAM cell is 8.27/5.56 less than in ST 10T/6T SRAM cells. Also, in the proposed cell, WPDP is the lowest of all the cells that were looked at. It occurs as a result of the planned 10T SRAM cell's quicker write time and lower write power.

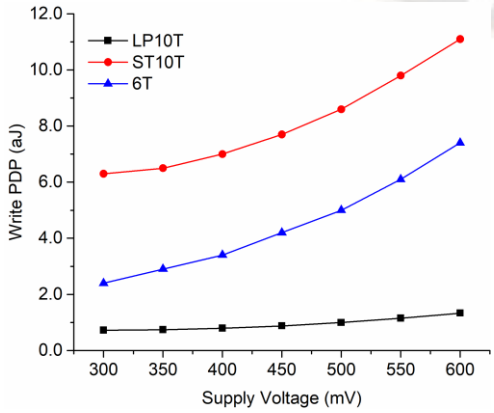

Figure 16. Write Power Delay Product

Stability

Scaled technologies increasingly expose the stability of SRAM cells to process variations. This stability is quantified by the static noise margin (SNM), which estimates the amount of noise required to flip a stored bit on a node. Conventional 6T SRAM cells have a propensity to be less stable at lower supply voltages as a result of competing access transistors. To increase stability when reading, the recommended FinFET-based 10T SRAM cell incorporates a read decoupled topology. As seen in Figure 17, the model of curve butterfly is used to evaluate how well each cell reads. The Read Static Noise Margin (RSNM) is calculated as the length of a side of the greatest square that can fit between the two curves. This technique offers a complete assessment and performance in the presence of process variations.

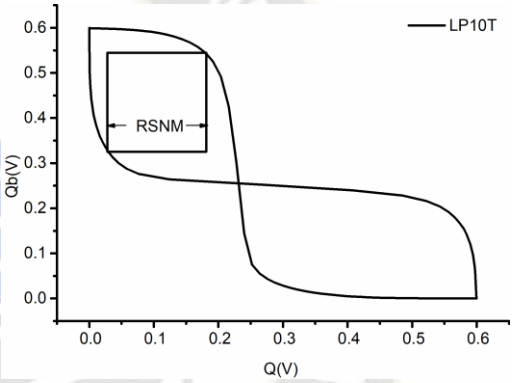

Figure 17. Read Mode VTC of FinFET Based 10T Cell of SRAM

Figure 18 demonstrates that of all the cells examined, the suggested FinFET-based 10T SRAM cell has the highest read SNM. This is as a result of the read decoupled structure that is employed when reading the cell. The 10T cell's RSNM is 1.67 greater at 0.6V than the 6T SRAM cell's. The read buffer transistors must be strengthened to get the greater RSNM.

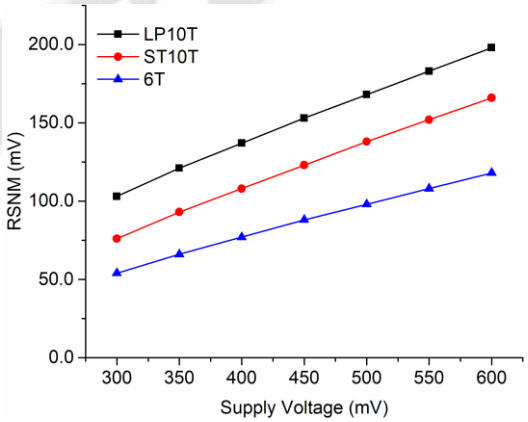

Figure 18. Read SNM

The pull-up ratio of an SRAM cell, which must be less than 1 in order for a write operation to function, determines the cell's WSNM. The WSNM is calculated using the read voltage

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transfer characteristics (RVTC) and write voltage transfer characteristics (WVTC) curves. The voltage is changed from 0 to Vdd at node Q, followed by storage node Qb to provide the read transfer characteristic curve. Additionally, by varying the voltage at storage node QB from 0 to Vdd and then tracing it to storage node Q, the write transfer characteristic curve is discovered. The WSNM is calculated using the side length of the square that can be cut between the RVTC and WVTC curves. The WSNM curve of the FinFET-based 10T SRAM cell is depicted in Figure 19.

To lessen the likelihood that the pull-down and read buffer transistors may split the VGD signal, the signal is maintained at a logic high level. The gates of the NM3 and NM4 transistors are connected to the bit-line potential. In the proposed FinFET-based 10T SRAM cell, a voltage divider is generated between the pull-down and read buffer transistors, making writing difficult. The VGD signal has been held at a logic high to prevent this issue from getting worse. The WSNM of simulated topologies is displayed in Figure 20. A ST 10T/6T SRAM cell's WSNM is 1.58/1.86 larger than that of a FinFET-based 10T SRAM cell.

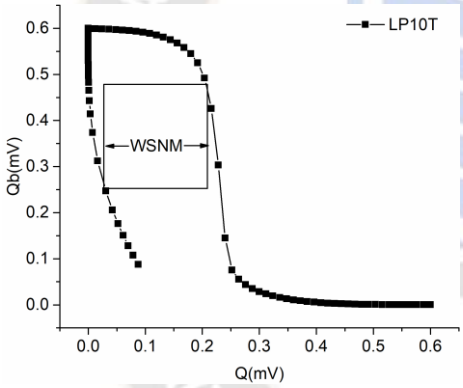

Figure 19. Write Mode VTC of FinFET Based 10T SRAM Cell

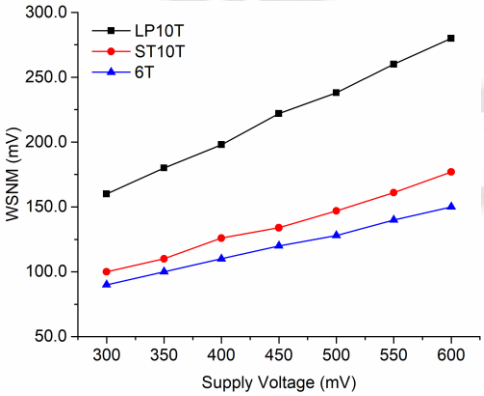

Figure 20. Write SNM

Soft errors

In SoC devices, SRAM arrays are made up of a lot of cells with a lot of circuitry. As the supply voltage goes down, the amount of charge stored on the internal data nodes gets smaller, which may make it more likely that the chip will fail. Alpha particles go through the silicon wafer and change the charge at the storage nodes of the SRAM cell. This makes charged particles like electron-hole pairs. This caused the data in the SRAM cell to flip, which is called a "soft" error (or single-event-upsets). The error-correcting codes method is used to solve the soft error problem. In this method, redundant SRAM cells are added to each word, which makes encoding, detection, and correction take longer (Tomar and Sachdeva, 2022). Also, soft errors can be less of a problem if technology is improved so that the distance between transistors gets shorter and the storage node area gets smaller (Chatterjee et al.,2014).

Table 4 shows a summary of the simulation results for all the SRAM cells that were looked at with a supply voltage of 0.6V. Table 4 shows that the proposed FinFET-based 10T SRAM cell reduces the amount of power it uses and improves its performance. When compared to other cells, the RSNM of the cell is also improved by a large factor. When reading or writing to a FinFET-based 10T SRAM cell, three bit-lines are used. This makes it more complicated. Also, as the number of transistors goes up, it takes up a lot more space. These are the things that hold the work back.

Table 4. Analysis of various proposed and taken into consideration cell parameters using 18nm FinFET technology

Parameters/Topologies	Low power FinFET-based 10T (LP10T)	FinFET based ST10T SRAM Cell	FinFET based 6T (A. Pavlov and
Supply Voltage (V_{dd})	0.6V	0.6V	0.6V
Read current (□A)	9.03	8.27	8.4
Read Power(□W)	1.3	2.44	2.17
Write Power(nW)	14.5	75.7	47.2
Leakage Power(nW)	34.1	55.9	32.9
I_{on}/I_{off} Ratio ($\times 10^2$)	5.8	4.12	4.91
Read Delay(pS)	28.54	73.21	56.16
Write Delay(pS)	92.4	147.81	157.08
Read SNM (mV)	198	166	118
Write SNM(mV)	280	177	150
Read PDP (aJ)	37.102	178.6324	121.8672
Write PDP(aJ)	1.33	11.1	7.4

IV. Conclusion

This article looked at low power 10T FinFET-based SRAM's read/write stability, read/write power, read/write access time, read/write power, power delay product, and Ion/Ioff ratio. Loop cutting has been employed to enhance the cell's capacity for writing, while read decoupled structure has been used to enhance read stability. Additionally, it has been demonstrated that a single-ended read operation lowers the read power. The high Ion/Ioff ratio in the proposed FinFET-based 10T SRAM cell illustrates the high bit cell density. The RDP for all cells is

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lower when the read access time is quicker and the read power is lower. The proposed FinFET-based 10T SRAM cell, in conclusion, might be the best option for low power applications.

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