*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
***Article Received**: 02 January 2023 **Revised**: 29 January 2023 **Accepted**: 18 February 2023*

# Design and Analysis of Multiplexer based Approximate Adder for Low Power Applications

**RamakrishnaReddy Eamani[1], N. Vinodh Kumar[2]**
[1]Research Scholar Department of Electronics and Communication Engineering,
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology ,
Avadi, Chennai 600062, India,
erkrishnareddy.phd@gmail.com
[2]Associate Professor, Department of Electronics and Communication Engineering,
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology,
Avadi, Chennai 600062, India,
vinodhkumar.cc@gmail.com

**Abstract**— Low power consumption is crucial for error-acceptable multimedia devices, with picture compression approaches leveraging various digital processing architectures and algorithms. Humans can assemble useful information from partially inaccurate outputs in many multimedia applications. As a result, producing exact outputs is not required. The demand for an exact outcome is fading because new innovative systems are forgiving of faults. In the domain where error-tolerance is accepted, approximate computing is a new paradigm that relaxes the requirement for an accurate modeling while offering power, time, and delay benefits. Adders are an essential arithmetic module for regulating power and memory usage in digital systems. The recent implementation and use of approximate adders have been supported by trade-off characteristics such as delay, lower power consumption. This study examines the delay and power consumption of conventional and approximate adders. Also, a simple, fast, and power-efficient multiplexer-based approximate adder is proposed, and its performance outperforms the adders compared with existing adders. The proposed adder can be utilized in error-tolerant and various digital signal processing applications where exact results are not required. The proposed and existing adders are designed using EDA software for the performance calculations. With a delay of 81 pS, the proposed adder circuit reduces power consumption compared to the exact one. The experiment shows that the designed approximate adder can be used to implement circuits for image processing systems because it has a smaller delay and uses less energy.

**Keywords**- Approximate Computing; Error-tolerance; Approximate Adder; Mulitiplexer; Low Power Circuits.

## I. INTRODUCTION

The main driving forces behind the development of standard VLSI architecture and innovative implementation methods are the constantly rising performance demand and application complexity [1]. Hard computing always adheres to stringent accuracy standards, regardless of the applications. The cost of implementation rises due to the need to maintain precision throughout the design; new, emergent applications face significant difficulties. Arithmetic circuits serve as the fundamental building blocks of all computing systems. Recently, various dynamic machine learning and CNN algorithms have used resource-constrained, low-power devices such as edge sensors and embedded processors [2]. Our human visual and auditory systems can typically overlook minor imperfections. Hence, precise computing is only sometimes necessary for various digital system applications, such as voice, image, and text processing. Also, because of the data volume and the calculation's complexity, digital systems for multimedia applications are incorporate with deep learning model which require more circuit area and power. One of the simplest ways to reduce computational complexity and energy consumption is by using approximate computing techniques [3].

Efficiency and energy usage are key considerations in the design of digital circuits. The energy-consuming parts of digital architectures are adders, which is the basic building blocks of arithmetic circuits like dividers and multipliers. As a result, creating an effective adder improves the effectiveness of a digital system as a whole [4]. Several traditional methods of low-power implementation, including power gating, various transistor technology, and clock gating, have been thoroughly researched. Researchers have recently paid much attention to approximate computing design and its consequences for energy-efficient architecture. For ever-expanding error-tolerant applications like big data, and pattern matching, approximate computing offers a low-power solution. These applications do not rely on a specific solution but rather accept a collection of approximations due to the user's constrained perceptual senses and the noise of real-world data [5, 6].

Whereas speed requires additional power and size with accurate computing, precision is surrendered for energy and speed in approximate computing. Moreover, circuits are

*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
*Article Received: 02 January 2023 Revised: 29 January 2023 Accepted: 18 February 2023*

increasingly susceptible to specification change with applied voltage. The device density increased due to the development of process technology at the scaling range. Hence, designing fault-free computations circuits for today's heavy workloads rather inefficient [7]. Instead of considering the error-resilient for the discrete signal input, prior research on approximate adders has mainly tried to reduce the critical path of the carry output by decreasing errors.

As a result, this form of approximate computing is advantageous in energy, resource utilization, especially for image processing applications like CNN, where precise computation is not required [8]. The delay, area, and power consumption decrease using erroneous computing circuits. Based on this concept, various approximate adders and multiplier circuits [9, 10] have been discussed in the article for deep learning, image, and digital signal processing. Only adequate results are needed for the many error-resistant applications employed in smart city components to analyze the data. Devices with tiny chip sizes, efficient and faster processing speeds are needed for health care, mobility, medical facilities, intelligent cities, advanced devices, etc.

The new application is focused on something other than accuracy and deterministic calculation. Hence, approximation computing is the solution to all these issues. It allows greater performance at a negligible expense. These systems need an effective mechanism that satisfies the goals of speed, delay, and power to complete the mission. A prospective architectural strategy called approximate computing creates new opportunities for designing circuits that are smaller, faster, and consume less energy also sacrificing accuracy for real-time.

The usage of approximation circuits is appealing for applications like artificial intelligence and CNN architecture, which can be built to tolerate mistakes. The three distinct groups of error-tolerant circuits are as follow as:

a) Circuits that can withstand error to a certain point before their behavior starts to deteriorate, such as artificial intelligence.

b) Applications that cannot programs like image processing use systems whose performance deteriorates as error levels rise.

c) Applications to internal error resilient techniques, like the logic system, can quickly absorb many mistakes.

The paper focuses on the approximate computing of Adder circuits for low-power applications to reduce power consumption and increase performance. The following sections make up the structure of the paper: The paper's introduction is shown in Section 1. Part 2 presented a review of the related work in approximate computing. Section 3 provides the proposed adder and conventional adder design. The simulation results and analysis are discussed in Section 4. Sections 5 outline the conclusion and the potential future application.

## II. RELATED WORK

Approximate adders are a crucial component of arithmetic circuits in approximate computing. Certain combinations of inputs result in inaccurate sum and carry outputs from approximate adders, whereas other input combinations result in accurate sum and carry outputs. As a result, the system's hardware requirements for approximate computation are lowered. As a result, the architecture uses approximation computation to produce high speed and low power consumption. Yet, if correct results are not critical, approximation computing is an appropriate option for DSP applications, including video, picture, and audio processing. To lower the design's power consumption, adders are implemented using various digital CMOS technologies, including transmission gates; pass transistor logic, and double-pass transistor-based adder circuits. For error-tolerant applications, the error design performance to reduce design parameters like transistor and power consumption and to increase accuracy, tolerant adders and other arithmetic full adders have been proposed in the past. The performance of various types of approximate adders was examined based on the performance metrics. Different approximate adder techniques are analyzed in Honglan Jiang et al. [11].

The Equal Segmentation Adder provides the more erroneous bit but it required less hardware than other types. The specification related power and circuit delay, approximate adders are contrasted with the ripple carry adder [12]. In Sato et al. [13] proposed approximate adder based on masking of the carry propagation at run time. This adder is used for error-tolerant applications and reduces power and delay. In data mining and multimedia signal processing, approximate adders are used instead of exact adders because they can tolerate error. In order to reduce the amount of hardware needed, a 4-2 compressor tree with OR gates in place of one of the XOR gates were suggested [14]. In applications of image processing, an approximate adder is used to implement multipliers. Algorithmic noise Tolerant schemes are used in soft DSP to compensate for algorithmic performance degradation brought on by input-dependent errors. To enhance the accuracy of the image processing algorithm, approximate computing plays a major role, in that prediction-based error control was proposed. In DCT picture compression, approximate computation was applied [15]. To assess the various metrics, such as delay, energy usage, and PSNR, a collection of images is compressed. The design, implementation, and analysis of precise adders are also done

*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
***Article Received**: 02 January 2023 **Revised**: 29 January 2023 **Accepted**: 18 February 2023*

in order to maximize power efficiency and minimize hardware requirements.

Utilizing approximate computing, smart devices' computing power can be increased while using less energy. Circuit and system design are facing challenges as a result of the rapidly increasing number of IOT devices. In order to increase efficiency and speed by approximation, there are two different types of approaches. The first one conserves energy by using the Voltage-Over-Scaling technique [16, 17]. The second method relies on redesigning the circuit to approximate the exact circuit. The demand for high-performance systems has increased due to the increase in applications, and these needs are met by approximate circuits. Over the past ten years, various methods have been used to redesign arithmetic blocks. Two numbers are added together using adders; the most popular adders are ripple carry adders and carry look-ahead adders. As a nearly perfect adder, speculation adders [18] were suggested to reduce critical path delay using LSBs foretell carry.

The equal segmented adder consists of a small number of sub-adders. In this all sub adders executed in parallel manner with a fixed number of inputs [19]. Because carry and sum are two distinct blocks, error-tolerant adder version II suggests an improvement over the previous [20]. The partial sum in the accurate reconfigurable approximate adder is treated as MSBs. Errors in the circuit is corrected using a separate error detection and correction system [21]. A multiple bit adder circuit is separated into sub adders by a dithering main block. Pass transistors logic based on XOR/XNOR gates were used to improve this in approximate complete adders [22].

In [23] authors developed imprecise computing model like adder, multiplier, and divider that were inspired by biological systems on the other end of the spectrum. The lower-part OR gate separates p bits into two m-bit and n-bit units is a type of imprecise adder. A precise value for m in MSB is calculated by p-bit adder. N bits are approximately calculated using the OR gate. In order to create a smaller and speedier circuit, BAM splits CSA array and leaves out the logic. In order to enhance rectification and debugging, [23] describe a method for adding LUT to the circuit. A LUT-based approximate circuit with intended error was put up by [24] in 2020. Based on a random and algorithmic model, LUT insertion is performed. The approximate adder suggested in [25] includes both an accurate and an incorrect sub-adder and can be implemented using FPGA and ASIC.

The static approximation of the approximate adders explained up to this point includes pre-fixed sizes for the accurate and inaccurate sub-adders, and this can be adjusted in accordance with an application. However, there is another class of approximate adders that includes a dynamic approximation, allowing the level of approximation to be adjusted as needed. Moreover, depending on the necessity, outputs may be produced that are roughly or precisely accurate. Dynamic approximate adders contains additional carry prediction and control units circuits to be able to provide approximate or accurate outputs as needed, are covered in references [26]. These additional designs would require more resources (LUTs) when built on an FPGA together with the approximation adder logic, which would result in worse design metrics than the native accurate FPGA based adder. Hence it is in need of designing an approximate adder for low power application like image processing and digital signal processing applications.

## III. THE PROPOSED APPROXIMATE FULL ADDER

In this part, we presented conventional full adder, existing approximate adder and proposed approximate adder circuit design and its operation.

### *A. Accurate Full Adder*

The schematic circuit diagram of conventional adder shown in Figure 1. The conventional full adder consists of 24 transistors. We have considered A, B, C are the inputs and the outputs are sum and carry. The conventional adder is also called as error free adder. The truth table for conventional adder presented in the Table 1.

### *B. Approximate Full Adder*

Upcoming architectures and improvements now depend heavily on approximate computing [27]. This is accomplished using approximate computation, which forgoes precision in favor of speed. The exact computations, which were previously the main use of computers, may seem paradoxical. The schematic circuit diagram of existing approximate adders is shown in Figure 2. In the existing approximate adder consists of only 11 transistors for performing sum and carry operation. This approximate adder produces one erroneous bit in carry output and three erroneous bits in Sum. The corresponding truth table for existing approximate adder presented in the truth Table 1. Note that, the output of carry will be considered as the complementary function.

*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
***Article Received**: 02 January 2023 **Revised**: 29 January 2023 **Accepted**: 18 February 2023*

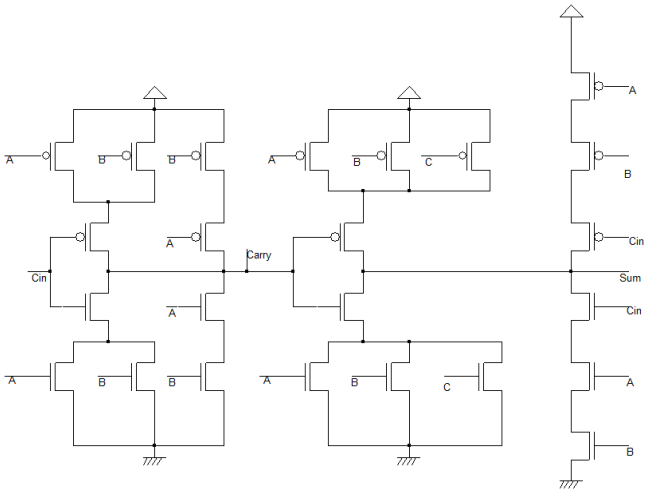


Figure 1. Conventional Adder using CMOS Logic Design

### *C. Proposed Approximate Full Adder*

Simple Gate Diffusion Input (GDI) logic circuits are created with the help of CMOS logic functions. In this technique the PMOS and NMOS substrates are connected to VDD and ground. The drain and source terminal can be used for input logic function based on the nature of circuit. In this work, we developed a simple multiplexer-based approximate adder with help of GDI-CMOS techniques. The proposed approximate adder required only 11 transistors for performing sum and carry operation. Compared with existing approximate adder and conventional adder the proposed adder reduces the transistor count and power dissipation. The proposed adder produces one erroneous bit in carry output and two erroneous bits in Sum. The corresponding truth table for existing approximate adder presented in the truth Table 1.

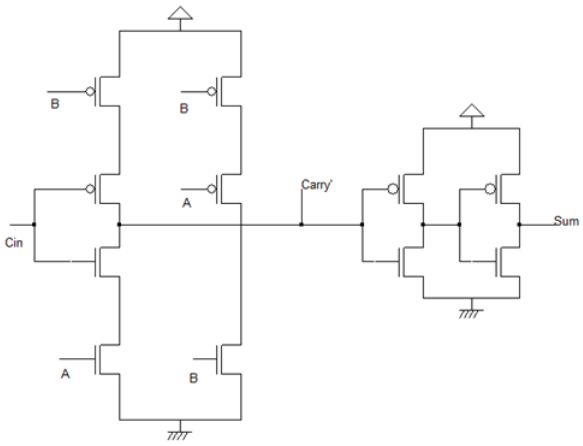


Figure 2. Approximate Adder Using CMOS Logic Design

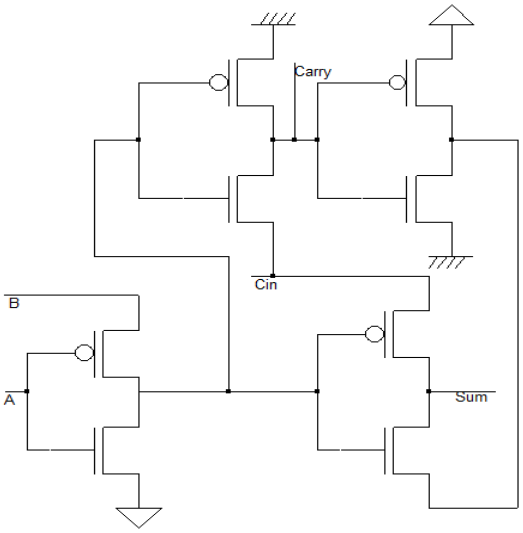


Figure 3. The Proposed Multiplexer-based Approximate Adder using GDI-CMOS Logic Design.

Table 1. The conventional and approximate adder's truth table.

| Inputs | | | Conventional Adder | | Approximate Adder[IMPACT] | | Proposed Approximate Adder | |
|---|---|---|---|---|---|---|---|---|
| A | B | C | Sum | Carry | Sum | Carry | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 | 0✓ | 0✓ | 0✓ | 0✓ |
| 0 | 0 | 1 | 1 | 0 | 1✓ | 0✓ | 1✓ | 0✓ |
| 0 | 1 | 0 | 1 | 0 | 0✗ | 0✓ | 1✓ | 0✓ |
| 0 | 1 | 1 | 0 | 1 | 1✗ | 0✗ | 0✓ | 1✓ |
| 1 | 0 | 0 | 1 | 0 | 0✗ | 1✗ | 1✓ | 0✓ |
| 1 | 0 | 1 | 0 | 1 | 0✓ | 1✓ | 0✓ | 1✓ |
| 1 | 1 | 0 | 0 | 1 | 0✓ | 1✓ | 1✗ | 0✗ |
| 1 | 1 | 1 | 1 | 1 | 0✓ | 1✓ | 0✗ | 1✓ |

The simulation result of proposed adder I shown in figure 4. The simulation results verify that the proposed adder produces only three erroneous bits in both sum and carry output. Hence we can use proposed approximate adder for low power application such as digital signal processing, image processing and multimedia applications.

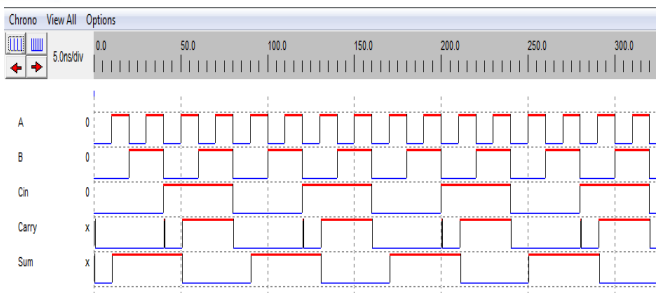


Figure 4. The Proposed approximate adder simulation output using EDA tool.

*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
***Article Received**: 02 January 2023 **Revised**: 29 January 2023 **Accepted**: 18 February 2023*

## IV. RESULTS AND DISCUSSION

The presented approximate adder circuit is designed and performed the simulation analysis using the EDA software tool. The developed approximate adder performance is analyzed with the conventional adder and existing approximate adder. The Comprehensive study on approximate adder with CMOS logic circuits simulation results are presented in Table 2. The proposed approximate adder compared with conventional and existing approximate adder performs well in delay and power.

Table 2. Comprehensive study on Conventional and Approximate Adder

| Logic | Conventional Adder | Approximate Adder [27] | Proposed Approximate Adder |
|---|---|---|---|
| Threshold Voltage | 0.7 | 0.7 | 0.7 |
| Supply Voltage | 1 | 1 | 1 |
| No. of Transistor | 24 | 11 | 8 |
| No. erroneous bits | 0 | 4 | 3 |
| Power Dissipation (µW) | 115 | 67.54 | 25.187 |
| Delay(pS) | 133 | 98 | 81 |

The performance analysis major findings are the multiplexer-based approximate adder offers high speed and low power consumption as shown in Figure 5 and 6.

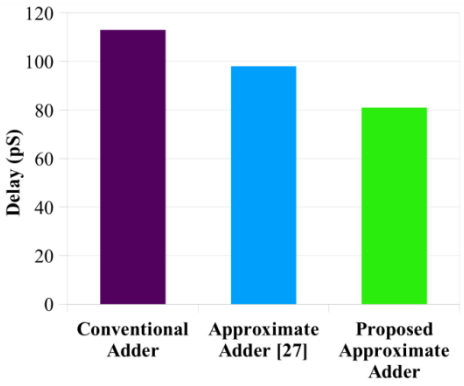


Figure 5. Delay comparison with existing system

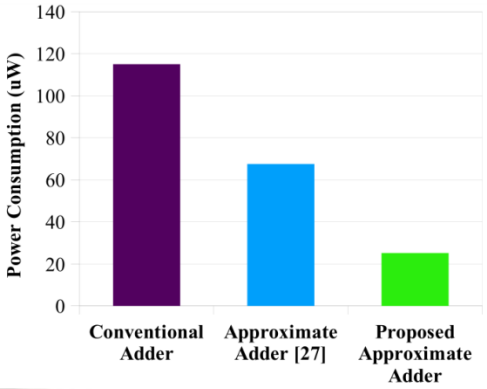


Figure 6. Power comparison with existing system

## V. CONCLUSION

Recently, edge and portable components such as cell phones, embedded systems, and server computers have become a most important concern for low energy consumption and high performance. In this manuscript, low power and hardware efficient multiplexer-based approximate adder is proposed and implemented using GDI logic for low-power applications. An 8T approximate adder is designed and investigated through extensive simulations using the EDA software tool to decrease delay and to be less error percentage. The power supply voltage applied to the adder circuits was 1 V. Experimental results show that the developed adder consumes less power and reduces delay compared with the conventional adder and existing approximate adder. The GDI multiplexer-based approximate adder required only eight transistors which leads to low power and decreases the delay of the sum and carry outputs. The designed multiplexer-based approximate is suitable for error-resilient applications that demand low-power embedded devices.

## ACKNOWLEDGMENT

This article supported by Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology and Usha Rama College of Engineering and Technology. I express my gratitude to Sri Sunkara Ramabrahmam, Chairman of Usha Rama Educational academy and also express my gratitude to my guide Dr.N.Vinodhkumar for his enthusiastic co-operation, valuable suggestions for doing my Research.

## REFERENCES

[1] Lee, Y. H., Kuei, C. H., Kao, Y. Z., & Fan Jiang, S. S. (2021). Algorithm and VLSI architecture designs of a lossless embedded compression encoder for HD video coding systems. Journal of Circuits, Systems and Computers, 30(04), 2130004.

[2] Sasikumar, A., Subramaniyaswamy, V., Jannali, R., Rao, V. S., & Ravi, L. (2022). Design and area optimization of CMOS operational amplifier circuit using hybrid flower

*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 3*
*DOI: https://doi.org/10.17762/ijritcc.v11i3.6341*
***Article Received**: 02 January 2023 **Revised**: 29 January 2023 **Accepted**: 18 February 2023*

pollination algorithm for IoT end-node devices. Microprocessors and Microsystems, 93, 104610.

[3] Chung, Y., & Kim, Y. (2021). Comparison of approximate computing with sobel edge detection. IEIE Transactions on Smart Processing & Computing, 10(4), 355-361.

[4] Hasan, M., Siddique, A. H., Mondol, A. H., Hossain, M., Zaman, H. U., & Islam, S. (2021). Comprehensive study of 1-bit full adder cells: review, performance comparison and scalability analysis. SN Applied Sciences, 3(6), 644.

[5] Pandey, D., Singh, S., Mishra, V., Satapathy, S., & Banerjee, D. S. (2021, May). Sam: A segmentation based approximate multiplier for error tolerant applications. In 2021 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1-5).

[6] Mohammadi, A., Ghanatghestani, M. M., Molahosseini, A. S., & Mehrabani, Y. S. (2022). High-performance and energy-area efficient approximate full adder for error tolerant applications. ECS Journal of Solid State Science and Technology, 11(8), 081010.

[7] Shin, H., Kang, M., & Kim, L. S. (2021, December). Fault-free: a fault-resilient deep neural network accelerator based on realistic reram devices. In 2021 58th ACM/IEEE Design Automation Conference (DAC) (pp. 1039-1044). IEEE

[8] Sasikumar, A., Ravi, L., Kotecha, K., Indragandhi, V., & Subramaniyaswamy, V. (2022). Reconfigurable and hardware efficient adaptive quantization model-based accelerator for binarized neural network. Computers and Electrical Engineering, 102, 108302.

[9] Liu, W., Zhang, T., McLarnon, E., O'Neill, M., Montuschi, P., & Lombardi, F. (2019). Design and analysis of majority logic-based approximate adders and multipliers. IEEE transactions on emerging topics in computing, 9(3), 1609-1624.

[10] Nojehdeh, M. E., & Altun, M. (2020). Systematic synthesis of approximate adders and multipliers with accurate error calculations. Integration, 70, 99-107.

[11] Jiang, H., Santiago, F. J. H., Mo, H., Liu, L., & Han, J. (2020). Approximate arithmetic circuits: A survey, characterization, and recent applications. Proceedings of the IEEE, 108(12), 2108-2135.

[12] Bhattacharjya, R., Mishra, V., Singh, S., Goswami, K., & Banerjee, D. S. (2020, September). An approximate carry estimating simultaneous adder with rectification. In Proceedings of the 2020 on Great Lakes Symposium on VLSI (pp. 139-144).

[13] Sato, T., Yang, T., & Ukezono, T. (2019). Trading accuracy for power with a configurable approximate adder. IEICE Transactions on Electronics, 102(4), 260-268.

[14] Ramachandran, G., DIXIT, C. K., Kishore, K., & Arunraja, A. (2021, March). Performance analysis of mantissa multiplier and dadda tree multiplier and implementing with DSP architecture. In 2021 International Conference on Artificial Intelligence and Smart Systems (ICAIS) (pp. 1583-1587).

[15] Puchala, D. (2021). Approximate calculation of 8-point DCT for various scenarios of practical applications. EURASIP Journal on Image and Video Processing, 2021(1), 18.

[16] Rizzo, R. G., & Calimera, A. (2019). Implementing Adaptive Voltage Over-Scaling: Algorithmic Noise Tolerance vs. Approximate Error Detection. Journal of Low Power Electronics and Applications, 9(2), 17.

[17] Asaithambi, S., Rajappa, M., & Ravi, L. (2019). Optimization and control of CMOS analog integrated circuits for cyber-physical systems using hybrid grey wolf optimization algorithm. Journal of Intelligent & Fuzzy Systems, 36(5), 4235-4245.

[18] Thakur, G., Sohal, H., & Jain, S. (2020, November). FPGA-based parallel prefix speculative adder for fast computation application. In 2020 Sixth International Conference on Parallel, Distributed and Grid Computing (PDGC) (pp. 206-210).

[19] Khaksari, A., Akbari, O., & Ebrahimi, B. (2023). BEAD: Bounded error approximate adder with carry and sum speculations. Integration, 88, 353-361.

[20] Kim, Y. (2019). An accuracy enhanced error tolerant adder with carry prediction for approximate computing. IEIE Transactions on Smart Processing & Computing, 8(4), 324-330.

[21] Patel, S. K., Garg, B., & Rai, S. K. (2020). An efficient accuracy reconfigurable CLA adder designs using complementary logic. Journal of Electronic Testing, 36, 135-142.

[22] Vaithiyanathan, D., Kolhe, R., Mishra, A. K., Britto, P. J., & Kunaraj, K. (2020, December). Performance Analysis of 8-Point Approximate DCT Architecture Using Conventional and Hybrid Adders. In 2020 IEEE International Symposium on Smart Electronic Systems (iSES)(Formerly iNiS) (pp. 246-249).

[23] Nayar, R., Balasubramanian, P., & Maskell, D. L. (2020, July). Hardware optimized approximate adder with normal error distribution. In 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 84-89).

[24] Vinod, G. U., Vineesh, V. S., Tudu, J. T., Fujita, M., & Singh, V. (2020, November). LUT-based circuit approximation with targeted error guarantees. In 2020 IEEE 29th Asian Test Symposium (ATS) (pp. 1-6).

[25] Nagarajan, M., Sasikumar, A., Muralidharan, D., & Rajappa, M. (2020). Fixed point multi-bit approximate adder based convolutional neural network accelerator for digit classification inference. Journal of Intelligent & Fuzzy Systems, 39(6), 8521-8528.

[26] Yin, P., Wang, C., Waris, H., Liu, W., Han, Y., & Lombardi, F. (2020). Design and analysis of energy-efficient dynamic range approximate logarithmic multipliers for machine learning. IEEE Transactions on Sustainable Computing, 6(4), 612-625.

[27] V. Gupta, D. Mohapatra, A. Raghunathan and K. Roy, "Low-Power Digital Signal Processing Using Approximate Adders," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, pp. 124-137, Jan. 2013, doi: 10.1109/TCAD.2012.2217962.