International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 1
DOI: https://doi.org/10.17762/ijritcc.v11i1.6055
***Article Received**: 18 November 2022 **Revised**: 22 December 2022 **Accepted**: 02 January 2023*

Design and Analysis of High Speed Multiply and Accumulation Unit for Digital Signal Processing Applications

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Abstract—The fundamental component used in many of the Digital signal Processing (DSP) applications are Multiply and Accumulation Unit (MAC). In the literature, a multiplier consists of greater number of full adders and half adder in partial product reduction stage, which increases the hardware complexity and critical path delay to MAC unit. To overcome this problem, two novel multipliers are proposed in this article. The proposed multipliers are designed and implemented in hardware, which reduces the circuit complexity and improves the overall performance of the MAC unit with less delay. The proposed multipliers are compared with the 4-bit existing designs and observed that the number of slices Look Up Tables (LUTs) are minimized from 113 to 43, Slices are reduced from 46 to 14, Full Adders (FAs) are lessened from 28 to 23, bonded Input Output Blocks (IOBs) and Half Adders (HAs) were not altered. The time delay is reduced from 14.251ns to 7.876ns. The proposed multipliers are compared in the literature with the 8-bit multiplier, then the number of Slice LUTs are reduced from 510 to 231, Slices are reduced from 218 to 113, FAs are reduced from 120 to 110, HAs are reduced from 56 to 39, time delay is reduced from 26.228ns to12.748ns, but bonded IOBs count remains same. The synthesis and simulations results are verified by using Xilinx ISE 14.7 version tool.

Keywords- DSP (Digital Signal Processing), FA(Full-Adder), HA(Half-Adder), IOB (Input Output Blocks), LUT (Look up Table), MAC (Multiply and Accumulation Unit).

I. INTRODUCTION

The adders and multipliers are the major functional blocks used in many of Digital signal processing applications [1], [2]. These designs are widely used for real-time signal processing like audio signal processing, video processing, Image processing and data processing applications. Adders and multiplier units are also critical components of the MAC unit. Hence, for high performance DSP applications we require low complexity and less critical path delay MAC unit architecture. The main objective of this research is to implement a MAC unit with high speed by using the proposed multiplier. A conventional MAC unit consists of three fundamental components such as multiplier, adder, and accumulation unit. To implement the N-bit MAC unit requires 2N bit multiplier. The multiplier will generate the partial products and then partial products are reduced by the FAs and HAs. Then the results are fed to the adder which will add both the multiplier results and previously accumulated result. Generally, adders used in this stage are ripple carry adder or carry save adder [3]. The performance of the MAC unit can be improved by enhancing the performance of either multiplier or adder. Enhancing the performance of the multiplier will greatly reduce the parameters like area and delay of the MAC unit rather than adder. Previously various multipliers have been implemented like Wallace tree multiplier and Dadda multiplier [4 - 6] to design the MAC unit. Hence the major advantages of using this multiplier are to reduce the partial product reduction stage. Hence this design consumes a greater number of full adders and half adders to implement a multiplier. Another approach is to improve the performance of the adders, based on these various adders' architecture designs were implemented [7-10].

Various MAC units were implemented by using different adders. In [11-12] to implement the MAC unit they use carry

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save adder to perform final addition. In final stage of carry save adder consists of ripple carry adder which consumes more critical adder. In some other designs [13], [14] they used different types of compressors to reduce the partial production stage instead of full adders and half adder which will reduce the hardware complexity of the design, but they fail to achieve the performance of the circuit stage. These multipliers are used in MAC unit to red t. In existing design [15], they have implemented MAC architecture for the reduction of critical path delay. So, in this design they have integrated a part of additions into the PPR process. In this MAC unit, Final addition, and accumulation (adder) of most significant bits are performed in the Partial Product Reduction process of the next multiplication. Hence, the carry propagation length can be reduced, but slightly increasing in hardware complexity. The two MAC architectures are implemented in this paper, two novel multipliers architecture were proposed, which consists of a smaller number of full adders and half adders in partial product reduction both Area and critical path delay of the overall design. In this paper, we also implemented an FIR filter using Proposed MAC to evaluate its overall performance.

The paper discusses about previous multiplier and MAC architectures that were implemented over a decade, two novel multipliers architecture and their implementation as a MAC unit, the Digital signal processing application that is implemented by using the proposed MAC unit. various parameters and simulation results of existing and proposed design.

II. Related Works

In recent times they are large number of works that are going on MAC architectures. In this, a novel design is carried out to decrease the equipment intricacy of the fractional item decrease and the last expansion, hence diminishing the general power. The speed of operation can be improved by adding the summation tree before the last adder as opposed to going through the whole summation network in the design. In various types of multipliers and they performance parameters are analyzed. Wallace tree and Dadda multiplier are used in MAC unit to improve the performance. In a novel Wallace multiplier is designed by using different types of counters such as 5:3, 6:3 and 7:3 counters to reduce the PPR stage, hence further they can use in MAC unit stage. Approximate multiplier is designed by using high order compressor, which will reduce both area and delay will loss of accuracy. In [16-18] various parallel adders were implemented such as ripple carry adder and carry look ahead adder is used in final stage of multipliers. These adders also used in accumulation (adder) stage to reduce critical path delay and area. A survey on MAC unit is done. Different MAC units were implemented by using different adders and multipliers. Multipliers are used to generate the PPR stage and while adders are used to reduce the accumulation stage. Some of the multipliers used in this design are array multiplier and booth multiplier. A novel high-Speed MAC is introduced in [19] which are implemented by using 4:2 compressors in multiplier stage, they by reducing the hardware complexity and critical path delay. A new modified-Booth algorithm is used for high-speed multiplier circuit [20],[21]. The existing MAC design is shown in Fig.1. This architecture consists of two cycle MAC architecture to implement the final result. The first cycle performs the Partial Product generation process, the partial production stages use full adder and half adder to reduce the circuit; the other bits are done in final addition. Then, the second stage performs the (k + α)-bit addition to generate the accumulation result.

The fig 1. It consists of two operands X and Y. In the current MAC unit, the aggregation has been handled in both the α-bit addition and fractional item decrease handling. In this manner, to come by the end-result in the last cycle, the creator has debilitated the expansion of k + α bits in different cycles to save power. This plan utilizes the AND entryway with an empower sign to cripple the expansion of pieces (k + α). The empower sign will be '1' on the keep going cycle and '0' on different cycles. The phase of fractional item age and halfway item decrease of the existing design shown in below fig. 2(a) and fig. 2(b). AND gate is used of partial product generation. Half adders and full adders are used for partial product reduction process.

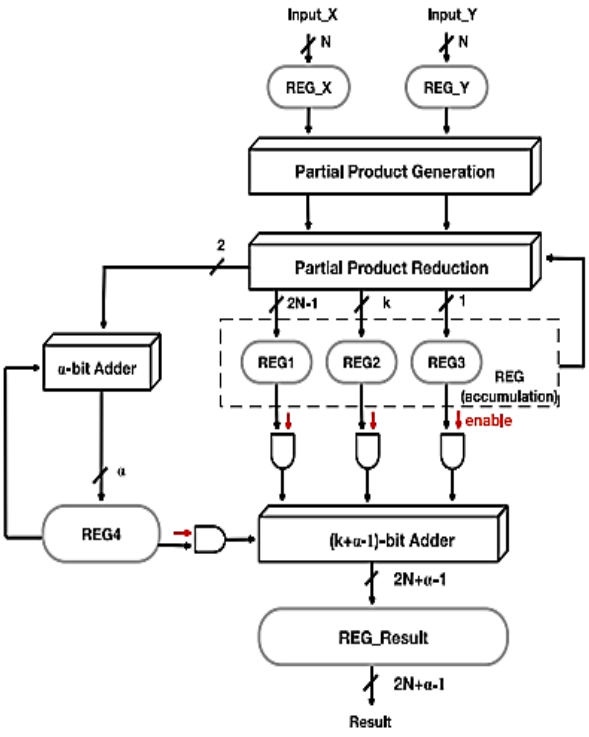

Figure 1. Existing MAC architecture

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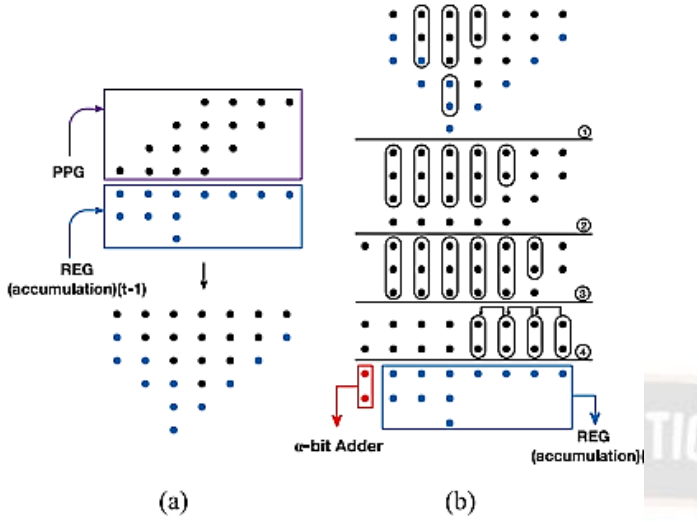

Figure 2. (a) PPG process (b) PPR process

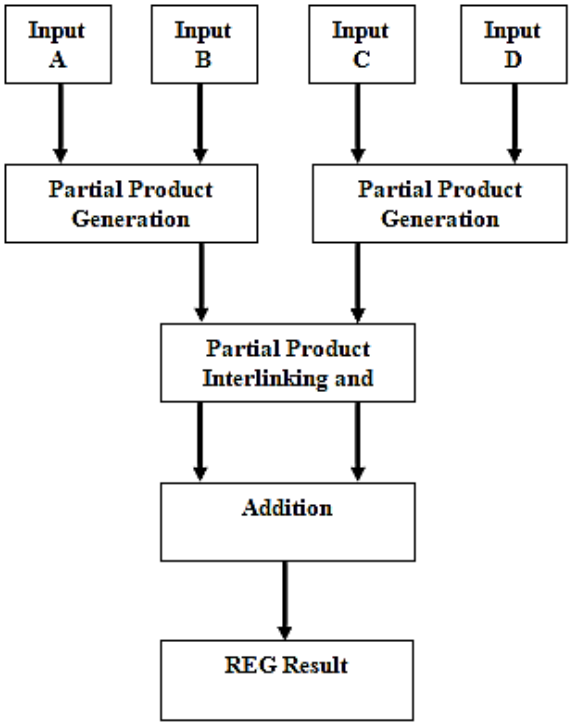

Figure 3. Block diagram of Proposed MAC architecture

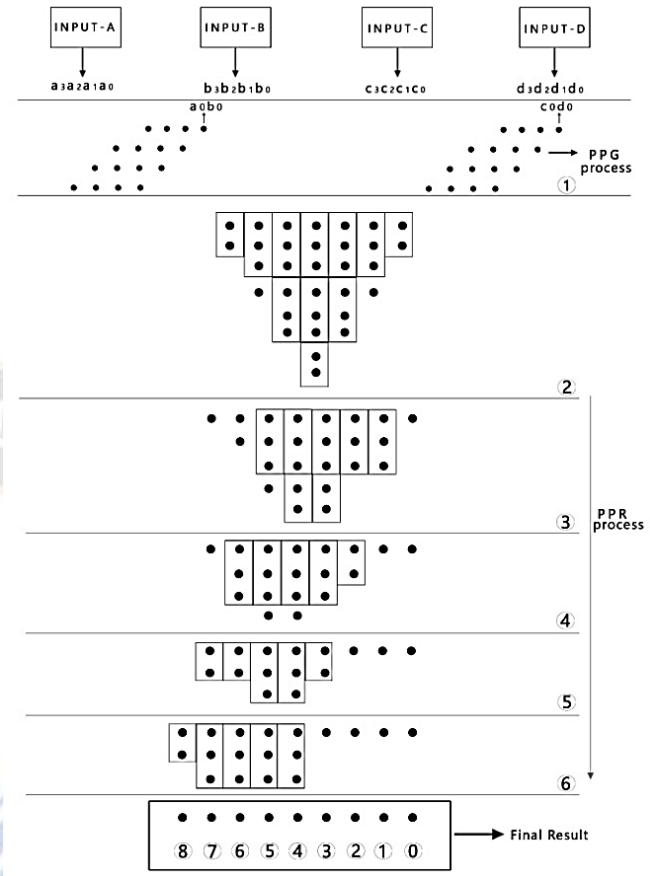

Figure 4. Internal MAC architecture of proposed design 1

The Fig 5 shows the proposed method 2 for MAC design. The total of 23 full adders and 9 half adders used to generate the result for design 1. For design 2 we require 33 full adders, and 14 half adders are used to implement the design. The performance of the proposed design 1 is slightly greater than the proposed design 2.

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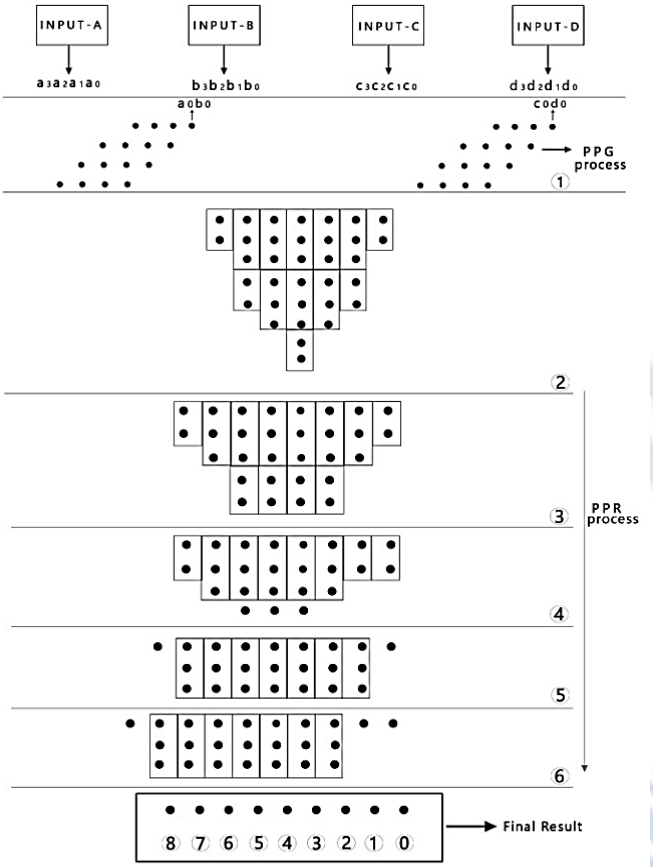

Figure 5. Internal MAC architecture of proposed design 2

In this article, FIR filter is implemented by using proposed MAC unit. This FIR filter is mostly widely used component in many DSP applications. 8 tap FIR filter is designed by using four proposed MAC unit as shown in below Fig 6. High order FIR filter is used in many digital applications, so reduction of MAC block will improve the overall performance of applications.

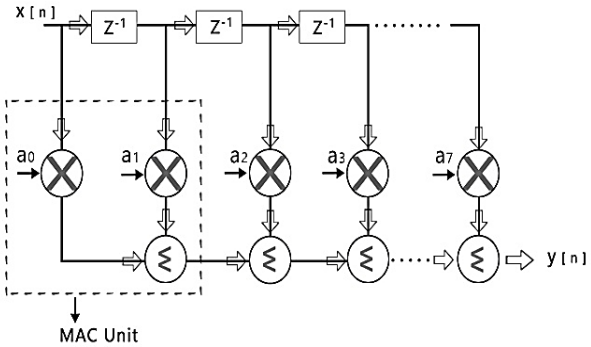

Figure 6. 8-tap FIR filter using proposed MAC unit

III. RESULTS

Simulation results:

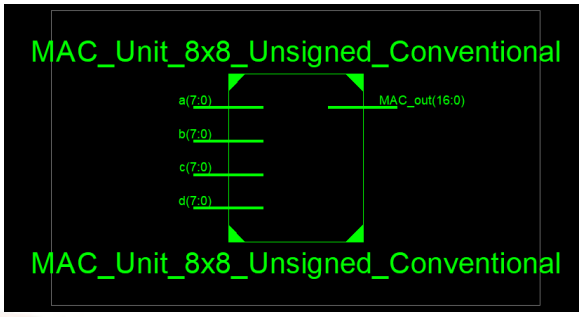

Figure 7. RTL schematic(8-bit) for proposed design

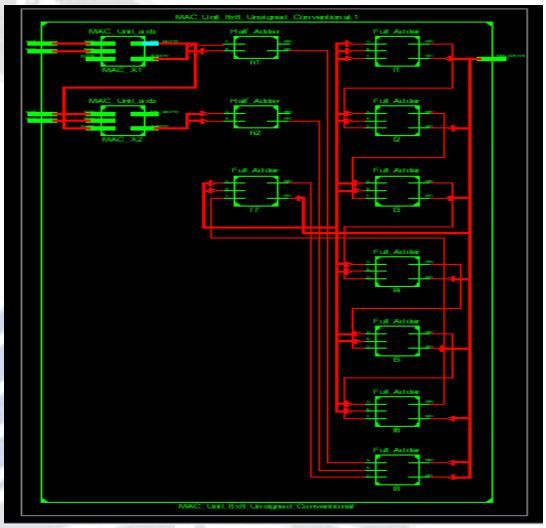

Figure 8. Full view of simulated schematic(8-bit) for proposed design

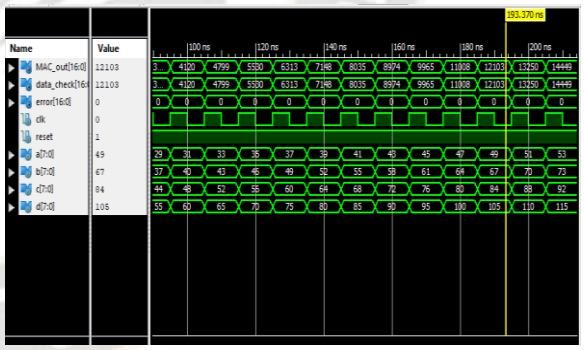

Figure 9. Simulation results of 8-bit proposed MAC unit1

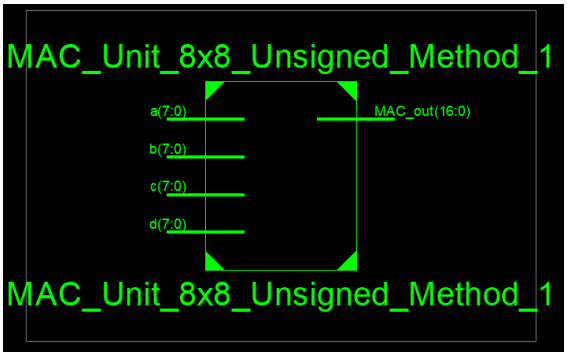

Figure 10. RTL Schematic of Proposed MAC unit2

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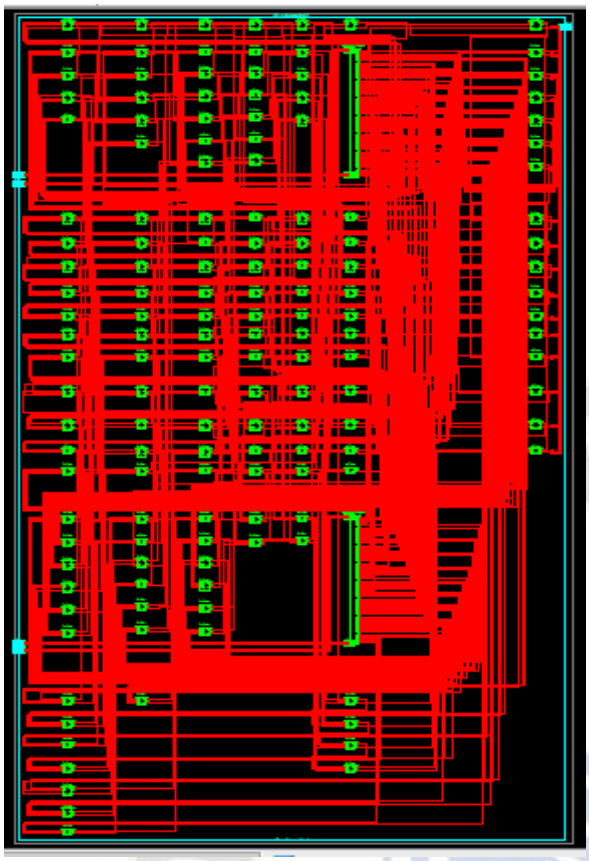

Figure 11. Full view of Proposed MAC unit2

Figure 7,8,10,11 represents the RTL Schematic and full view of proposed methods 1 and 2.

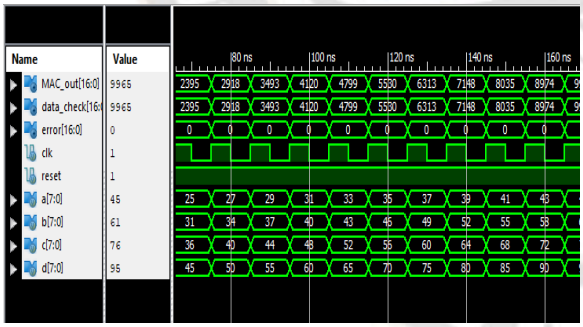

Figure 12. Simulation results of 8-bit proposed MAC unit2

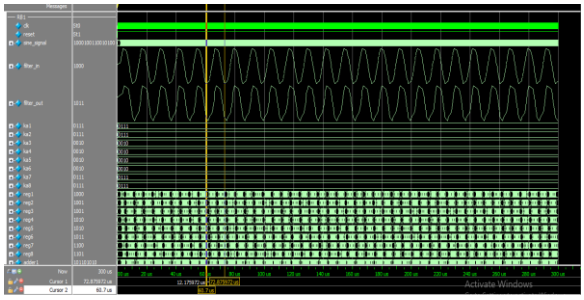

Figure 13. Simulation result of 8-tap FIR filter.

Comparisons for 4x4 Unsigned Multiplier:

TABLE I. COMPARISON BETWEEN EXISTING AND PROPOSED DESIGN OF MAC ARCHITECTURE

Comparisons for 4 Bit MAC Architecture - XC5VLX50t-2ff1136 FPGA:			
Parameters	Existing Method	Method 1 with reduced adders	Method 2 with reduced area
Number of Slice LUTs	113	43	110
Number of Slices	46	14	92
Number of bonded IOBs	25	25	25
Number of FAs	28	23	33
Number of HAs	9	9	14
Delay (ns)	14.251	7.876	14.538
Power (mW)	0.560	0.560	0.560

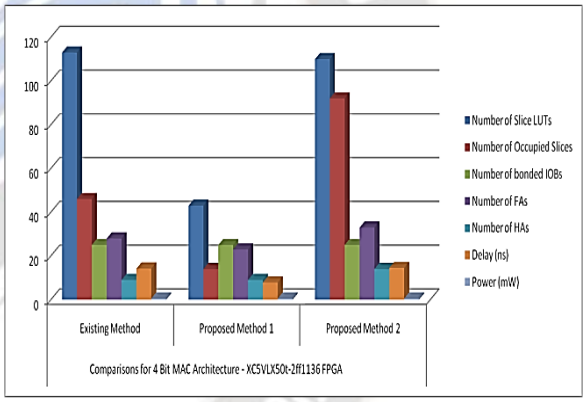

Figure 14. Device utilization report for existing and proposed designs for 4-bit MAC unit

The above Table 1. Shows the comparison between the existing design and proposed designs of 4-bit MAC unit. The proposed MAC unit has a smaller number of LUT's nearly half of the existing design. These synthesis results are generated by using Xilinx ISE tool. The performance parameters of method 1 like area and delay is less when compared to existing design. Whereas proposed method 2 had less area complexity with slightly increasing in delay. The bar graph representation of various parameters and their analysis is shown in above figure 14

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Comparisons for 8x8 Unsigned Multiplier:

TABLE II. COMPARISON BETWEEN EXISTING AND PROPOSED 8 BIT MAC ARCHITECTURE.

Parameters	Comparisons for 8 Bit MAC Architecture - XC5VLX50t-2ff1136 FPGA		
	Existing Method	Method 1 with reduced adders	Method 2 with reduced area
Number of Slice LUTs	510	231	231
Number of Occupied Slices	218	113	100
Number of bonded IOBs	49	49	49
Number of FAs	120	110	110
Number of HAs	56	39	36
Delay (ns)	26.228	12.748	12.503
Power (mW)	0.560	0.560	0.560

The comparison between existing design and proposed designs of 8-bit MAC architecture is shown in above table 2. As the bit length increase the parameters like area and delay will greatly reduce in the proposed designs.

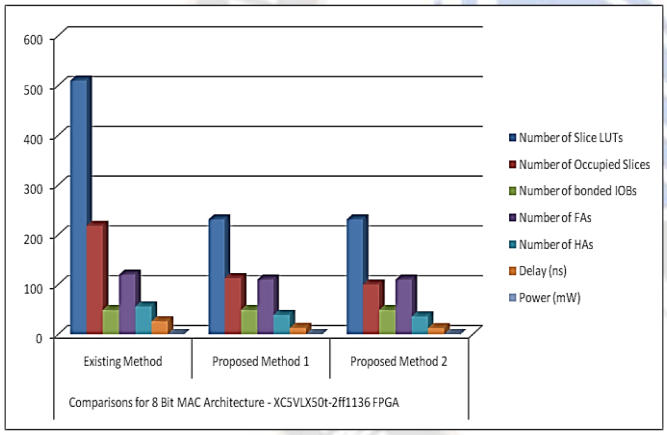

Figure 15. Device utilization report for existing and proposed designs for 8-bit MAC unit.

Comparisons for 8th Order 4 Bit and 8-Bit FIR Filter Design:

TABLE III. COMPARISON TABLE FOR FIR FILTER

Parameters	FIR Filter 8th Order - 4 Bit Method 1	FIR Filter 8th Order - 4 Bit Method 2	FIR Filter 8th Order - 8 Bit Method 1	FIR Filter 8th Order - 8 Bit Method 2
Number of Slice LUTs	320	352	994	1004
Number of Slices	234	257	861	750
Number of bonded IOBs	10	10	16	16
Delay (ns)	10.694	11.726	17.866	17.866
Power (mW)	3.519	3.519	3.521	3.520

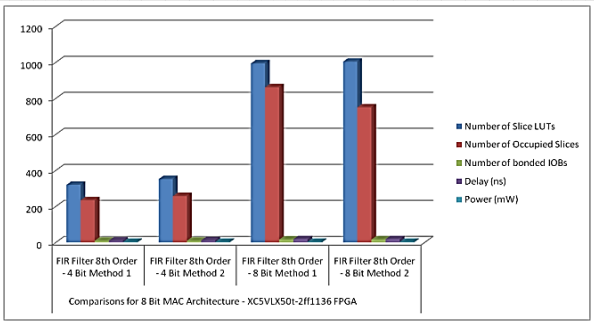

Figure 16. Device utilization summary of FIR filter for Proposed Methods

The comparison between existing design and proposed designs of FIR filter is shown in above table 3. The device utilization summary of FIR filter is shown in above fig 16. As the bit length increase the parameters like area and delay will greatly reduce in the proposed designs.

IV. CONCLUSION

In this paper, an area efficient high speed MAC architecture is implemented. Two novel multipliers are designed, each multiplier has its own advantages. Based on this multiplier two MAC architecture are designed. From the above results we can say that the proposed methods consume less area and less delay when compared to conventional and existing designs. When compared to the 4-bit multiplier with the existing design, the number of Slice LUTs were reduced from 113 to 43, Number of Slices were reduced from 46 to 14, Number of bonded IOBs were not changed, Number of FAs were reduced from 28 to 23, Number of Has were not altered, delay was reduced from 14.251ns to 7.876ns. When compared to the 8-bit multiplier with the existing design, the number of Slice LUTs were reduced from 510 to 231, Number of Slices were reduced from 218 to 113, Number of bonded IOBs were not changed, Number of FAs were reduced from 120 to 110, Number of Has were reduced from 56 to 39, delay was reduced from 26.228ns to12.748ns. The synthesis and simulation results of proposed and existing designs are taken from Xilinx ISE 14.7 version tool.

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