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Design of Ka-Band Low Noise Amplifier Using CMOS Technology

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Abstract:- In this paper, design of a Low Noise Amplifier is undertaken for higher frequency bands, particularly Ka-band. The designed LNA can be used in satellite transponders for the mentioned frequency band. Generally LNAs are the first block in a transponder and are very sophisticated in trems of noise performance. A common-source topology along with source degeneration is used to achieve low noise figure and linearity with high gain. The use of CMOS technology provides new applications in designing this amplifier. It offers designs at lower cost, reduced power consumption and higher levels of integration. Proposed circuit achieves a maximum gain of 23dB with a relatively low noise figure of 2.9dB. This system can work in Deep-Space region as part of a satellite transponder.

Keywords: *LNA, CMOS, Common-Source (CS), Ka-Band, source degeneration, Noise Figure (NF), gain, linearity, impedance matching.*

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1. INTRODUCTION

Basic design of a satellite transponder consists of a LNA, a mixer circuit with Voltage Controlled Oscillator (VCO) and a Power Amplifier in the same order. Of course it also consists of a receiving and a transmitting antenna. Hence, the first component in a receiver system is chosen to be LNA as it dictates the performance of the entire system. Not only does it amplify the gain, it makes sure that noise from the other successive stages does not really affect the Noise Figure (NF) of the system. This can be verified by Friis equation

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \qquad (1)$$

where F_{total} is the total noise figure of the system. As seen from the equation, NF from the subsequent stages is limited by the gain from the first stage. In other words NF from following stages is not too large if the gain from LNA is significant. This is the reason why we choose to have the LNA as the first stage.

Noise performance is a major factor while designing LNAs. In fact, all the key specifications like gain, linearity, noise figure, input-output matching, power consumption play an important role in the designing process. These factors are influenced by the topologies that we use. As we are using MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) the topologies available are limited. Common-Source (CS), Common-Gate (CG), Cascode, Differential are some of the commonly used topologies that are used for different applications. For our design we are using 2-stage cascode configuration with inductive source degeneration [1].

Section 2 describes the design process for LNA. In section 3 the proposed design is presented while the simulation results are given in section 4 and conclusion in section 5. The design is implemented using ADS (Advanced Design System, Keysight technologies) to design LNA, PA, Mixer circuit. HFSS is used for designing the antennas.

2. DESIGN PROCESS

In this section we highlight the design process followed for the designing of LNA. Firstly, we require a topology to start with as the choice of matching networks and the values of lumped components is governed it [2].

As stated in the previous section, the design topologies available with MOS devices are limited. Following figure shows source degeneration topology using resistors. A resistor is connected to the source terminal and one resistor is taken as the load.

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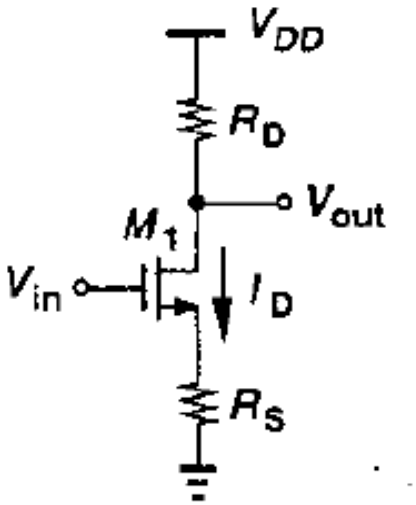

Figure 1: Source Degeneration with resistive load [1]

From the figure, if V_{in} decreases, I_D also decreases and the voltage appears across the degenerate resistor leader to a linear drain current.

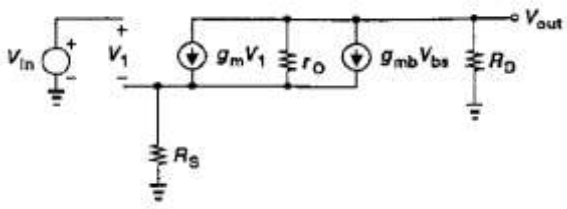

Figure 2: Equivalent circuit of Figure 1 [1]

From the small signal model the small signal gain can be calculated as;

$$A_V = -G_m R_D \qquad (2)$$

Where,

$$G_m = \frac{g_m}{1+g_m R_S} \qquad (3)$$

Hence gain can also be written as,

$$A_v = \frac{g_m}{1+g_m R_S} R_D \qquad (4)$$

Inductive source degeneration with cascode topology is used such that the only noise sources will be matching and biasing networks and the transistor itself. Source degeneration also improves stability and linearity of a circuit. Inductive source degeneration with inductive load is depicted in the following figure;

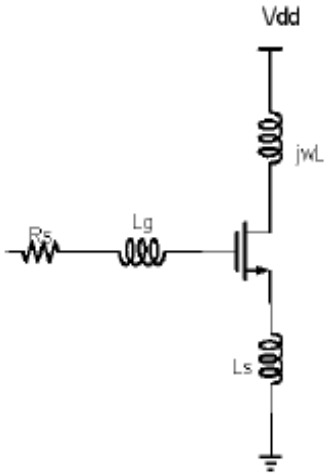

Figure 3: General circuit of Inductive source degeneration [3]

After deciding the topology, next step is to design the matching networks. As an accepted standard, the input and output are matched at 50Ω. The equivalent input impedance, Z_{in}, for source degenerated circuit like the one shown in above figure is calculated as;

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{jw\,C_{gs}} + \frac{g_m L_s}{C_{gs}} \qquad (5)$$

There are two types of matching networks. One of them is concerned with maximum transfer of power from source to load. Other one is related to minimizing signal reflection from source to load. However, the condition to satisfy matching is same for both the cases i.e. the source impedance must be equal to the load impedance [3]. In this case the impedance needs to be matched at 50Ω. Now we have to choose the type of biasing that needs to be applied to the transistors for optimum performance. In CS amplifiers, the input bias signal is applied to the gate terminal, known as the gate to source voltage V_{GS}. This voltage needs to be greater than the threshold voltage in order for the transistor to be ON. Ideally, gate-to-source voltage is taken to be as small as possible such that it does not compromise the other parameters [1]. However, at higher frequency operation like ours, it is desirable to have a slightly higher V_{GS} biasing for achieving higher f_t (transit frequency) which lowers noise figure of the system. F_t is a measure of operating frequency. It is the frequency where current gain is 1 [4].

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (6)$$

Now we need to do transistor sizing by first calculating the targeted drain current. After finding out the drain current, we can easily calculate width and length of the transistors

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and also g_m (transconductance) of the amplifier by using the following equations:

$$I_{D=}W v_{sat} C_{OX} \frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_C L}(1+\lambda V_{DS}) \quad (7)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (8)$$

After we have these values, parameters such as load and gate capacitance can be readily calculated. This concludes the design steps for designing the LNA.

3. LNA DESIGN

There are a lot of specifications that are needed to be fulfilled for the device to function properly. Most importantly, the device should be stable in the frequency range chosen for operation.

This project utilizes the source degeneration topology for amplifying the signal. In this, an inductor is connected to the source terminal and grounded, along with an inductance connected to the gate terminal as well. Full schematic implemented on ADS is shown below.

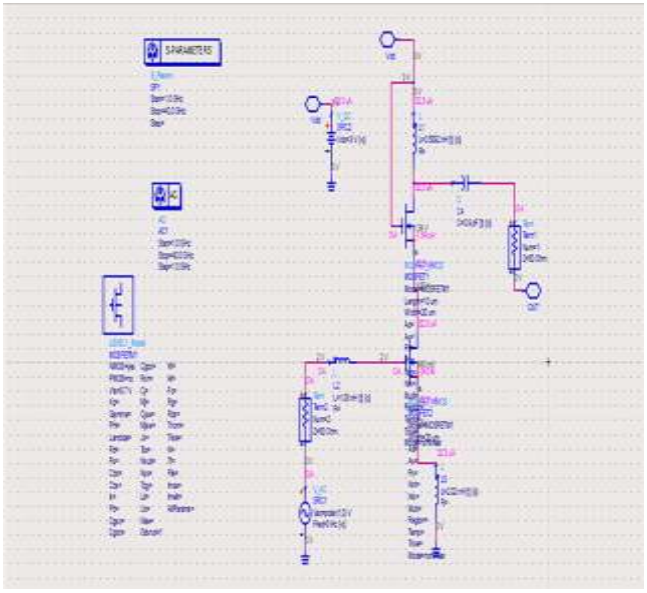

Figure 4: Circuit implementation on ADS

As can be seen from the figure, inductances are connected to the source and gate terminals. The load is also taken to be an inductor as it induces very low noise and makes sure the resonant frequency remains constant. A feedback path exists between the load and gate of the second transistor to increase stability. Moreover, cascode topology is employed for operation in higher frequency range. It also ensures that reverse current reduces from output to input. MOS transistors used are operated in strong inversion and sub-threshold region. Capacitor placed at the output terminals is to filter out the noise coming from the DC source. Use of resistors is avoided as they have large area and induce a lot of thermal noise and heat [5]. Values of the inductors can be calculated from;

$$R_s = L_s \frac{g_m}{C_{gs}} = 50\Omega \quad (9)$$

From the figure we can infer that the matching network used is an inductive one. Input and output ports are matched at 50Ω. Input signal is applied to the lower MOS device through an inductor. Input source is a RF signal with a frequency of 28GHz.

At higher frequency ranges, S-parameters are used for analyzing 2-port networks. It measure the incident and reflecting voltages at these two ports. Usually represented in the form of a matrix, they are also known as scattering parameters. S_{12} and S_{21} are the reverse and forward voltage gain. S11 and S22 are input and output reflection constants [11]. Together they make the scattering matrix for two port networks. As the gain-bandwidth product remains constant, number of amplifying stages can be increased to provide high gain and low NF at higher frequencies. Following section deals with simulation of the proposed circuit.

4. SIMULATION and RESULTS

All the simulations are done using ADS design tool. After carefully selecting the values of all the lumped parameters, simulation of the design is performed. Threshold voltage for the transistors is taken as 0.6V. input signal is 0.9 to 1V at a frequency of 28GHz. Overall power supply (Vdd) for the system is 2V.

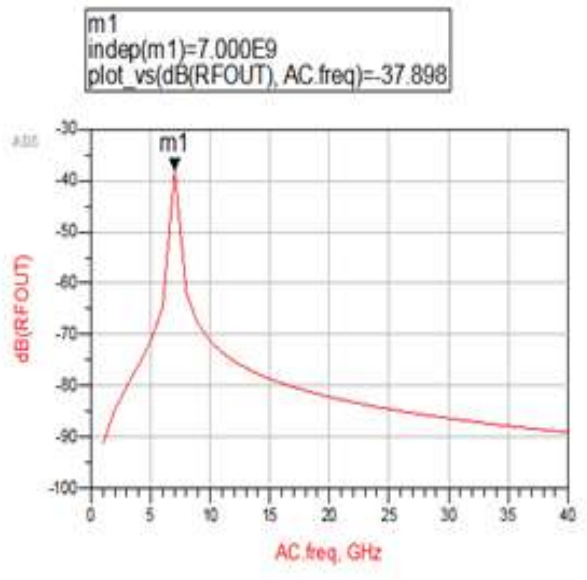

Figure 5: output in dB

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Above figure shows that the circuit achieves a maximum gain of 23dB. The device can amplify signals at the desired frequency range. However it is essential to make sure that the gain should increase in tandem with the input signal. Following waveform gives the output magnitude with respect ro frequency.

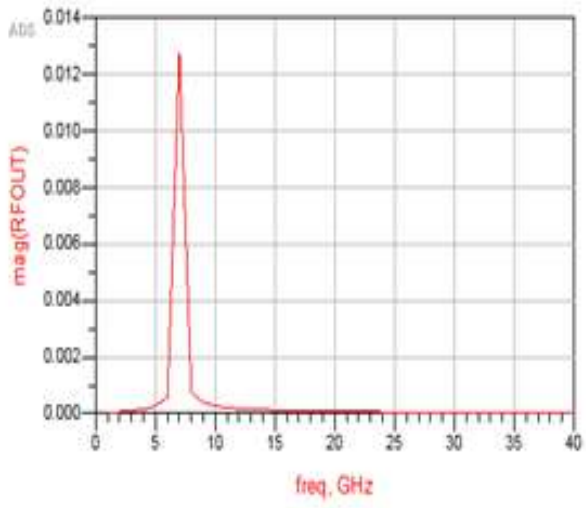

Figure 6: output magnitude

Above figure shows that the circuit achieves a maximum gain of 23dB. The device can amplify signals at the desired frequency range. However it is essential to make sure that the gain should increase in tandem with the input signal.

It is evident from the waveform that proposed circuit shows good linearity at the frequency of operation.

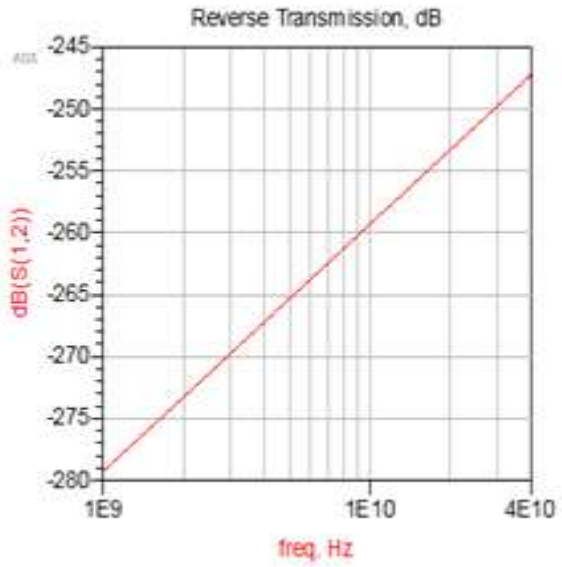

Figure 7: S_{12}

Parameter S_{12} is the reverse voltage gain while S_{11} is the input voltage reflection constant. it is a good measure of linearity and stability. The system achieves stability at 11GHz

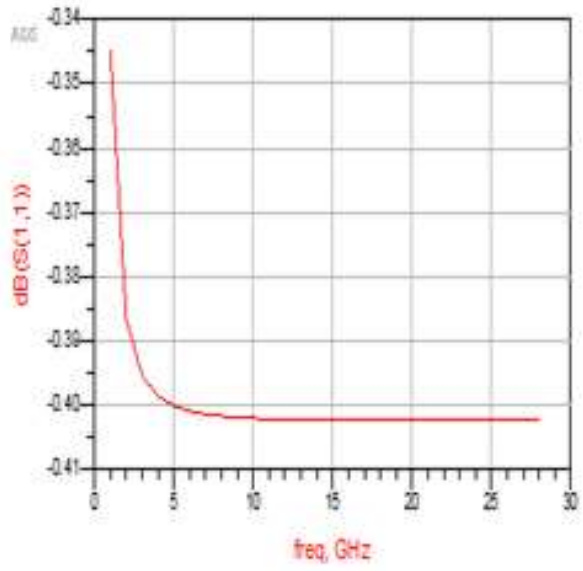

Figure 8: S_{11}

S11 provides a good input impedance matching at -0.40dB. It is the measure of input voltage that is reflected at the terminal.

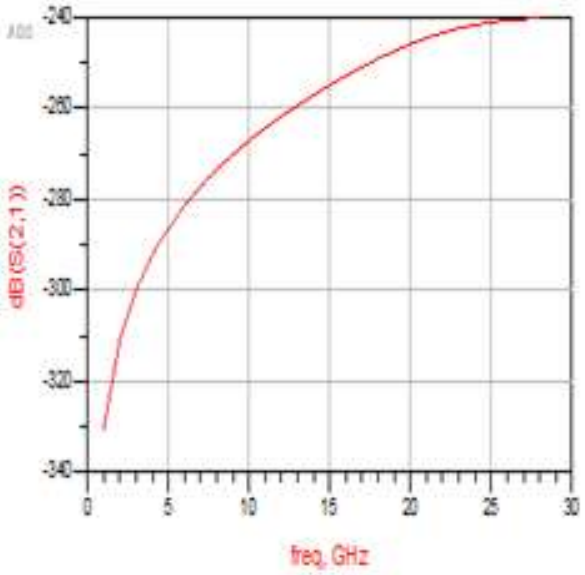

Figure 9: S_{21}

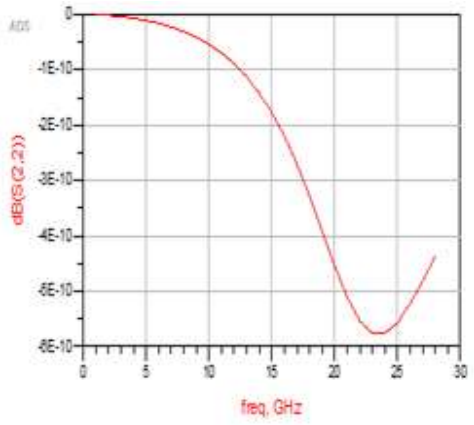

Figure 10: S_{22}

S_{21} and S_{22} are measured at the output terminal. While S_{22} is the output voltage reflection constant, S_{21} in general terms is the gain of the amplifier. Hence, at RF operations, S-parameters play a huge role in analysis of the LNA.

There are many sources of noise when dealing with analog circuits. Moreover, since we are using MOS transistors, it is essential to rectify all the noise sources present in the devices. CMOS technology suffers from thermal noise, flicker noise as well as noise from the parasitic capacitances. Noise figure of LNA should be less than 3dB for being considered as a good amplifier. As seen from the following figure, noise factor is calculated to be around 2.9dB. As the proposed LNA is designed for use in satellite transponders, there can be many environmental factors as well that can produce or induce noise in the signal. Therefore it becomes necessary that the LNA should have a good gain and low noise figure as the entire system depends on the gain of the first block i.e. LNA. If this is achieved then the power of the signal can be increased sufficiently in order to transmit it over a broad area without much interference from environmental factors.

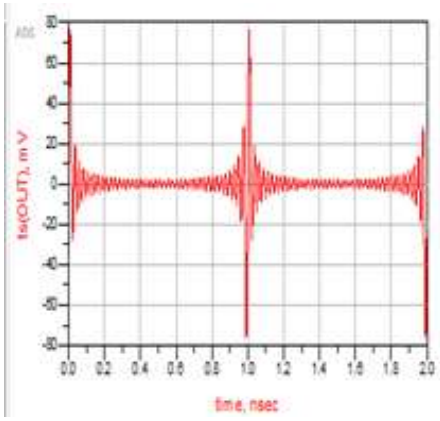

Figure 11: Noise Analysis

5. CONCLUSION AND FUTURE SCOPE

Proposed device shows good performance at higher frequency range, in particular the Ka-band. Inductive degeneration with cascode device and inductive load is the selected topology. Device shows a gain of 23dB and a reduced noise figure of 2.9dB. S-parameters were observed and characteristic waveforms were observed. Input voltage was taken as 1V at 28GHz. Width was calculated to be 20µm while the length of the channel is 10µm.

Though the device shows good performance, it can be seen that increasing the number of amplifying stages may increase the performance of the system. One other noise cancellation technique that can be used further reduce noise figure. When an inversion channel is formed and MOSFET starts to conduct, it can behave as a capacitor. This property of MOS devices can be used for matching purposes by taking into consideration that if the MOS capacitance is high enough then it can be a part of the input impedance matching network. Furthermore, many new techniques can be applied to reduce noise in a system.

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