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Design of Digital Frequency Synthesizer for 5G SDR Systems

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Abstract—The previous frequency synthesizer techniques for scalable SDR are not compatible with high end applications due to its complex computations and the intolerance over increased path interference rate which leads to an unsatisfied performance with improved user rate in real time environment. Designing an efficient frequency synthesizer framework in the SDR system is essential for 5G wireless communication systems with improved Quality of service (QoS). Consequently, this research has been performed based on the merits of fully digitalized frequency synthesizer and its explosion in wide range of frequency band generations. In this paper hardware optimized reconfigurable digital base band processing and frequency synthesizer model is proposed without making any design complexity trade-off to deal with the multiple standards. Here fully digitalized frequency synthesizer is introduced using simplified delay units to reduce the design complexity. Experimental results and comparative analyzes are carried out to validate the performance metrics and exhaustive test bench simulation is also carried out to verify the functionality.

Keywords: SDR system, Frequency synthesizer, Phase locked loop, ADPLL.

I. INTRODUCTION

In recent years the throughput demands of wireless devices used for communication systems is increased steadily which requires greater flexibility. This can be achieved through the SDR system in many real time applications since SDR offers low complexity wireless radio which can offer different wireless standards by formulating the appropriate design functions. In general SDR systems come as reprogrammable single compound devices which can support multi-service, multi-standard, multi-band radio systems.

The relatively hardware cost and energy consumption rate of software-defined radio (SDR), should be as minimum as possible to extend its application ranges [1]. To accomplish this, it is essential to optimize frequency synthesizer which is the main computational block. Moreover the local oscillator (LO) used in frequency synthesizer and its tuneable range should meet the design requirement which is most critical task. SDR transceiver system with Quadrature Direct Digital Frequency Synthesizer (QDDFS) [2] can generates trigonometric signals in digital format to speed up the Digital Up Converters (DUC) and Digital Down Converters (DDC).Three most common design methodologies used for FS implementation are as follows: Indirect, Analog and Digital. Indirect FS unit use PLL circuit to compare the reference input clock and output signal with optimal performance range and step ranges. In Analog FS [3] mathematical computations is performed using multiplication, division in order generate the desired output frequency. For high performance DDFS the computational cost required for PLL design is needs to be reduced and also it is essential to formulate SDR as single device which support different wireless standards. And also to accommodate various standards the PLL frequency synthesizer should provide wide frequency tuning range, improved settling time, reduced phase noise and frequency spur. Software defined radio for wireless communication system should equip PLL as integrated component to support wide range of standards.

In general DSPs and FPGAs are two different approaches used for implementing SDR in hardware platform. DSP based model offers the flexibility with the improved energy and area efficiency. But DSP model can't meet desired throughput rate demands of emerging wireless communication system. And lack of reconfiguration also limits its performance. On the other side FPGA based modelling allows dynamic reconfiguration which can support wide range of standards and retains all the potential metrics of DSP based approaches.

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Moreover the recent advancements in FPGA technology allow developing a high performance SDR system. In some cases graphics processing unit (GPU) also used for its parallel computing abilities.

1.1 DIRECT DIGITAL FREQUENCY SYNTHESISER (DDFS)

DDFS is the most generic sinusoidal signal generator used to generate different frequency with the dynamic range of 1Hz–several GHz. In wireless application [4]-[5] it can also be used for the conversion from the baseband to IF frequency range. It has several potential metrics like sub-Hertz level frequency resolution, fast-frequency switching, suppressed phase noise, improved spectrum large bandwidth and purity etc. though it is preferred choice for SDR system due to its inherent performance measures PLL widely used in many recent wireless communication systems. The implementation of DDFS has some practical difficulties in terms of resource utilization rate and complex computations.

In existing methods, Coordinate Rotation Digital Computer (CORDIC) Technique [6] and Lookup Table (LUT) [7] are widely used in Direct Digital Frequency Synthesizer (DDFS). In some cases hybrid combination of LUT and CORDIC is used to for DDFS. But due to demands over extended memory requirement lookup Table approaches are not suitable for many wireless applications since memory devices are power hungry devices in nature. On other side CORDIC based implementations [8] requires highly iterative computation which cause significant delay overhead. Moreover due to its Trigonometric measures sine and cosine signals are generated using highly complex architecture in CORDIC, which reduces its potential merits for DDFS implementation [9]-[10].

II. RELATED WORKS

Frequency synthesizer proposed in Van Driessche et al (2006) enables the quadrature LO-signals for generating an extremely wide range of frequencies which is ranging from 174 MHz to 5.825 GHz. The tuning range is precisely increased using programmable dividers and a reconfigurable delay locked loop (DLL). In [12] developed PLL with high-speed dividers for designing frequency synthesizer to generate in-phase/quadrature phase signal with frequency bands of 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and in-phase signal over 20-28 GHz for software-defined radio applications [13].

In [14] proposed monolithic software-defined radio design for 2 × 2 MIMO system which includes dedicated wide-band frequency synthesizers for both uplink and downlink paths to enable Frequency Division Duplex (FDD) radios. Here Direct Digital Synthesis (DDS) based integer-N PLL is used in frequency synthesizer with 3-tank VCOs, loop-filter. Due to the inclusion of zero-spur phase detector low-spur and high resolution is achieved [15].

In [16] developed fully integrated frequency synthesizer using dual-band quadrature output voltage-controlled oscillator for generating frequencies ranges from 47 MHz to 6 GHz and tuneable transformer-based narrow-band load. This synthesizer can support Multi Band-OFDM and UWB bands with optimal settling time and accommodate wireless standards ranges from 47 MHz to 10 GHz. Ga and Fathima (2015) proposed highly optimized Quadrature Direct Digital Frequency Synthesizer (QDDFS) for SDR wireless applications such as Orthogonal Frequency Division Multiplexing (OFDM) system [17]. This Quadrature based approach rapidly hopping between the various ranges of frequencies with its functionality which helps improved response time. Moreover the sine and cosine values are generated in digital domain to produce appropriate phase and frequency resolution with least complexity overhead [18].

In [19] developed transient PLL with switched capacitors to cover a frequency range of several GHz (>10GHz) for implementing SDR in avionic communication applications. The single mixer based PLL core reduces the settling time into 3.92 μs with suppressed total phase noise. In [20] proposed narrow band PLL which can generates wideband outputs by mixing and dividing. The quadrature single side-band (QSSB) mixer operates in constant loop parameters and passive negative resistance (PNR) during frequency mixing for a superior image side-band rejection ratio (ISRR).

In [21] developed dual-mode VCO with highly optimized automatic frequency calibration (AFC) to implement PLL component. This method also includes multi-phase counter (MPC) accelerates supports configurable band selection which increase the calibration accuracy well as an energy consumption. In [22] introduced fractional-N frequency synthesizer for improved system performance which includes level-shift-less phase frequency detector and a chopping differential charge pump components. Experimental results proves reduction in quantization noise and in-band and out-band phase noises also reduced by 3 dB and 6 dB with root mean square jitter value of 210fs.

In [23] proposed energy efficient ADPLL loop for hybrid-loop receiver (RX) to accomplish interference tolerant Bluetooth communication. This digitalized frequency synthesizer in hybrid-loop structure improves the interference tolerance and allows to digitize frequency-modulated signal without an ADC component. In [24] developed discrete time event-driven compound ADPLL to interconnect as a Cartesian grid like system-on-chip components. The oscillator completely integrated using 65-nm CMOS processing to carry out phase and frequency synchronization over small-scale multiple input multiple-output systems (MIMO).

Digital implementation of ADPLLs and most of its functional blocks are easily configured on Field Programmable

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Gate Arrays to incorporate parallel computation and reconfigurability measures. In [25] utilized binary search algorithm to regulate the locking range of ADPLL over any arbitrary frequency generated during frequency synthesis. Here Coordinate Rotational Digital Computer (CORDIC) is used for phase to amplitude conversion to reduce the hardware complexity overhead and overcome the limitation of exiting Look Up Table (LUT) based implementation.

In [26] introduced quadrature oscillator model which comprises of four low-Q series LC tanks in a ring structure. It reduces distortion levels of delta-sigma architecture and performance rate significantly increased. In [27] increased feasibility and other performance metrics of the ADPLL using digitally controlled ring-oscillator (ring-DCO) design for system-level integration. Both the frequency resolution and the tuning ranges are significantly increased. In [28] developed FPGA based an event-driven all-digital phase locked loop (ADPLL) for asynchronous control. The simulations are carried out using exhaustive test bench to verify individual components of ADPLL networks and statistically comparison with other models in terms of transient response, phase noise and the performance rate.

III. ROPOSED FRAMEWORK

3.1 FREQUENCY SYNTHESIZER ARCHITECTURES

Digital clock Synthesizer is most useful and essential building block in SDR radio where local-oscillator (LO) is used to formulate the information which can be optimally tuned with improved spectrum purity. As shown in Figure1 the generic digital frequency synthesizer (FS) formulate the input frequency and optimally generate the r required frequency ranges. But to meet the performance demands for given local oscillators (LO) specifications is difficult task to reach and the accuracy measure and phase noise accumulation are also high unstable. Any specification driven given local oscillator cannot meet the required performance for different frequency ranges are incorporated. Figure 2 also illustrates the analogy driven Digital clock Synthesizer for SDR system. In most cases, the PLL in any digital synthesizers are comes with VCO and associated signal mixer to generate the various frequency band within its signal tuning range. A wide range of frequency bands are also generated using different types of VCOs. Both analog bound VCO and dual VCO comes with its own merits and drawbacks. But in many real time applications, the PLL based frequency synthesizer are used only one SSB mixer and associated VCO is reducing the system with some notable performance trade-off in energy consumption and frequency tuning range as well.

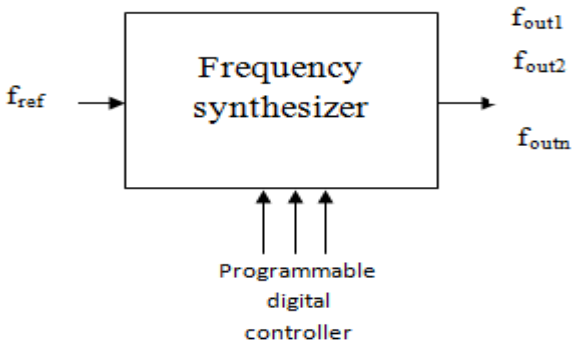

Figure 1 Digital frequency synthesizers

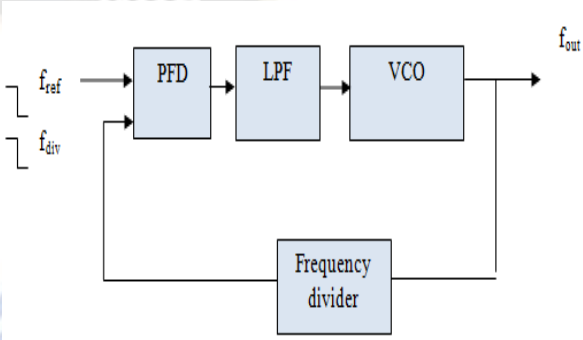

Figure 2 PLL for frequency synthesizer

In SDR systems Frequency Synthesizers are configured as electronic devices to generate wide range frequencies for given input reference frequency and also ensures the stability and spectral measures of the overall system performance. Phase Locked Loops are implemented in different ways namely generic PLL (GPLL), Digital PLL (DPLL), All Digital PLL (ADPLL). Generic PLL are based on analog techniques and digital PLLs consist of both analog and digital components to increase its robustness.

ADPLL has numerous advantages over its counterpart PLL model due to its ability of producing the various range of system clock and formulate the signal exclusively in SDR system. All digital PLL offers more flexibility [29] with reduced sensitivity to process variations. PLLs is generally used to produce the output signal whose frequency is dynamically changes using some programmable units in the range of multiple of an input frequency. PLL also helps conventional to maintain locked condition over the phase and frequency of the input signals. In most cases PLL exhibits some frequency discrimination from its loop filter due to narrow-band tracking characteristics. Moreover the linearity of the voltage-controlled oscillator VCO in PLL also affects the overall linearity of design. Another major limitation of PLL is its parametric constrains over the range of the modulation frequency due to its sensitiveness to low frequency region and its unstable dynamic properties due to its analog components.

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As discussed in section among three methodologies used for designing FS unit direct Digital Synthesizers has numerous advantages over indirect Synthesizers like Phase Locked Loop (PLL) to generate the desired frequency for SDR system in wireless applications. Moreover in digitalized FS the quality of the output directly related to the input signal and hence called Direct Synthesizers. Direct Digital Frequency Synthesizers make use of digital components to produce even frequencies in lower regions with least possible small step sizes. All Digital Phase Locked Loop (ADPLL) [30] is most widely used model used as a Direct Digital Frequency Synthesizer (DDFS) for improved lock-in time. Due to the exclusion of linear analog components both scalability and portability is increased considerably.

3.2 ADPLL

The operating frequency of the fully digitalized SDR frequency synthesizer is largely depends onmethodologies used to formulate the output frequency and feedback loops used frequency divider. Digitalized DCO-based frequency divider arecomprise ofonly digital components which extend its applicability of SDR FS to next generation wireless communication system. The most generic SDR architecture of a FS comes with a replacement of analog driven VCO to regulate the phase difference between input reference frequency and generated frequency. The most common SDR frequency synthesizer ADPLL block diagram comprise of main components in its FPGA implementation which includes: voltage-controlled oscillator (VCO), phase frequency detector (PFD), and programmable divider as shown in Figure 1. The division ratio N is formulated using highly reconfigurable frequency dividerwith phase match as follows,

$N = P \times M.$

The accumulation of a prescalerincludes the performance improvement comes with digitalized reconfigurable frequency divider. In this work, a noveldigitalized SDR FS based on improved frequency tuning range and maximal coverage. The proposed SDR FS comprise of phase detector, digitalized frequency controller (DCO), configurable frequency divider which can support SDR system to wide range of applications.

3.3 PHASE-FREQUENCY DETECTOR

In PLL based frequency synthesizer VCO is the most predominant building block that affects the overall system performance both in terms of jitter and phase noise. A resonant VCO with an LC tank offers notable performance metrics in above mentioned measures, but this type of VCO model is not suitable for monolithic hardware implementations and also demands the integration of several external digital components. Moreover the on-chip implementations of inductors provides low quality factor (Q). As a replacement to LC components and mitigate the problem over jitter sensitive applications ring oscillators are effectively used in most cases as an integrated component.

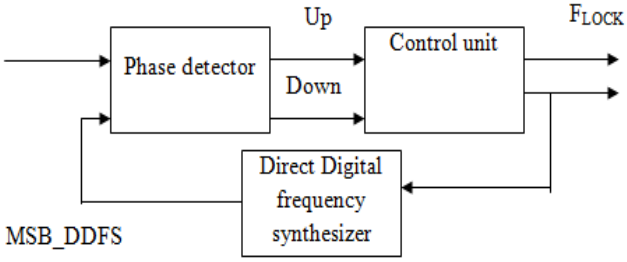

Figure 3 Block of digital frequency synthesizer system

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In particular for mobile applications, lock time is the essential measure to support fast exit and entry over dynamic power management. ADPLLs have inherent fast frequency locking and its digitization characteristics improve the system stability. To generate the required pulse output Direct Digital Frequency Synthesizer (DDFS) is acted as basic building blocks and decides various performance metrics which include 1. Improved Lock Time 2.Wide tuning Range 3.Reduced complexity overhead 4.Energy efficiency.

3.4 EXPERIMENTAL SETUP

Here top down digital design model is used to integrate all basic building blocks of proposed ADPLL which are described in Verilog HDL and synthesized in Quartus II EDA FPGA synthesizer with cyclone II family EP2C50F484C6 device. Initially by using model functional verification is carried out using exhaustive test bench input stimulus. Both variable rate clock dividing capabilities and all other inherent properties like phase match constraints and associated phase synchronization are well proved using simulation results.

IV. SIMULATION RESULTS

Here to validate the performance metrics of configurable delay line in phase synchronization measure and the iteration limits associate to phase error accumulation are verified in all stages during matching process over various clock rates. And the overall system re-configurability and scalability are well proved with its counter unit adaptability as per the required adoptive frequency range of ADPLL and the appropriate lock time. Based on modulo-2 operation phase differences are evaluated as shown in Figure 4.

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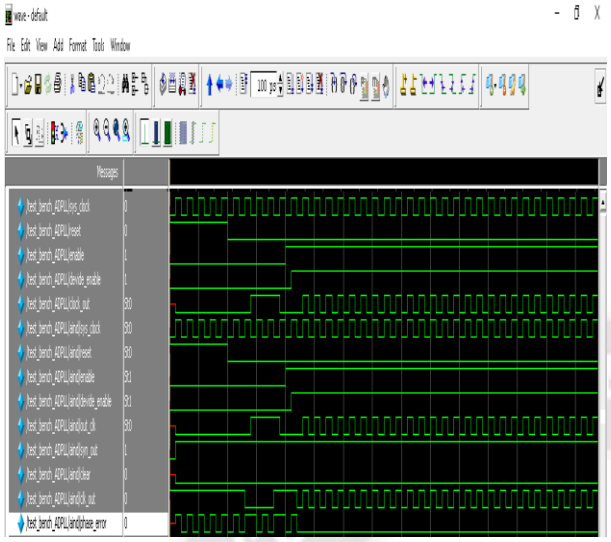

Figure 4 Phase Detector Output

4.1 FS SYSTEM SYNTHESIS RESULTS

Synthesize results of proposed frequency synthesizer proved that the overall complexity reduction at logic register's level and Logic element utilization levels; and also achieves significant performance improvements. From the timing report, it is proved that the proposed FS core offers significant data rate improvement as shown in Table 1 which includes both settling time and number of configurable elements for phase matches. It is also proved that proposed synthesizer unit reduces the path delay considerably over conventional FS model. Here delay is optimized by reducing both path delay which arise during comparison and critical path delaythat accumulates during delay state transition.

Table 1 Reconfiguration vs. locked time

Frequency divider (N) value	Settling time	Number of Buffer chain used
10	2.67ns	17
20	3.53ns	31
30	4.03ns	44
40	4.51ns	57
50	5.42ns	71

In real time applications the overall system performances of any DS is degraded with associated system integration which is also needs to overcome any types of sequential state transition models and associated pattern length. Here buffer enabled phase matching model associated in SDR system model gives improved system performance and frequency dependent state transition operations. Here the path delay propagation is also reduced which results with overall critical path reduction in both forward and backward data path. The time quest timing analyzer tool is introduced to compute the maximum operating frequency of given input digital design. Here due to the accumulation of phase synchronized phase matching process over global clock generation is suppressed and solved using input clock rate driven validation check. Here FPGA hardware synthesize results are used to validate the system performance along with computation complexity reduction and associated resource utilization; in addition to this the proposed DFSS in fully digitalized SDR system offers significant performance improvements. From the performance report, it is validated that the proposed DFSS design comes with significant performance improvement

The critical path accumulated in proposed frequency synthesizer blocks for given DDFS is used to evaluate the maximum operating frequency report as a measure of worst case critical path during data propagation. From the settling time results it is proved that the proposed ADPPL offers improved performance efficiency and its performance gap will increase narrowly with divider rate as shown Figure 5 since the number of delay lines required for post phase match is directly related to the number of stages used in phase matches. Moreover due to sequential operation iteration counts has direct impact over critical path delay. It is found that the proposed ADPLL reduces the critical path delay significantly over the conventional FS architecture.

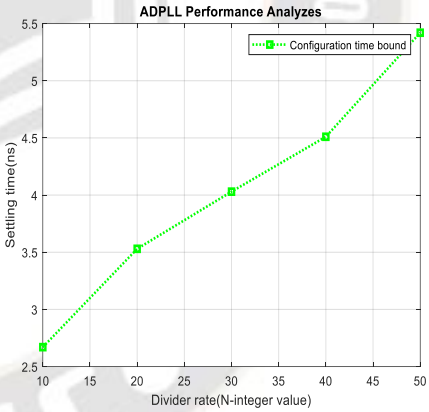

Figure 5 Settling Time Trade Off Analyzes

4.2 COMPUTATIONAL COMPLEXITY OVERHEAD

This experimental result also illustrates the difference in design complexity for proposed hardware optimization through resource sharing and ADPLL model over architecture level optimization. Besides the reduced arithmetic complexity, the effective implementation of the proposed FS model also benefits with improved throughput rate with sequential transition model. Exclusion of pipelining schemes avoids latency related problems during system integration. Finally, the

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post synthesis placement mapping model proved to be hardware efficient one as shown in Figure 6.

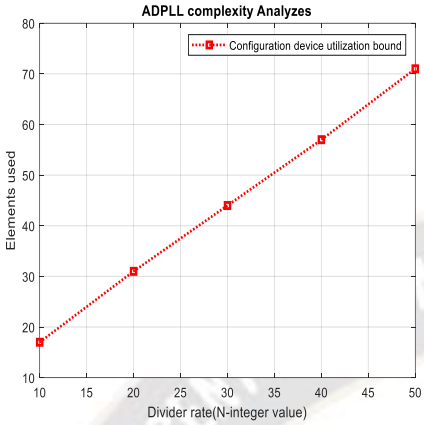

Figure 6 Complexity Overhead Analyzes

Table2 Synthesis details of proposed DCO

Parameter	Measures
Logic element used	672
LUTs	500
Power dissipation	178.09mW

4.3 STATE-OF-THE-ART COMPARISON WITH OTHER FS

The overall system performance of SDR system is also depends on latency measures and tolerates in wireless applications. In frequency synthesizer the computational time takes for the exact reconfiguration set to generate the desired output frequency signal and its integrity leads latency overhead problem. Here at first the synthesizer is designed to run at a peak operating clock frequency with improved frequency tuning range as compared to its counterpart state-of-the-art model as shown in Table 3. During frequency synthesis ADPLL generates frequency that can be changed at run-time using configurable delay chain and simplified reconfigurable units

which meet hardware requirements and energy constraints of FS system. The performances of various synthesizers are compared in Table 3.

Table 3 FPGA state-of-the-art comparison with other ADPLL models

Methodology used	FPGA device used	Frequency tuning range
Ring-DCO (Radhapuram et al. (2019)	Xilinx Zynq/ 7010	120 MHz to 300 MHz
Reconfigurable delay lines-DCO	ALTERA Cyclone II/EP2C50F484C6	50 MHz to 451.47 MHz

V. CONCLUSION

In this section, a novel ADPLL frequency synthesizer is proposed for high performance SDR system and its extensive performance metrics in terms of complexity reduction, memory efficiency and throughput rate are presented. Reconfigurable buffer chain enabled concurrent phase matching is incorporated for both parallel computation and reconfigurable dynamic updation. The hardware synthesis results indicated that our proposed ADPLL model offers the 70% and 50% frequency tuning resolution in lower and higher region respectively as compared to existing ring counter enabled DCO and also mitigate both memory constraints and computational complexity with its simplified configurable buffer chains. The performance metrics of the proposed high speed CONFIGURABLE DCO models is compared to other state-of-the-art CONFIGURABLE and DCO models.

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