International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

Design of Hybrid Full Adder using 6T-XOR-Cell for High Speed Processor Designs Applications

Venkat Subba Rao.Manchala [1*], Satyajeet Sahoo[2] , G.Ramana Murthy[3].
[2]Senior IEEE-Member
[1]venkat.manchala111@gmail.com;[2]satyajeetsahoo.eltc@gmail.com;[3]ramana.murthy@alliance.edu.in.
[1,2]Vignan's Foundation for Science, Technology & Research (VFSTR)-522212
[3]Alliance University – Bangalore
*Corresponding Author (Tel: +91-6304947590, venkat.manchala111@gmail.com)

Abstract
Hybrid-logic implementation is highly suitable in the design of a full adder circuit to attain high-speed low-power consumption, which helps to design n any high speed ALUs that can be used in varies processors and applicable for high speed IoT- Application. XOR/XNOR-cell, Hybrid Full Adder (HFA) are the fundamental building block to perform any arithmetic operation. In this paper, different types of high-speed, low-power 6T-XOR/XNOR-cell designs are being proposed and simulated results are presented. The proposed HFA is simulated using a cadence virtuoso environment in a 45nm technology with supply voltage as 0.8V at 1GHz. The proposed HFA consumes a power of 1.555uw, and the delay is 36.692ns. Layout designs are drawn for both 6T-XOR/XNOR-cell, and 1- bit HFA designs. XOR/XNOR-cells are designed based on the combination of normal CMOS-inverter and Pass Transistor Logic (PTL). Which is used in the design of high end device processors such as ALU that can be implemented for the IoT- design applications?

Keywords: Hybrid Full Adder(HFA);Low-Power high Speed;PassTransistor Logic (PTL);Transmission Gate(TG);Transmission Function Adder (TFA); Complementary-pass transistor logic(CPTL); Process-Voltage-Temperature(PVT);Power-delay Product (PDP); Energy-delay product(EDP);Dynamic Power.

1 Introduction

Current trends in innovation and creativity in designing equipment or devices need an emphasis on certain qualitative acknowledgment by designing processors such as high end Computers and Portable design applications (PDAs) occupy a key factor for the development of modern electronic Technology [1]. The usage of these electronic gadgets is increasing day by day and has also become every household part and parcel of life becoming an integral part of every human life[2],[3],[9]. Research in the field has been a continues and Designers are busy and striving hard for developing new devices that have a feature of low-power consumption, are of small in size, high speed, energy-efficient[1],[8] 15]. Mostly, every electronic system comprises arithmetic circuits; an adder is the fundamental building element of these for any ALU- operations such as addition, subtraction, and multiplication processes [10], [14]. Therefore, power and delay are the two key performance parameters in any given electronic circuit. Nevertheless, improving the speed adder design enhancing the performance of the adders would significantly improve the entire system operation1-3],[13],[22].

2 Literature Review

2.1 HFA-Design

'Hybrid' is defined as the combination of more than one logic is used to implement a FA design [1],[10].HFA-design comprising of three modules. Module-I represents the XOR/XNOR-cell design, and Module-II depicts the design of TG and implementation of the 'SUM'. and Module-III depicts the design and implementation of 'Cout'. The advantage of HFA design when compared to CMOS and PTL logic is that it achieves higher speed and displays full swing output voltage [1]. Hence, the usage of this HFA design demand is rapidly growing in modern electronic devices as mensioned in Fig.1.[1][10],[15].

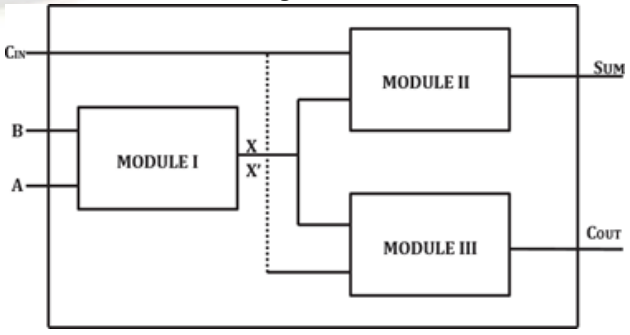


Fig.1:Module level HFA-design [1],[3]

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

2.2 Hybrid full Adder design-18T: The logic used in the design of HFA are, i)Conventional CMOS-logical, and ii)C-PTL-logic. The feature of 18T-HFA is to produce a full swing output and maintain high speed [12]. The performance parameters such as power and speed are improved [15] [19]. The bottleneck in the implementation of PTL-logic is mainly due to Module-I, which consists of positive feedback connections in the output, and also affects efficiency in terms of speed [15]. Thus, increasing the delay due to the presence of an internal node occurs. Generally, usage of NOT (PMOS) gates in any design, increases the delay in the circuit. Thus, it reduces the speed of the operation. To overcome these limitations, a new hybrid adder design is considered [17]. Which is depicted in the below figure-2.

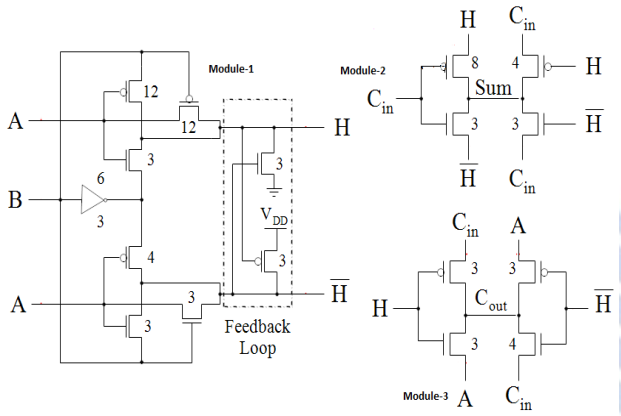


Fig.2:18T- HFA-Schematic [33]

2.3 Hybrid Full Adder design 18T- Transistors: HFA-design uses the implementation of CMOS, and TG-logics [1],[2]. XOR-cell is the major power-consuming section in any of the given FA designs [4-7], [13]. The speed of the operation is more due to the use of TG [6]. The major advantage of HFA is that it enables full swing output voltage and yields a high speed of operation. However, this design consumes more power due to the high transistor count mentioned in the Fig.3 shown below.

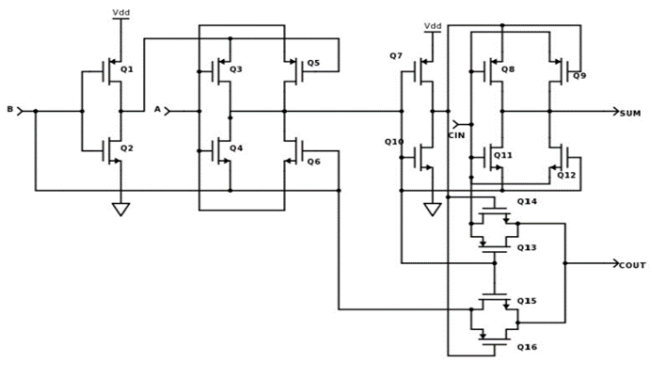


Fig.3: Schematic diagram-16T-HFA [9]

2.4 Hybrid Full Adder design-13T: The existing HFA-design needs 13T- transistors that are used for generating the output for all input combinations. XOR-cell is designed based on PTL-logic with 3T- transistors [21][27]. However, reducing the transistor count affects power consumption and enhances energy efficiency levels [34]. Typically, to attain the full swing output voltage at XOR-cell, it needs 6T-transistors [5][9][18]. The limitation and the bottleneck are due to the non-presence of supply rail (Vdd) at the pull-up of a network. As shown in Fig.4. [1-3],[7].

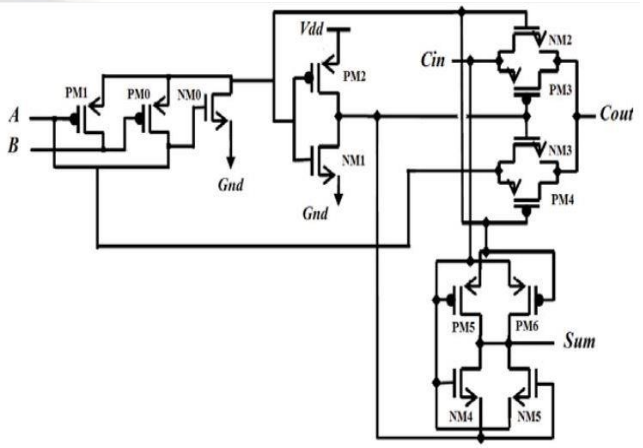


Fig.4: Schematic diagram-13T-HFA-design [34]

2.5 XOR-Gate -3T: This XOR-cell is developed by modified version of conventional CMOS-inverter. It behaves like a normal inverter, when input terminals A=0, B=1. Hence, the resulting output at C is logic-high. When, input B is at Logic-low, output at the CMOS inverter is at logic- high stage. However, when transistor T_3 is in the 'ON'– state the output resembles input A while, input A is at logic-low, and input B is at Logic-high, the voltage degradation problem occurs due to a drop in the threshold voltage at the transistor M_3. Therefore, the output at C, i.e., degraded voltage. This voltage degradation problem mainly exists due to PTL logic implementation. as shown in Fig.5 [14-15].

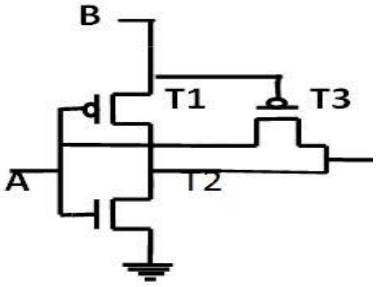


Fig.5: XOR-3T- Gate- Schematic [33]

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

3 Design Methodology

3.1 Proposed 4T-XOR Design:

The proposed design consists of 4T- transistors, which are parallelly arranged with each other.A, B,and C are the input and output terminals respectively.This design is simple and symmetrical.

3.1.1 Proposed XOR-design operation: T_1, T_2transistors of PMOS and NMOS respectively are used for its implementation as an inverter. Transistors T_3 and T_4 are PMOS and NMOS transistors are arranged in a parallel manner. Gate terminals of T_3 and T_4 transistors are sorted and attached to the input as shown in Fig-6. When the input A =0, B=0, transistors T_1 and T_3 are in ON-state (i.e., closed switch), and T_2, T_4 transistors are in 'OFF'-state (i.e., open switch). Hence, output 'C', remains at a logical low. A=1, B=1, transistor T_2, T_4 are in 'ON'-state (i.e., closed switch), and T_1, T_3transistors are in OFF-state (i.e., open switch), the output C is at logic-low. If inputs A=0, B=1, transistor T_1, T_4 are in ON-state. The transistors T_2 and T_3 are in OFF-state, therefore, the conducting path happens by T_1, T_4. The output 'C' is at Logic-High. Likewise, input A=1, B=0 iteration, transistor T_2, T_3 is ON -state, and transistors of T_1, T_4 is OFF-state. Hence, transistor T3 only provides the conduction path through the critical path. The output 'C' is at logic high. shown inFig.6.[1013].

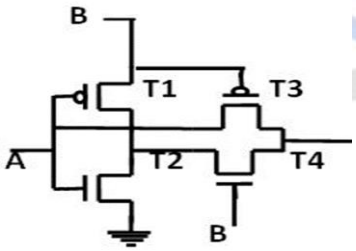


Fig.6: XOR-4T- Gate- Schematic

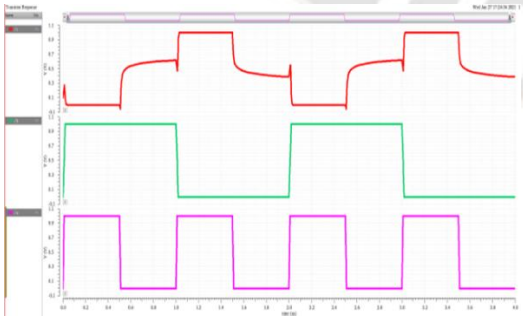


Fig.7 : XOR-4T- Gate- Timing diagram

3.2 Proposed 6T-Xor-Design:

a) The proposed 4T-XOR design suffers due to full swing output voltage which is evident from fig.7 that occurs due to PTL -Logic. To overcome these limitations a modified design is created as shown in fig.-8(a), Which has an additional transistor of PMOS (T_5) and NMOS transistor (T_6) are used as a 'restorer'. T_5, T_6 gate terminals are connected to input A. This 'restoration' process of transistors produces the full swing voltage [13].

b)To enhance the limitations presented in the fig.8(a) the design is changed as per the requisite norms as shown in fig.8(b). Here, transistors T_5, and T_6 of the gate terminals are connected in cross-coupled to improve full swing output voltage. However, it fails to produce full swing output voltage when compared to fig 8(a)

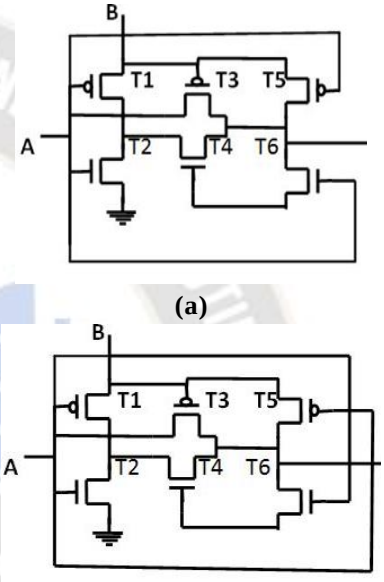
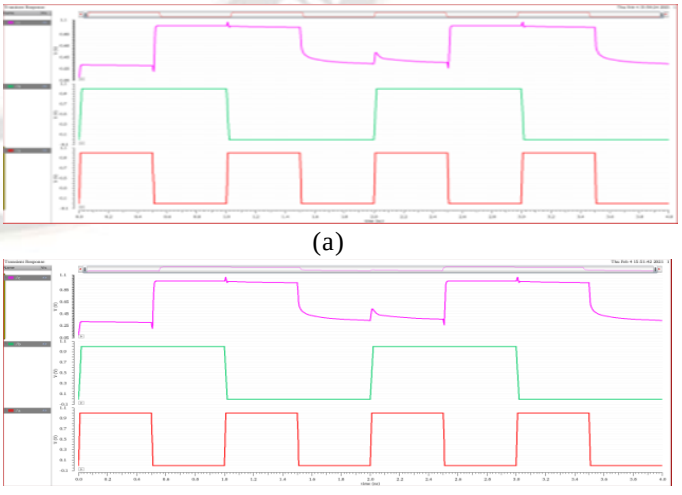


Fig.8 (a), (b) : XOR-6T- Gate- Schematic

3.3 Output waveform



(a)

(b)

Fig.9 (a), (b): Timing diagram

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

3.3 Proposed 4T-Hybrid Adder Design:

The proposed HFA-design is implemented using three logical modules as shown in Fig-10. The 4T-XOR module is used to generate 'XOR' output, and TG- the logic module is used to achieve full swing voltage and high-speed operation [12]. The TG logic has the advantage of low-short circuit power and high speed, and Module-3 is a 'Level Restorer' for the generation of the 'SUM. As shown in Fig.10.[13].

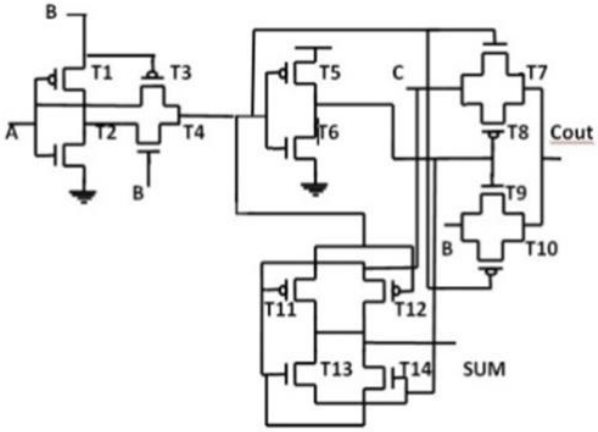


Fig.10: Schematic diagram4T-XOR-based 1-bit HFA

3.5 Output waveforms:

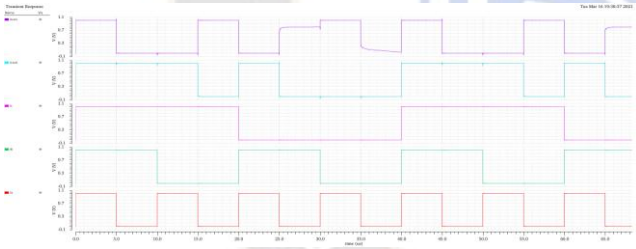


Fig.11: 4T- based Hybrid Full Adder Timing diagram

3.6 XOR Gate-6T- based Full Adder: The proposed HFA- design fails to produce full swing voltage for the input combination A=0, B=1, C=0. as shown in fig.12 This limitation arises due to Pass Transistor Logic (PTL). To overcome this issue, the proposed circuit is further modified by introducing an additional Transistor T_5, T_6which acts as a 'restorer ' to produce full swing output voltage for all the input combinations as shown in fig.12

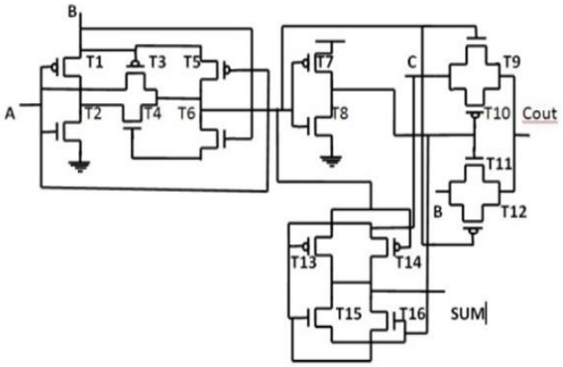


Fig.12 :Schematic diagram 6T-XOR-based 1- bit HFA

4.0 Proposed Hybrid Adder 16T-Design: To overcome the limitation in 6T-XOR-based 1-bit HFA as shown in fig.12, 16T- HFA is newly proposed, that generates full swing output voltage. It is achieved by connecting the source terminal of PMOS (T1)- transistor to the supply rail (Vdd) as shown in fig 13. T_1 and T_2 transistors combination behave like a normal CMOS inverter. T_2, T_3pass transistors are arranged parallelly, where both the gate terminals are sorted and thereby connected to input B. Transistors T_5, T_6 are used as 'restorers'. Hence, the output of the XOR gate produces full swing voltage. The output waveform depicts the 'Sum' and 'Carry' outputs for all input combinations, which revealed full swing output voltage and maintained high speed. As shown in Fig.13 and layout designs for XOR/XNOR designs are presented in Fig.15 and Fig.16. [15],[40].

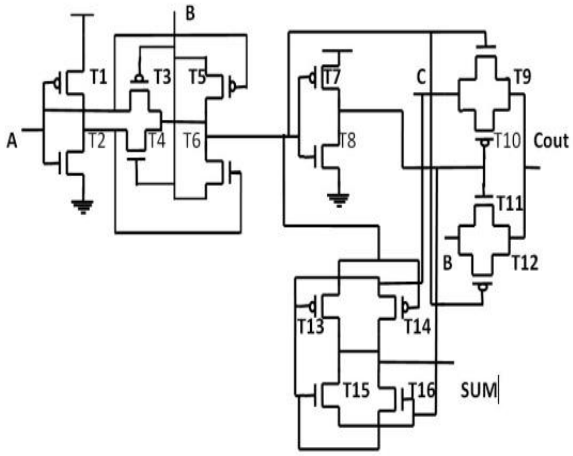


Fig.13: Proposed Schematic diagram6T-XOR-based HFA

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

4.1 Output waveform:

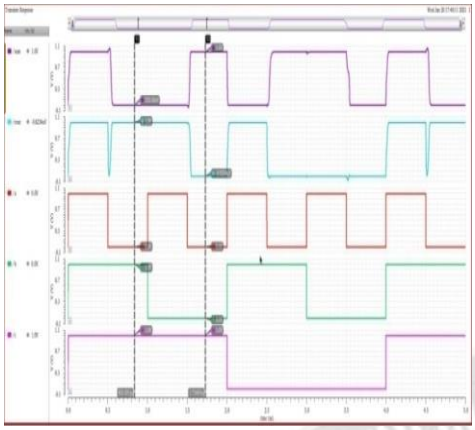


Fig.14: Output waveform -6T-XOR-based HF

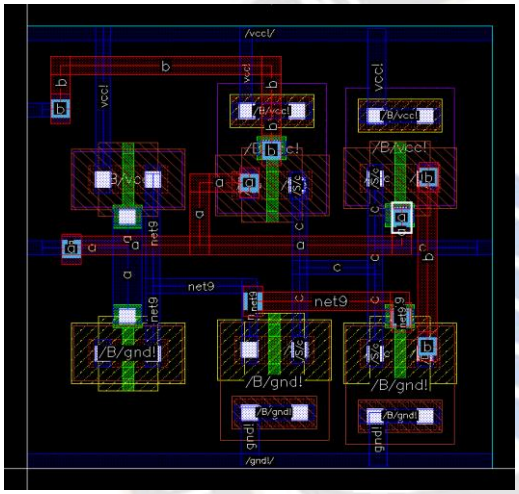


Fig.15: Layout Diagram for Proposed 6T-XOR gate in 45nm Technology at 1GHz

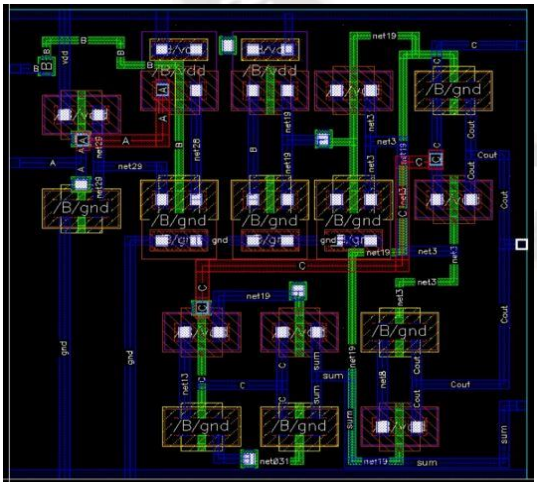


Fig.16 : Layout Diagram for Proposed 16T-Hybrid-Full Adder (HFA) in 45nm Technology at 1GHz

4 Result and Discussion

The proposed XOR/XNOR design simulation results are observed in the supply voltage 1.0 at a frequency of 1GHz.as shown in the Table.1 and Table.2 as shown below.

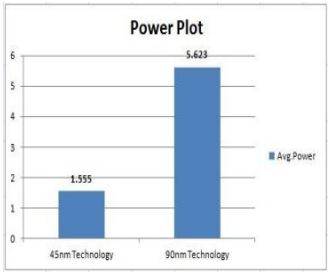
Table -1: Explains the 6T-XOR,1- bit HFA Layouts and its analyzed reports for the amount of are occupying.

Design	Units	Technology	Supply voltage(V)	Area
Proposed XOR-CELL-6T	nm	45	1.0	3.439
Hybrid Full Adder-(HFA)	nm	45	1.0	9.641

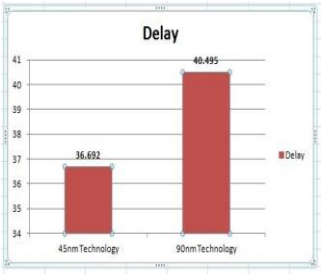
Table.-2: The efficiency of 1- bit hybrid full adder design in terms of Power,Delay,PDP,EDP can be calculated in both 45nm node and 90nm node at a frequency of 1GHz [13].

S.No	Performance Parameters	Units	Technology 45nm	Technology 90nm
1	Voltage	V	1.0	1.2
2	Frequency	GHz	1.0	1.0
3	Power	uW	1.555	5.623
4	Delay	ps	36.692	40.495
5	PDP(Power x Delay)	e-18 Joules	0.05705	0.2276
6	EDP(Delay x PDP)	e-27 joules	2.093	9.218

The Fig.17 a), b), c),d).shows the power, delay, PDP, EDP of a proposed HFA in cadence virtuoso tool of 45nm, 90nm respectively with a source voltage of 1.0V with 1GHz. it is observed that the Power is 1.555uW,delay is 36.692 ps, PDP 0.0577A(fJ), EDP(2.093) respectively, which gives the better performance results compared to the existing design

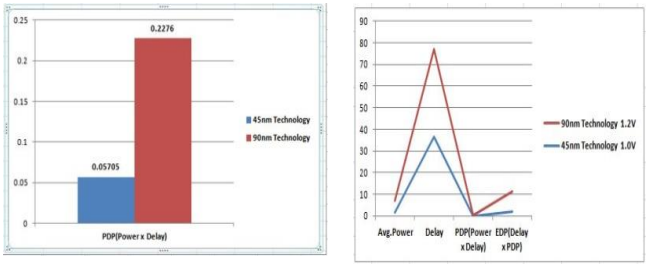


(a) Power consumption



(b) Delay of HFA

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*



Pictorial Representation of (c) **PDP,** (D) Analysis of **Performance Parameters** in 45nm,90nm Technology.

5 Conclusion

The proposed HFA design has been developed based on the Inverter, pass transistor, Level Restore logics, which can be used in high speed and low power consumption designs. A total of 16T- transistors are needed to complete the design for the proposed 1- bit HFA. It is simple and symmetrical, also the best suitable design for low-power consumption applications. The major advantage of this proposed design is to overcome the existing design problems because it did not include or have any cross-coupled connections that resulted in reducing delay, short-circuit power, and leakage power in the design. Performance parameters of the proposed 1-bit HFA-Power, Delay, PDP, and EDP are simulated in 45nm, and 90nm technology nodes and the results area accordingly tabulated. The area occupied by XOR-cell,1-bit HFA in 45nm node with a supply voltage rail (V_{dd}) at 1.0 volts is 3.439 nm^2,9.641 nm^2 respectively presented. This proposed design overcomes all those limitations and bottlenecks with sophisticated results. Hence, the proposed design achieves high speed with full swing. This design is best-suited one for high-speed low-power consumption devices.

6 References

[1]. Jyoti Kandpal, Abhishek Tomar, Mayur Agarwal, and K. K. Sharma (2020) -" High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell-IEEE *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 28(6), pp-1413-1422.

[2]. Mehedi Hasan, Md. Jobayer Hossein, Mainul Hossain, Hasan U. Zaman, and SharnaliIslam (2020)-" Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation"- *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 67(8), pp-1464-1468, .

[3]. Hareesh-Reddy Basireddy, Karthikeya Challa, and Tooraj Nikoubin-" Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures" (2019) - *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Vol. 27(5), pp-1138-1147.

[4]. K. Haghshenas, M. Hashemi, and T. Nikoubin, (2018) "Fast and energy-efficient CNFET adders with CDM and sensitivity-based device-circuit co-optimization," *IEEETrans.Nanotechnol.*,vol.17(4), pp.783–794,

[5]. T. Nikoubin, M. Grailoo, and C. Li,(2016) "Energy and area-efficient three-input XOR-CELLs with systematic cell design methodology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 24(1), pp. 398–402.

[6]. Shubhajit Roy Chowdhury, Aritra Banerjee, Aniruddha Roy, Hiranmay Saha (2008) –"A high Speed 8 Transistor Full Adder Design Using Novel 3 Transistor XOR Gates International Journal of Electronics and Communication EngineeringVol: 2(10),

[7]. R. M. Anacan and J. L. Bagay, (2015)"Logical effort analysis of various VLSI design algorithms," in *Proc. IEEE Int. Conf. Control Syst., Comput. Eng. (ICCSCE)*, George Town, Malaysia, pp.19–23.

[8]. P. Pramod & T. K. Shahana-" Delay and Energy Efficient Modular Hybrid Adderfor Signal Processor Architectures"- IETE Journal of Research.

[9]. Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar, and Anup Dandapat (2015)" Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit- *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*, 23(10) pp-2001-2008.

[10]. Sameer Goel, Ashok Kumar, and Magdy A. Bayoumi, *Fellow, IEEE-"* Design of Robust, Energy-Efficient Full Adders for Deep- Submicrometer Design UsingHybrid-CMOS Logic Style- *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*, VOL. 14(2) ,2008.

[11]. Venkat Subba Rao.Manchala,Ramana Murthy.Gajula "Low-Power and Low-Leakage Design Techniques in CMOS T echnology" Proceedings of the Fifth International Conference on Trends in Electronics and Informatics (ICOEI). IEEE Xplore Part Number:CFP21J32-ART; ISBN:978-1-6654-1571-2

[12]. Venkat Subbarao.Manchal,Satyajeet Sahoo, G.Ramana Murthy."Design and analysis of 16- bit spares kogge stone adder with proposed 6T-XOR cell, 1- bit HFA design for high speed Arithmetic operations".2022 International Conference on Communication, Computing and Internet of Things (IC3IoT) | 978-1-6654-7995-DOI: 10.1109/IC3IOT53935.2022.9767976.

[13]. Venkat Subbarao.Manchal,Satyajeet Sahoo, G.Ramana Murthy."Design and analysis of Novel XOR/XNOR Based Hybrid Full Adder for IoT- Applications 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021) -978-1-6654-6633- IEEE DOI: 10.1109/ICRTCST54752.2022.97819. Sahoo, S. and Prabaharan, S.R., 2017. Nano-ionic solid state resistive memories (re-RAM): A review. *Journal of nanoscience and nanotechnology*, *17*(1), pp.72-86.DOI-10.1166/jnn.2017.12805.

[14]. Sahoo, S., Manoravi, P. and Prabaharan, S.R.S., 2019. Titania Based Nano-ionic Memristive Crossbar Arrays: Fabrication and Resistive Switching Characteristics. *Nanoscience & Nanotechnology-Asia*, *9*(4), pp.486-493.DOI:https://doi.org/10.2174/2210681208666180628l2

2146.

[15]. Sahoo, S., 2021. Conduction and switching behavior of e-beam deposited polycrystalline Nb2O5 based nano-ionic memristor for non-volatile memory applications. *Journal of Alloys and Compounds*, *866*,p.158394.DOIhttps://doi.org/10.1016/j.jallcom.2020.158394

[16]. Masoud Pashaeifar, Mehdi Kamal, Ali Afzali-Kusha, and Massoud Pedram(2018)"Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications"- *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*, 26(11), pp-2530-254,

[17]. Sana pala, Ramachandran Sakthivel,*(2019)* "Ultra-low-voltage GDI-based hybrid full adder design for the area and energy-efficient systems"-IET Circuits, Devices & Systems, Vol. 13 (4) pp. 465-470

[18]. K.Navi, V.Foroutan, M.RahimiAzghadi, M.Maeen, M.Ebrahimpour, M.Kaveh, O.Kavehei (2009)" A novel low-power full-adder cell with a new technique in designing logical gates based on static CMOS inverter-Microelectronics Journal 40 (2009), pp-1441-1448

[19]. H. Naseri and S. Trimarchi,(2018) "Low-power and fast full adder by exploring new XOR and XNOR gates," *IEEE Trans. Very Large Scale. Integer. (VLSI) Syst.*, vol. 26(8), pp. 1481–1493, Aug.2018.

[20]. M. Amini-Valashani, M. Ayat, and S. Mirzakuchaki, "Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder," *Microelectron. J.*, vol. 74, pp. 49–59, Apr.2018.

[21]. M. A. Valashani and S. Mirzakuchaki (2016), "A novel fast, low-power and high-performance XOR-XNOR cell," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp.694–697.

[22]. M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H.Nabovati, and A. Golmakani,(2011) "Design of new full adder cell using hybrid-CMOS logic style," in*Proc.18thIEEEInt.Conf.Electron.,Circuits, Syst.*, Dec.2011, pp.451–454

[23]. C.-H. Chang, J. Gu, and M. Zhang (2005) "A review of 0.18-μm full adder performances for tree-structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695.

[24]. A.P. Chandrakasan, S.Sheng,andR.W.Brodersen,(1992) "Low-power CMOS digital design," *IEICE Trans. Electron.*, vol. 75(4), pp. 371–382, 1992.

[25]. R. Zimmermann and W. Fichtner(1997) "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul.1997.

[26]. M. Aguirre-Hernandez and M. Linares-Aranda,(2011) "CMOS full-adders for energy-efficient arithmetic applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 718–721.

[27]. V. Foroutan, M. Taheri, K. Navi, and A. A. Mazreah,(2014) "Design of two low-power full adder cells using GDI structure and hybrid CMOS logic style," *Integration*, vol. 47, no. 1, pp. 48–61.

[28]. M. Agarwal, N. Agrawal, and M. A. Alam (2014) "A new design of low-power high-speed hybrid CMOS full adder," in *Proc. Int. Conf. Signal Process. Integer. Netw. (SPIN)*, pp.448–452.

[29]. M. Vesterbacka(1999) "A 14-transistor CMOS full adder with full voltage- swing nodes," in *Proc. IEEE Workshop Signal Process. Systems. Design Implement. (SiPS)*, pp.713–722.

[30]. H. Tien Bui, Y. Wang, and Y. Jiang(2002) "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," *IEEE Trans. CircuitsSyst.II, AnalogDigit.SignalProcess.*,vol.49(1),pp.25–30, 2002.

[31]. M. Zhang, J. Gu, and C.-H. Chang (2003) "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*,vol.5,May2003,p.5.

[32]. P. Malini G. Naveen Balaji K. Boopathiraja (2019)-"Design of Swing Dependent XOR-XNOR Gates based Hybrid Full Adder"- 2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS)-pp-1164-1170

[33]. A.P. Chandrakasan, S.Sheng,andR.W.Brodersen (1992) "Low-power CMOS digital design," *IEICE Trans. Electron.*, vol. 75, no. 4, pp. 371–382, 1992.

[34]. D. Radhakrishnan,(2001)"Low-voltage low-power CMOS full adder," *IEE Proc.-Circuits, Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[35]. M.Geetha Priya1, Dr.K.Baskaran2, D.Krishnaveni,(2012)-Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications- International Conference on Communication Technology and System Design 2011- Elsevier-Procedia Engineering pp: 1163 – 1170.

[36]. **[36]** Bagyalakshmi K, M. Karpagam(2020).-"Performance enhancement of efficient process based on Carry-Skip Adder for IoT applications"- Microprocessors and Microsystems- Elsevier -Contents lists available at Science.

[37]. Manan Mewada, Mazad Zaveri, Rajesh Thakker (2019)."Improving the performance of transmission gate and hybrid CMOS Full Adders in a chain and tree structure architectures"- Elsevier-Integration, the VLSIJournal-0167-9260/2019- Elsevier.

[38]. MajidAmini-Valashani, MehdiAyat, SattarMirzakuchaki (2018) "Design and Analysis of a Novel Low power and energy -Efficient 18T Hybrid Full adder" - Micro Electronics Journal- Elsevier Volume-74(5), Pages 49-59.

[39]. Salam Surjit Singh, Dolly Leishangthem, Md. Nasiruddin Shah ,Biraj Shougaijam. "A Unique Design of Hybrid Full Adder for the Application of Low Power VLSI Circuits".Fourth International Conference on Electronics, Communication and Aerospace Technology (ICECA-2020) IEEE Xplore Part Number: CFP20J88-ART; ISBN: 978-1-7281-6387-1.

[40]. Sahoo, S., 2021. Conduction and switching behavior of e-beam deposited polycrystalline Nb2O5 based nano-ionic

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 10 Issue: 1s
DOI: https://doi.org/10.17762/ijritcc.v10i1s.5900
***Article Received**: 10 October 2022 **Revised**: 19 November 2022 **Accepted**: 09 December 2022*

memristor for non-volatile memory applications. *Journal of Alloys and Compounds*, *866*,p.158394.DOIhttps://doi.org/10.1016/j.jallcom.2020.158394.

Mr.Venkat Subba Rao Manchala received a B.E degree from RVR & JC College of Engineering under affiliated with Nagarjuna University in the year 2009, Andhra Pradesh, India. Firstly joined as a Telecom Engineer with a role of RF-Drive Test for Ericsson/NSN in the Delhi region. Secondly Joined HBL(Hyderabad Batteries Limited)-Power Electronics division - Sharmeerpet-(Hydera bad) industry with an experience of 5-years as a Quality Analyst (QA) and R& D for Mother board design division during the time of 2010-2015. Later received an M. Tech degree from Sri Venkateshwara College of Engineering and Technology Andhra Pradesh in 2018. Currently working as a Research Scholar in VLSI -Design From Vignan's Foundation for Science, Technology & Research. (VFSTR), Vadlamudi, Guntur. My research interests include VLSI, Embedded Systems, Low-power design, FPGA, and IoT related to VLSI Applications.

Thanks and regards.

Dr. Satyajeet Sahoo is currently an Assistant Professor with the department of Electronics and Communication Engineering at the Vignan's Foundation for Science, Technology and Research, Guntur, India. He completed his M.Tech. in VLSI Design in 2014 as well as his PhD in Nano Solid State Memories in 2019 from VIT University, Chennai Campus. His research interests include analog IC design, design and fabrication of Memristive devices.

Thanks and regards.

Prof. Dr. G. Ramana Murthy C. Eng, MIET, SMIEEE received B. Tech degree from Nagarjuna University, Andhra Pradesh, India in 1990, M. Tech degree from G.B. Pant University of Agriculture & Technology, Uttar Pradesh, India in 1993, and Ph.D. from Multimedia University, Malaysia, and secured a grant from Telekom Malaysia in 2019. Currently, he is working as Professor in the Electronics and Communication Engineering Department at Alliance university - Bangalore-India. His main research interests include VLSI, Embedded Systems, Nanotechnology, Memory optimization, low-power design, FPGA, and Evolutionary Algorithms. This grant was secured by him in 2019 May from TMR&D.