

A New Subthreshold Current-Mode Four Quadrant Multiplier

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Abstract— This paper presents a novel current mode four quadrant multiplier. A pair of sub threshold translinear loops and current conveyors are the basic building blocks in realization scheme. The proposed multiplier features simplicity, low power dissipation. The salient features of this approach are; it's single ended inputs; since it uses sub threshold region of operation, this make the design interesting for low power application; current mode application yields large dynamic range and low power dissipation.

Keywords— *analog multiplier; current mode; translinear circuit.*

I. INTRODUCTION

The analog multiplier is the basic building block of analog signal processing circuits and draws much importance in this fast growing market of communication systems. Today's market need is to develop efficient portable devices that has stimulated the VLSI world to create low power devices with superior performance and lower cost. Low power consumption hence has become an important designing parameter. CMOS technology is the most developed technology for integrated circuits implementation [1][2]. Many multiplier circuits have been proposed in the literature [3] [4] [5] [6]. Several works use low power design technique & using CMOS technology [7][8][9]. The floating gate MOS technology [10], well input and source degeneration method [11], differential input [4]. However these methods suffer from increased processing steps or input impedance. The differential input technique leads to additional hardware uses. The current-mode approach has also been adopted in works [12][13]. But it either introduces much complexity or only one quadrant multiplier has been designed.

In this paper, the proposed multiplier structure is based on the up-down topology of voltage translinear loops and current conveyor blocks are included to implement the required four quadrant multiplication operation. The circuit is suitable for standard CMOS fabrication and is simple, only MOSFETS are employed.

The advantages of the proposed multiplier are:

1. It has single ended input, which does not require additional hardware and consequently more silicon area.
2. The processing and calibration steps for floating gate devices have been avoided.
3. Input impedance reduction associated with well input driven devices is avoided.
4. Sub threshold region operation use yields low power.
5. Standard CMOS technology can be used.

The Paper is organized as follows. Section II presents the background and basic idea behind the multiplier design, which is nothing but the Translinear Principle that is reviewed. Then the proposed multiplier designs given in section III dealing with the pros and cons of the design. The paper is concluded in section IV and a reference is given at the end of this paper.

II. REVIEW AND BACKGROUND

A. TRANSLINEAR PRINCIPLE:

This principle was first proposed by Barrie Gilbert in his article "Translinear circuits: a proposed Classification", *Electronics Letters*, vol. 11, no. 1, pp. 14-16, 1975.

The principle states that: **"In a closed loop containing an equal number of oppositely Connected Translinear elements, the product of the current densities in the clockwise (CW) direction is equal to the product of elements in the counter-clockwise (CCW) direction."** By the translinear elements we mean: A translinear element is a physical device whose transconductance and current are linearly related i.e. the current is exponentially dependent on the controlling voltage. Such elements include diodes, BJT and MOSFET. The principle is an elegant means to implement complex functions by small number of transistors. These circuits are having 'current mode' operation since all inputs and outputs are currents. So the voltage swing within the circuits are not considered to analyze circuit behavior. In current mode approach as the voltage swings is limited, it facilitates the design as long as I-V relation remains exponential in mainly two ways:

- 1) Voltage swing limitation means that junction capacitances do not have to be significantly charged & discharged and so translinear circuits can give comparatively high speed.

2) The problem of slew rate limiting is avoided which occurs when a limited current is available to charge a node capacitance.

The translinear principle can be categorized in two groups : Static Translinear circuits and Dynamic Translinear circuits. The Translinear principle first evolved for BJTs and then exploited for MOSFETs operating in subthreshold. This principle has also been extended for MOSFETs operating in strong inversion.

B. STATIC TRANSLINEAR PRINCIPLE

Translinear circuits are based on the exponential relation between voltage and current, characteristic for the bipolar transistor and the MOS transistor in the weak inversion region. The collector current IC of a bipolar transistor in the active region is given by:

$$I_c \approx I_s \cdot e^{V_{be}/V_t} \quad (1)$$

where all symbols have their usual meaning. A TL loop is characterized by an even number of junctions. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Fig.1.

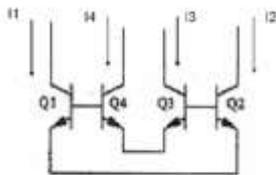


Fig 1. Four –transistor TL loop

It is assumed that the npn transistors are somehow biased at the collector currents I1 through I4. When all devices operate at the same temperature, from the translinear principle as proposed by Gilbert, the familiar representation of TL loops in terms of products of currents is:

$$I_1 \cdot I_2 = I_3 I_4 \quad (2)$$

This generic TL loop equation is the basis for a wide variety of static electronic functions, which are theoretically temperature- and process-independent.

C. DYNAMIC TRANSLINEAR PRINCIPLE

The introduction of the capacitance as a basic element of TL networks significantly extends the applicability of these circuits. The DTL principle can be illustrated with reference to the sub-circuit shown in Fig.2. Using the current mode approach, this circuit is described in terms of the collector current IC and the capacitance Icap flowing through the capacitance C. Note that the DC voltage source Vconst does not affect Icap.

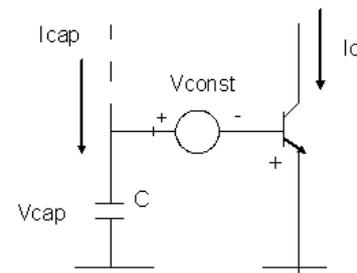


Fig 2. Showing DTL

$$I_{cap} = CVt \dot{I}_c / I_c \quad (3)$$

$$CVt \dot{I}_c = I_{cap} I_c \quad (4)$$

DTL principle: A time derivative of a current can be mapped onto a product of currents. At this point, the conventional (static) TL principle comes into play, for, the product of currents on right-hand side (RHS) of equation can be realized very elegantly by means of the STL principle. Thus, the implementation of a DE becomes equivalent to the implementation of a product of currents.

D. TRANSLINEAR THEOREM APPLIED TO MOSFET

TRANSLINEAR THEOREM APPLIED TO SUBTHRESHOLD MOS TRANSISTORS

In weak inversion the Id & Vgs relationships are given as:

$$I_d = I_o \cdot S \cdot e^{(V_{gs}-V_m)/nV_t} \cdot (1 - e^{(-V_{ds})/V_t}) \quad (5)$$

$$S = \frac{W}{L} \quad (6)$$

Io = positive constant current

For operation in saturation $V_{ds} > 3V_t \rightarrow 5V_t \approx 125mV$ where symbols have their usual meanings.

Then we have:

$$1 - e^{(-V_{ds}/V_t)} = 1 \quad (7)$$

$$I = \frac{I_d}{S} = I_o \cdot e^{(V_{gs}-V_m)/nV_t} \quad (8)$$

$$\ln \frac{I}{I_o} = \frac{V_{gs}-V_m}{nV_t} \quad (9)$$

$$V_{gs} = V_m + nV_t \cdot \ln \left(\frac{I}{I_o} \right) \quad (10)$$

For a simple translinear loop as shown in Fig3:

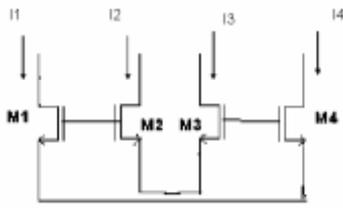


Fig3: A Translinear loop

Using KVL for each of the loops we get

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \quad (11)$$

Substituting Vgs:

$$2.V_m + 2.nV_t \cdot \ln\left(\frac{I_1 I_3}{I_0^2}\right) = 2.V_m + 2.nV_t \cdot \ln\left(\frac{I_2 I_4}{I_0^2}\right) \quad (12)$$

$$\ln\left(\frac{I_1 I_3}{I_0^2}\right) = \ln\left(\frac{I_2 I_4}{I_0^2}\right) \quad (13)$$

$$I_1 \cdot I_3 = I_2 \cdot I_4 \quad (14)$$

Therefore the theorem for sub threshold MOS is:

The product of normalized currents of translinear elements connected in CW direction is equal to the product for elements connected in anticlockwise direction in a closed loop consisting equal no. of elements connected in opposite directions.

This principle forms the basis of our multiplier design.

TRANSLINEAR PRINCIPLE APPLIED TO MOSFET IN STRONG INVERSION

For MOS transistors in saturated strong inversion is linearly related to the increase

in gate-source voltage above the threshold as under:

$$I_d = k \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 \quad (15)$$

$$\text{Transconductance: } \frac{\partial I_d}{\partial V_{gs}} = K \cdot \frac{W}{L} \cdot (V_{gs} - V_t) \quad (16)$$

Considering a loop in clockwise and anticlockwise directions of MOS transistors as shown in Fig 4 & satisfying conditions:

- *All transistors operate in strong inversion (i.e $V_{gs} > V_t$)
- *All transistors are in saturation (thus $|V_{ds}| > |V_{gs} - V_t|$)
- *The number of CW NMOS devices is equal to the number of ACW NMOS devices.
- *The number of CW PMOS devices is equal to the number of ACW PMOS devices.

There are **j** NMOS transistors and **k** PMOS transistors around the loop. Using KVL around the loop:

$$\sum_{CW_j} V_{gsj} + \sum_{CW_k} V_{sgk} = \sum_{ACW_j} V_{gsj} + \sum_{ACW_k} V_{sgk} \quad (17)$$

$$\sum_{CW_{j,k}} \left(V_{mj} + V_{tpk} + \sqrt{\frac{I_{dj}}{Kn(W/L)_j}} + \sqrt{\frac{I_{dk}}{Kn(W/L)_k}} \right) =$$

$$\sum_{ACW_{j,k}} \left(V_{mj} + V_{tpk} + \sqrt{\frac{I_{dj}}{Kn(W/L)_j}} + \sqrt{\frac{I_{dk}}{Kn(W/L)_k}} \right)$$

(18)

Canceling threshold voltage terms on both side of the equation:

$$\sum_{CW_{j,k}} \left(\sqrt{\frac{I_{dj}}{Kn(W/L)_j}} + \sqrt{\frac{I_{dk}}{Kn(W/L)_k}} \right) =$$

$$\sum_{ACW_{j,k}} \left(\sqrt{\frac{I_{dj}}{Kn(W/L)_j}} + \sqrt{\frac{I_{dk}}{Kn(W/L)_k}} \right)$$

(19)

The above equation is a statement of MOS translinear principle in strong inversion.

COMPARISON OF MOS TRANSLINEAR PRINCIPLE IN STRONG INVERSION & IN SUBTHRESHOLD

- 1) The MOS translinear principle in strong inversion is a summation of roots relation, which makes circuit synthesis more complicated. On the other hand, the Subthreshold version is a product relation and so naturally useful to implementation of functions involving multiplication and division.
- 2) MOS in subthreshold follow the exponential law over a wide current range while the range of MOS in strong inversion conform to an ideal square law is much limited.

III. PROPOSED MULTIPLIER DESIGN

A. OPERATION PRINCIPLE:

The proposed four quadrant analog multiplier designed is as shown in Fig.4. The operation

of the multiplier is based on the MOS translinear principle in weak inversion. The basic

Translinear network used for this purpose is as shown in Fig 4.

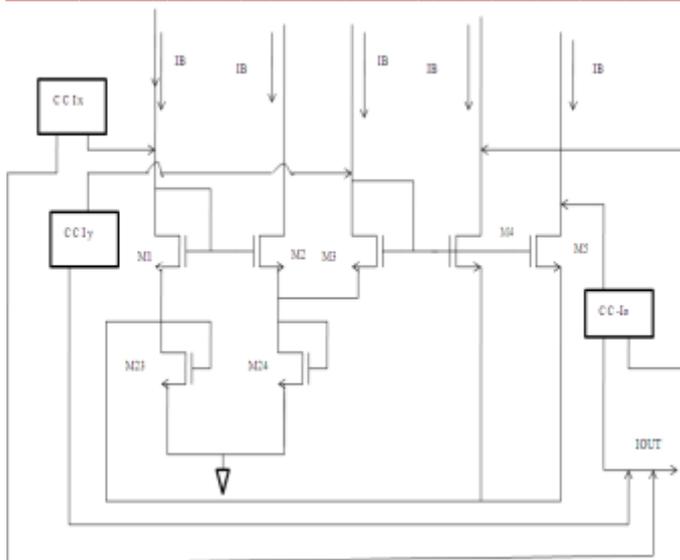


Fig 4. The circuit Diagram of the basic Translinear loop showing multiplication

For our circuit we have used:

I_B = Bias Current;

I_1 =Current through M1;

I_2 =Drain current of M2;

I_3 = Drain current of M3;

I_4 = Drain current of M4;

Inputs- I_x & I_y

$$I_1 = I_B + I_x \quad (20)$$

$$I_2 = I_B \quad (21)$$

$$I_3 = I_B + I_y \quad (22)$$

$$I_4 = I_B + I_o \quad (23)$$

where I_o is the output current taken from drain of M4 of the multiplier block.Using the Translinear principle for MOSFET in subthreshold:

$$I_1 \cdot I_3 = I_2 \cdot I_4 \quad (24)$$

$$(I_B + I_x)(I_B + I_y) = I_B \cdot (I_B + I_o) \quad (25)$$

$$I_o = (I_x + I_y) + \frac{I_x \cdot I_y}{I_B} \quad (26)$$

I_o from transistor M5 is fed to the current conveyor block CC-Io which produces two outputs, one positive output I_{o+} & a negative current I_{o-} .From I_{o-} the current I_x & I_y are fed back to the inputs the inputs through a feedback path realized by the currentconveyors CCIx & CCIy. Therefore, we get a multiplied version of the inputs scaled by a factor $1/I_B$.

The CURRENT CONVEYORS which are used for this purpose are realized by the circuits as shown in Fig 5 & Fig 6 .

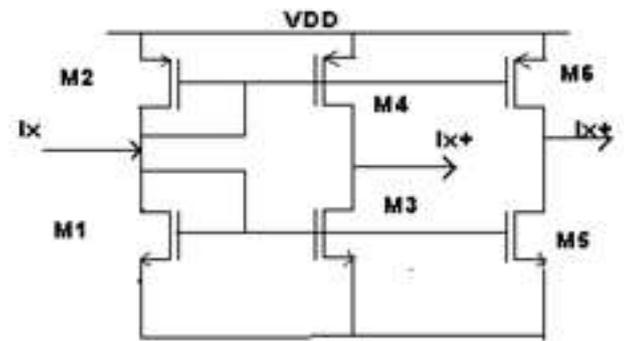


Fig 5: CCIx

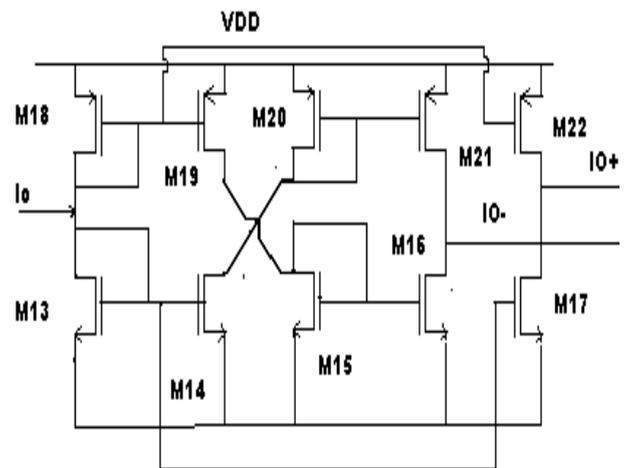


Fig6: CC Iy

The current in fig 5 produces the exact replicas of the input currents. But the current conveyor in fig 6 produces the exact but two outputs equal in magnitude as that of inputs but that from node drain of M16 as shown in the fig is of opposite polarity as that of input.

Effect Of Bias Voltage :

The bias voltage produces the bias current which plays an important role in our design.

Adjusting the bias current is a crucial point. The various limiting factors can be summedup below:

1. The bias voltage should be such that the transistors operate in subthreshold region otherwise the transconductance will not be linear with current supplied and for the designed circuit Translinear Principle will not be applicable. Hence the circuit will loose reliability. Also power dissipation will be more prominent.
- 2.The Four Quadrant multiplication requires that Bias Current should be as much large as possible so that it supports the negative phase of the current inputs. Therefore to keep the range of inputs large we need to keep the bias voltage/current high.

3. Increasing bias current decreases my ultimate output current I_{out} which is scaled by factor $1/I_B$. Therefore we need a good tradeoff between input range and magnitude of the output. This can be achieved by minute adjustment of bias voltage through perfect verification and a number of iterations.

B. CIRCUIT REALIZATION

The full circuit designed for the four quadrant multiplication purpose is as shown in fig 7 .The exact multiplication operation is obtained by the use of two types of current conveyors in the circuit. In the circuit designed, transistors M1 –M6 and M7-M12 acts as the current conveyor that produces two mirror image of their respective input currents. I_x and I_y are the two input currents. The multiplication operation is obtained by the transistors M26-M37. The set up is simply a up-down topology of the translinear loop of MOS devices arranged equally in number in clockwise and anticlockwise direction to obtain the relation. In the full circuit shown in Fig9 M25-M34 represents the basic translinear loop performing multiplication, M1-M6 & M7-M12 constitutes current conveyors CCI_x & CCI_y respectively. From M13-M23 is the CC-I_o block. The ultimate output is taken from drain of M16 with I_x & I_y fed back to the circuit.

C. SIMULATION

As the first step to check the circuit performance, a MOS of .18um technology is simulated using Win SPICE in subthreshold region to plot gm/Id vs V_{gs} curve. The region of operation is the range of V_{gs} for input where transfer efficiency or the gm/Id curve is found constant (flat) with V_{gs}.

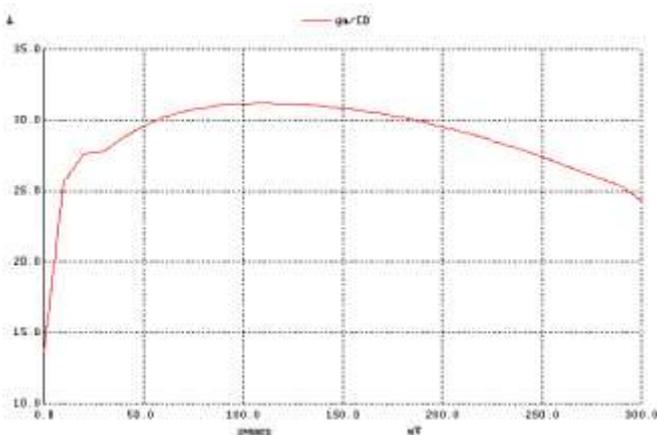


Fig8: MOS simulation for subthreshold region

IV. CONCLUSION

Mathematically we prove that the four quadrant multiplication is performed by the circuit. Simulation and layout of the proposed multiplier will be carried out in our future work.

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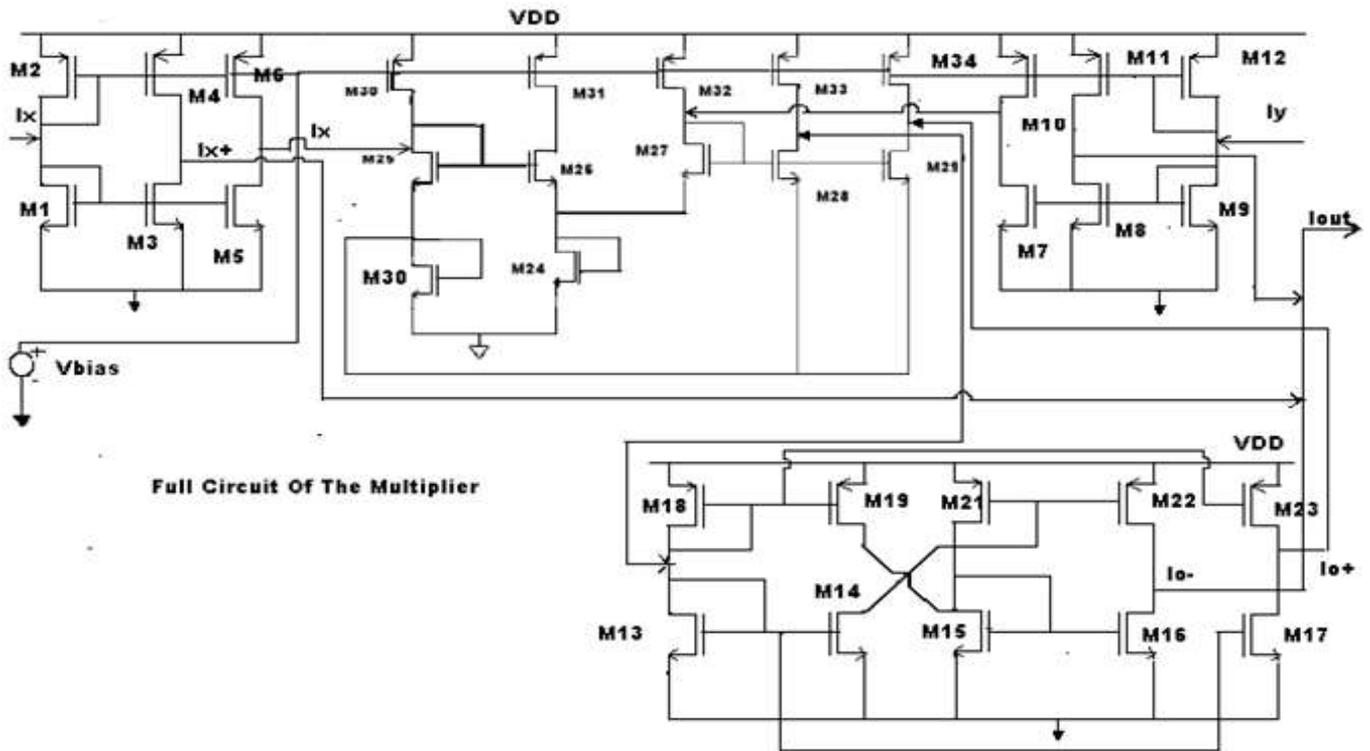


Fig 7: Full Circuit Of Multiplier