

Polar Code: An Advanced Encoding And Decoding Architecture For Next Generation 5G Applications

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Abstract—Polar Codes become a new channel coding, which will be common to apply for next-generation wireless communication systems. Polar codes, introduced by Arikan, achieves the capacity of symmetric channels with “low encoding and decoding complexity” for a large class of underlying channels. Recently, polar code has become the most favorable error correcting code in the viewpoint of information theory due to its property of channel achieving capacity. Polar code achieves the capacity of the class of symmetric binary memory less channels. In this paper review of polar code, an advanced encoding and decoding architecture for next generation applications.

Keywords- Polar, 5G, Encoding, Decoding, Channel.

I. INTRODUCTION

True In information theory, a polar code is a linear block error correcting code. The code construction is based on a multiple recursive concatenation of a short kernel code which transforms the physical channel into virtual outer channels. When the number of recursions becomes large, the virtual channels tend to either have high reliability or low reliability (in other words, they polarize), and the data bits are allocated to the most reliable channels. Polar codes were described by Erdal Arikan in 2009. There is work suggesting this is equivalent to an earlier optimised code for bitwise multistage decoding, a code originally described by Norbert Stolte. It is the first code with an explicit construction to provably achieve the channel capacity for symmetric binary-input, discrete, memoryless channels (B-DMC) with polynomial dependence on the gap to capacity. Notably, polar codes have modest encoding and decoding complexity, which renders them attractive for many applications. Moreover, the encoding and decoding energy complexity of generalized polar codes can reach the fundamental lower bounds for energy consumption of two dimensional circuitry.

There are many aspects that polar codes should investigate further before considering for industry applications. Especially, the original design of the polar codes achieves capacity when block sizes are asymptotically large with successive cancellation decoder. However, in block sizes that industry applications are operating, the performance of the successive cancellation is poor compared to the well-defined and implemented coding schemes such as LDPC and Turbo. Polar performance can be improved with successive cancellation list decoding, but, their usability in real applications still questionable due to very poor implementation efficiencies.

Although the fully parallel polar code based encoder architecture processes the bits in a fully parallel fashion but suffers with huge hardware complexity with increasing code length. As fully parallel polar code based architecture will cause logic complexity problem, while partial parallel polar code based architecture is limited by memory units of high-throughput applications.

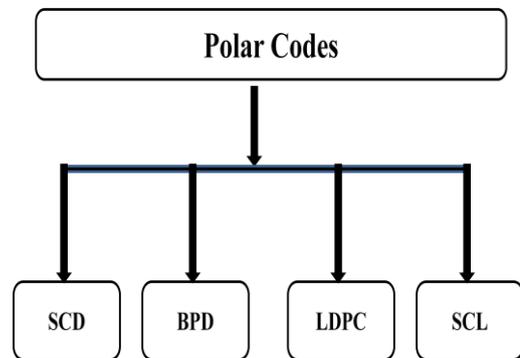


Figure 1: Types of polar code

Owing to their capacity-achieving performance and low encoding and decoding complexity, polar codes have drawn much research interests recently. Successive cancellation decoding (SCD) and belief propagation decoding (BPD) are two common approaches for decoding polar codes. SCD is sequential in nature while BPD can run in parallel. Thus BPD is more attractive for low latency applications. However BPD has some performance degradation at higher SNR when compared with SCD. Concatenating LDPC with Polar codes is one popular approach to enhance the performance of BPD, where a short LDPC code is used as an outer code and Polar code is used as an inner code.

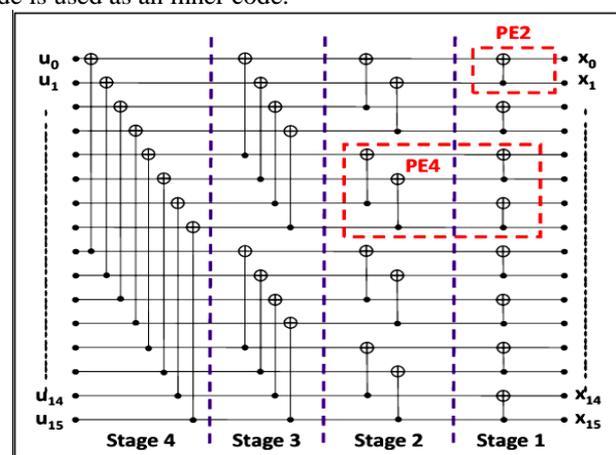


Figure 2: Operation of polar code[7]

In figure 2, showing operational steps of polar code. As it is known In information theory, a polar code is a linear block error correcting code developed by Erdal Arıkan. It is the first code with an explicit construction to provably achieve the channel capacity for symmetric binary-input, discrete, memoryless channels (B-DMC) with polynomial dependence on the gap to capacity. Notably, polar codes have encoding and decoding complexity, which makes them practical for next generation applications. The complete operation performed in 4 stages.

Operation- radix-2 based Polar encoder design, as depicted in Fig. 2. In dealing with a 16-point case, the encoder architecture is composed of several storage elements and radix-2 processing engines. By applying regular and scalable characteristics, it can be easily divided into 4 stages. The first stage consists of one radix-2 processing engine (PE2) and onebit FIFO (First-In First-Out). The radix-2 processing engine is employed for executing the PE2 operation. In addition to one XOR gate in the PE2, there also exist 2 MUXes and simple control circuits. As for the other stages, the only difference is the bit length of FIFO. In the n-th stage, FIFO needs $2n-1$ bits for the basic data storage. In the similar manner, the radix-4 based Polar encoder design and compared with the radix-2 encoder configuration, it only requires 2 stages, which each stage consists of 3 k-bit of FIFOs and one radix-4 processing engine (PE4) for the same 16-point case. The radix-4 processing engine is responsible for executing the PE4 operation in Fig. 2. Also, one PE4 needs 4 XOR gates, the corresponding MUXes, and needed control circuits. Due to the regular extension, the proposed radix-2 and radix-4 encoder designs can be applied for any power of 2 and 4 points, respectively. Most important of all, the similar design methodology is generalized to the other types of radix-k, where $k = 8, 16, 32, 64$ and so on.

II. LITERATURE SURVEY

P. Chen et al., [1] This work presents a kind of concatenated polar codes called hash-polar codes with flexible outer code lengths, in which a hash function-based encoder is used as an outer encoder. A partial hash-polar code is also proposed to enhance the error-correcting performance at high signal-to-noise ratios. Since polar codes have been recommended by 3GPP as the channel coding scheme for the 5G enhanced mobile broadband control channel, the design of hash-polar codes for 5G is considered, where both good error-correcting performance and low false alarm rate (FAR) are required. The simulation results show that, under the 5G FAR requirement, the proposed hash-polar codes have similar frame error rate performance to cyclic redundancy check (CRC)-polar codes and perform better than parity check polar codes. In order to support early termination (ET) for 5G coding, we then propose segmented hash-polar codes, which exhibit the advantages of the ET gain compared with both CRC-polar codes and distributed CRC-polar codes.

S. Shao et al., [2] Channel coding may be viewed as the best-informed and most potent component of cellular communication systems, which is used for correcting the transmission errors inflicted by noise, interference and fading.

The powerful turbo code was selected to provide channel coding for Mobile Broad Band (MBB) data in the 3G UMTS and 4G LTE cellular systems. However, the 3GPP standardization group has recently debated whether it should be replaced by Low Density Parity Check (LDPC) or polar codes in New Radio (NR), ultimately reaching the decision to adopt the code family for enhanced Mobile Broad Band (eMBB) data and polar codes for eMBB control. This work summarises the factors that influenced this debate, with a particular focus on the Application Specific Integrated Circuit (ASIC) implementation of the decoders of these three codes. We show that the overall implementation complexity of turbo, LDPC and polar decoders depends on numerous other factors beyond their computational complexity. More specifically, we compare the throughput, error correction capability, flexibility, area efficiency and energy efficiency of ASIC implementations drawn from 110 papers and use the results for characterising the advantages and disadvantages of these three codes as well as for avoiding pitfalls and for providing design guidelines.

H. Mu et al.,[3] Polar coded sparse code multiple access (SCMA) system is conceived in this paper. A simple but new iterative multiuser detection framework is proposed, which consists of a message passing algorithm (MPA) based multiuser detector and a soft-input soft-output (SISO) successive cancellation (SC) polar decoder. In particular, the SISO polar decoding process is realized by a specifically designed soft re-encoder, which is concatenated to the original SC decoder. This soft re-encoder is capable of reconstructing the soft information of the entire polar codeword based on previously detected log-likelihood ratios (LLRs) of information bits. Benefiting from the soft re-encoding algorithm, the resultant iterative detection strategy is able to obtain a salient coding gain. Our simulation results demonstrate that significant improvement in error performance is achieved by the proposed polar-coded SCMA in additive white Gaussian noise (AWGN) channels, where the performance of the conventional SISO belief propagation (BP) polar decoder aided SCMA, the turbo coded SCMA and the low-density parity-check (LDPC) coded SCMA are employed as benchmarks.

R. Shrestha et al., [4] This brief presents an algorithm for the processing element (PE) of polar decoder based on 2's complement representation of logarithmic likelihood ratios. It simplifies computation and alleviates critical path delay of PE. In addition, we propose a low complexity algorithm and p-node architecture for 2-bits successive-cancellation (SC) polar-decoding scheme. Furthermore, overall SC polar decoder-architecture has been design by incorporating suggested PE architectures as well as p-nodes to support code-length and code-rate (r) of 1024 bits and 1/2 respectively. We have synthesized and post-layout simulated our design in UMC 180 nm-CMOS process.

P. Chen et al., [5] With the development of high-speed trains (HST), efficient and reliable communication services in high mobility scenarios have become an urgent demand. As one of the strong candidates in 5G wireless system, polar codes along with its optimized design should also be investigated under high mobility scenarios. In this work a scheme of hash-

concatenated polar codes is proposed to reduce the false alarm rate, which is a key performance in 5G enhanced mobile broadband control channel. Then, for data channels, hash-based cyclic redundancy check (CRC)-aided polar codes with a joint successive cancellation list decoding method is introduced to improve the error-correcting performance. Simulation results show that the hash-concatenated polar codes can achieve both the lower false alarm rate and better error-correcting performance than conventional CRC-aided polar codes in both the AWGN and high mobility channels. Furthermore, with the joint decoding approach, hash-based CRC-aided polar codes perform better than LTE turbo codes for high-order modulations in terms of the frame error rate over the HST channel.

In October 2016 Huawei announced that it had achieved 27Gbps in 5G field trial tests using the Polar codes for channel coding. The improvements have been introduced so that the channel performance has now almost closed the gap to the Shannon limit which sets the bar for the maximum rate for a given bandwidth and a given noise level.

In November 2016 3GPP agreed to adopt Polar codes for the eMBB (Enhanced Mobile Broadband) control channels for the 5G NR (New Radio) interface. At the same meeting 3GPP agreed to use LDPC for the corresponding data channel.

A. III. CRC vs POLAR CODE

For control channel, FAR is the key metric which should be satisfied. FAR depends on the list size and error detection capability of CRC and parity bits. There is enough justification in literature to verify that CRC provides very good performance compared to other error detection codes. CRC is a kind of linear block code, showing very nice error detection capability.

The FAR of the parity bits based solution can be analyzed as follows. The parity bits used for early termination and the final CRC check can be considered to be a combined code because all of them are used for error detection. For example, a simplified early termination scheme is proposed where some parity bits are generated to support early termination and these bits are generated by the checksum of the transmitted information bits. Then, the corresponding bigger generator matrix can be obtained.

An example generator matrix for 3 parity bits and 5 CRC bits generated from 12 information bits are shown below.

The total number of undetectable errors is shown in Figure 2. The results are obtained by test every possible error of information block to check if it can be detected by CRC or PC+CRC (i.e., 2K error patterns). It is the absolute error detection capability metric. As can be seen from Figure 1, the parity check based scheme experiences nearly double the undetectable errors compared to distribute CRC. So it needs more CRC/PC bits to achieve the same FAR performance. The CRC polynomial used in the PC-Polar is 0x11021, and 3 additional parity check bits are used for early termination and

these three bits are also used for final error detection. The 19bit CRC is used in distributed CRC and the polynomial is 0xAF56F. Some companies showed FAR analysis assuming noise at the decoder.

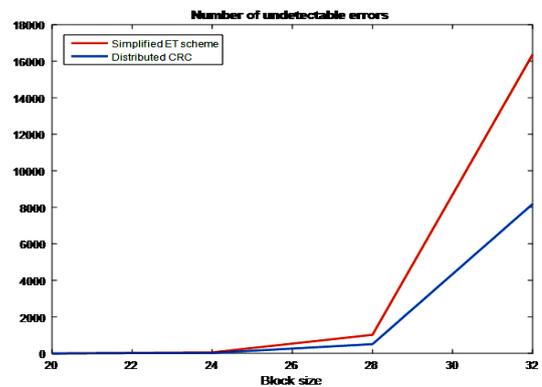


Figure 2: Number of undetectable errors[3]

The percent of ET is shown in Figure 3, which is the metric to evaluate how many errors can be early detected out of all errors. It can be seen that the distributed CRC scheme can 100% early detect the errors, and only 50% errors can be early detected by the simplified ET scheme, for multi-bit ET.

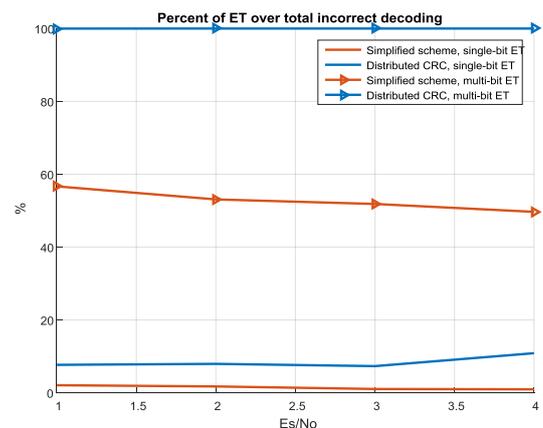


Figure 3. Percent of ET, for Polar code (64,43), where info = 24, CRC = 19.[3]

Figure 4 shows the overall saved computation by ET. It is defined by the percent of ET multiplied by the saved decoding. The saved decoding is defined as remained number of information bits to be decoded compared to the total number of information bits. It can be seen that the distributed CRC outperforms the PC based simplified ET scheme by approximately 100%.

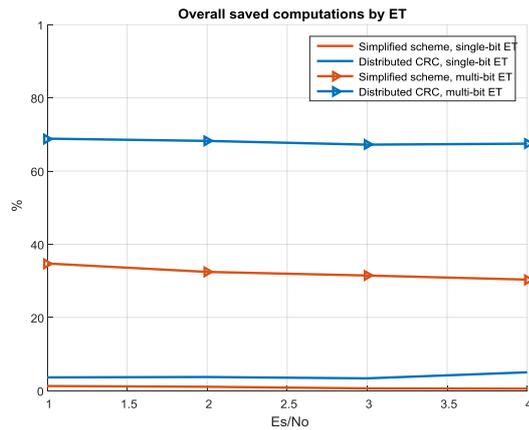


Figure 4: Overall save computation, for Polar code (64,43), where info = 24, CRC = 19

IV. CONCLUSION

In this paper, we reviewed the state of the art in polar code in encoding and decoding form. It was shown that the many decoding algorithms were developed and implemented to address various application requirements. Also compare polar code with CRC code. Many researchers propose that polar code can be used in advance wireless communication for next generation.

REFERENCE

- [1]. P. Chen, B. Bai, Z. Ren, J. Wang and S. Sun, "Hash-Polar Codes With Application to 5G," in *IEEE Access*, vol. 7, pp. 12441-12455, 2019.
- [2]. S. Shao *et al.*, "Survey of Turbo, LDPC and Polar Decoder ASIC Implementations," in *IEEE Communications Surveys & Tutorials*.
- [3]. H. Mu, Y. Tang, L. Li, Z. Ma, P. Fan and W. Xu, "Polar coded iterative multiuser detection for sparse code multiple access system," in *China Communications*, vol. 15, no. 11, pp. 51-61, Nov. 2018.
- [4]. R. Shrestha and A. Sahoo, "High-Speed and Hardware-Efficient Successive Cancellation Polar-Decoder," in *IEEE Transactions on Circuits and Systems II: Express Briefs*.
- [5]. P. Chen, M. Xu, B. Bai and J. Wang, "Design and Performance of Polar Codes for 5G Communication under High Mobility Scenarios," *2017 IEEE 85th Vehicular Technology Conference (VTC Spring)*, Sydney, NSW, 2017, pp. 1-5.
- [6]. Y. N. Li, "Robust Image Hash Function Based on Polar Harmonic Transforms and Feature Selection," *2012 Eighth International Conference on Computational Intelligence and Security*, Guangzhou, 2012, pp. 420-424.
- [7]. X. Shih, P. Huang and Y. Chen, "High-speed low-area-cost VLSI design of polar codes encoder architecture using radix-k processing engines," *2016 IEEE 5th Global Conference on Consumer Electronics*, Kyoto, 2016, pp. 1-2.
- [8]. X. Shih, P. Huang and Y. Chen, "LEGO-based VLSI design and implementation of polar codes encoder architecture with radix-2 processing engines," *2016 IEEE Asia Pacific*

- Conference on Circuits and Systems (APCCAS)*, Jeju, 2016, pp. 577-580.
- [9]. S. M. Abbas, Y. Fan, J. Chen and C. Tsui, "Concatenated LDPC-polar codes decoding through belief propagation," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.
- [10]. A. Arpure and S. Gugulothu, "FPGA implementation of polar code based encoder architecture," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0691-0695.
- [11]. B. Chen, T. Ignatenko, F. M. J. Willems, R. Maes, E. van der Sluis and G. Selimis, "A Robust SRAM-PUF Key Generation Scheme Based on Polar Codes," *GLOBECOM 2017 - 2017 IEEE Global Communications Conference*, Singapore, 2017, pp. 1-6.
- [12]. D. Chen, N. Zhang, N. Cheng, K. Zhang, Z. Qin and X. S. Shen, "Physical Layer based Message Authentication with Secure Channel Codes," in *IEEE Transactions on Dependable and Secure Computing*.