LNA for UWB transceiver using 0.18µm CMOS Technology

S. Khadar Bhasha
Assistant professor in Department of ECE
Aditya engineering College (Autonomous)
Surampalem, East Godavari, AP, India.
khadarbasha421@gmail.com

B.H.K. Bhagat Kumar
Assistant professor in Department of ECE
Aditya engineering College (Autonomous)
Surampalem, East Godavari, AP, India.
harikuamr470@gmail.com

Abstract**—** An Ultra WideBand CMOS Low Noise Amplifier (LNA) is presented. Due to really low power consumption and extremely high data rates the UWB standard is bound to be popular in the consumer market. The LNA is the outer most part of an UWB transceiver. The LNA is responsible for providing enough gain to the signal with the least distortion possible. CMOS 0.18µm TSMC technology has been chosen for the design of the LNA at the transistor level. As many as five on chip inductors are implemented for the proper gain shaping over the frequency range of 3.1GHz to 10.6GHz. A noise figure of 3.98 dB is achieved to make sure noise contribution of the amplifier is as low as possible.

Keywords*-Ultra Wideband(UWB), Low Noise Amplifier, Noise Figure.*

*****

I. INTRODUCTION

Ultra Wide-Band (UWB) technology has been designed to bring convenience and mobility of high speed wireless communication to homes and offices. It is specifically designed for short range Wireless Personal Area Networks (WPANs). UWB will play an instrumental role in freeing people from wires and enabling video transmission or other high bandwidth data transmission that is rarely possible with a conventional wireless connection. The short range UWB technology will also complement other wireless standards such as Wi-Fi and Wi-Max. It can transmit data within the radius of 10 meters from the host device. UWB technology is designed to provide a short range, very low power connection with much more bandwidth than cable. Since UWB communicates with short range pulses, it can be used for tracking various objects. It has been shown that a UWB device can successfully transmit data at a rate of 110 Mbps at a distance of 10 meters [1]. This bandwidth is 100 times faster than Bluetooth and twice as fast as Wi-Fi. This bandwidth is large enough to accommodate three concurrent video streams over a single connection. Designers are promising UWB products that have speeds of up to 1 Gbps [2].

A basic block diagram of the UWB transceiver, including a transmitter and a receiver, is shown in Figure 1. The baseband Digital Signal Processing (DSP) unit controls the messaging and signaling of information. The DSP unit also synchronizes the system clock. The main function of the receiver is to amplify the signal without amplifying the noise. The principal role of the transmitter is to boost up the signal using some line drivers in order to send high energy signals.

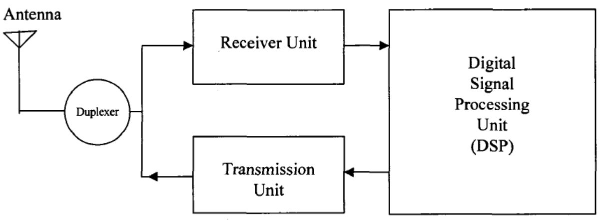

Figure1. Block diagram of UWB transceiver

The block diagram of a UWB receiver is shown in Figure 2. The receiver features a Low Noise Amplifier (LNA) followed by a mixer (demodulator). The mixer removes the carrier from the received radio frequency signal. Usually there is an automatic gain control block between the mixer and the Analog to Digital Converter (ADC). The purpose of this block is to balance the amplification or attenuation of the received signal in a way that it utilizes the maximum range of the ADC. The analog to digital converter then converts the analog signals to digital data which is fed to the DSP to process the transmitted data. The signal is then fed to the DSP block for baseband processing.

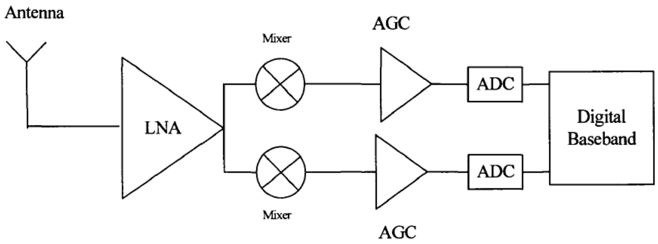

Figure 2. Block diagram of UWB receiver

In this context it is clear that an ultra wideband LNA should pass all the frequencies between 3.1 to 10.6 GHz. Such an amplifier must feature wideband input matching to a 50 Ω antenna for noise optimization and filtering of the out-of-band interferers. Moreover, it must show flat gain with good linearity and minimum possible noise figure over the entire bandwidth.

The LNA is an instrumental component of a UWB receiver. The LNA's noise figure has a major impact in deciding the system's overall noise figure, therefore this thesis deals with various aspects of the LNA design for a UWB device.

II. SYSTEM DESCRIPTION

Design Specifications

The field of UWB technology is of high demand these days because of the huge desire for data rates and speed which it can provide. According to high UWB requirements, the interest in designing appropriate WB devices has increased. Especially, the receiver part has come in the centre of attention and many UWB front-end have been designed in the past few years. LNA is considered the backbone of the UWB receiver. The design specifications includes frequency band of operation, desired noise figure (NF), selection of topology, technology used and gain requirements. It is these specifications which determine the LNA design and hence choosing specifications is a very crucial step in RF receiver design.

III. LNA Design For UWB Transceiver

The design and implementation steps followed in the design of inductive source degeneration LNA are mentioned below. This topology is simulated using Quite Universal Circuit Simulator (QUCS) studio.

A. Inductive source degeneration LNA topology

The proposed solution expands the basic inductively degenerated common source amplifier by inserting an input multi section reactive network, so that the overall reactance can be resonated over a wider bandwidth. This input matching network is shown in the Figure 3 by a dotted square. An inductor (Lg) is placed in series with a capacitor (Cp) to add flexibility to the design. Different values of Lg and Cp would give different matching conditions. The cascade connection of M1 and M2 improves the input output reverse isolation and the frequency response of the amplifiers. The source follower stage (M3 and M4) is used for measurement purposes.

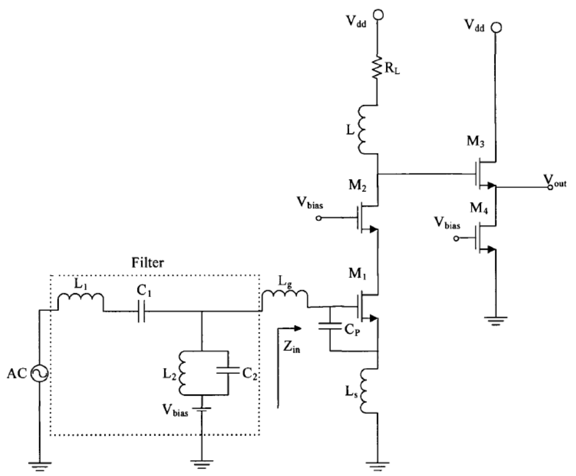

Figure 3. Proposed inductive source degeneration LNA topology

As seen in the circuit, the input impedance of transistor M1 is a series RLC circuit given by:

$$Z_{in}(s) = \frac{1}{C_{gs} + C_p} + s.(L_s + L_g) + \omega_T . L_s \qquad Eq.1$$

where ω_T is given by:

$$\omega_T = \frac{g_m}{C_{gs} + C_p} \qquad Eq.2$$

In order to get good input impedance matching, the real part of Z_{jn} should match with source resistance in the circuit. In the passband of the filter, the power loss is zero with a ripple ρ. There is a nonzero power loss for the frequencies not included in the passband, and that is how band rejection works. The choice of reactive elements in the filter determines the bandwidth of the in-band ripple. The input reflection coefficient *Γ* is related to ρ by:

$$|\Gamma|^2 = 1 - \frac{1}{\rho}$$

The input reflection coefficient (Γ) is a good measure of the input matching. The lower the reflection coefficient the better input matching is achieved.

The input network impedance is equal to $R_s/W(s)$ where W(s) is the Chebyshev filter transfer function given by:

$$W(s) = \omega . L_1 + \frac{1}{\omega . C_1} + \omega . L_2$$

Note that W(s) is approximately unity in the in-band and tends to zero at out-of-band. The impedance looking into the amplifier is therefore equal to R_s in the in-band, and it is very high out-of-band. At high frequency the MOS transistor acts as a current amplifier because of the channel length modulation effect. The current gain is given by P(s) = $g_m/(sQ)$. The current flowing into Mi is $[V_{in} W(s)]/R_s$ and therefore the output current is $V_{in}W(s)/(sC_tR_s)$.

The load of the LNA is a shunt peaking transistor used as a resistor. The overall gain is:

$$\frac{V_{out}}{V_{in}} = \frac{G_m . W(s) \left[R_L \left(1 + \frac{s.L}{R_L}\right)\right]}{s.C_1 . R_s[1 + s.R_L . C_{out} + s.L.C_{out}]} \qquad Eq.3$$

where, R_L is the load resistance, L is the load inductance, and C_{out} is the total capacitance between the drain of M2 and ground. That means $C_{out} = C_{db}2 + C_{gd}3$, where $C_{db}2$ is the drain and bulk capacitance and $C_{gd}3$ is the gate and drain capacitance of transistor M3. Equation 3 shows that the current gain roll is compensated by L because it is directly connected to the drain of transistor M2. Moreover, it shows that C_{out} introduces a spurious resonance with L, which must be kept out of the band.

The noise figure is defined by amount of noise contributed by the circuit. For any LNA design it is ideal to have our noise figure as low as possible. As mentioned in the abstract, the targeted noise figure for this topology was 4 dB and the design gives us a noise figure of less than 4 dB for the entire UWB frequency band which is 3.1 GHz to 10.6 GHz. The noise figure was simulated using the QUCS studio simulator.

The challenge posed by the measurement of conventional two port parameters motivates the scattering, or S–parameter characterization of linear two port systems. In contrast to the impedance, admittance, and hybrid parameters, the scattering parameters of linear electrical or electronic networks are measured without need of short circuiting or open circuiting input and output ports.

Instead, these ports are terminated in fixed and known characteristic impedances that are often similar or even identical to the terminating impedances incorporated in the design. Accordingly, the dynamic performance and operational integrity of a network under test are not compromised by test fixturing adopted for its scattering parameter characterization. An S-parameter simulation schematic is used to achieve the plot of S11, S21 and S22 in terms of decibels.

IV. Design Implementation and Results

Inductive source degeneration LNA circuit is simulated. The scattering parameter analysis is done and S-parameters, noise figure were obtained.

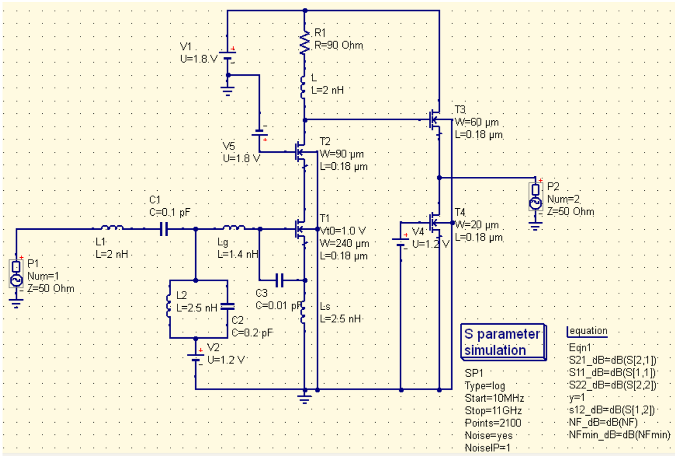

Figure 4. Experimental schematic of inductive source degeneration LNA

Simulation results

The simulation results of an inductive source degeneration LNA circuit are as shown in the Figure5. It contains the S11, S21, S22 and Noise Figure curves with respect to frequency.

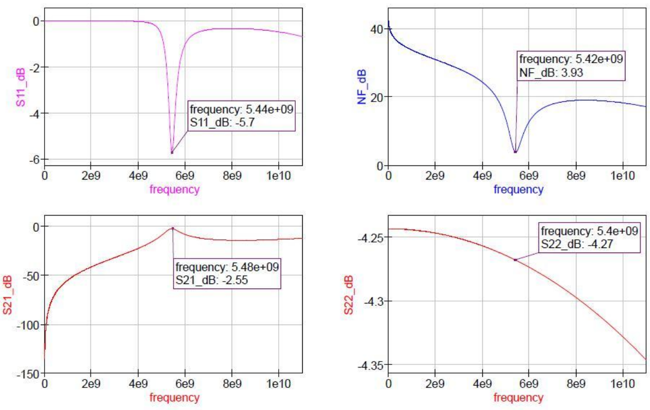

Figure 5. Simulation results: S11_dB, NF_dB, S21_dB and S22_dB

TABLE I. Simulation Results

Parameters measured at 5.4 GHz frequency			
S11 in dB	***S21 in dB***	***S22 in dB***	***Noise Figure in dB***
-5.7	-2.55	-4.27	3.98

V. Conclusion

The primary objective of the paper was to design a Low Noise Amplifier (LNA) that could be used for UWB applications. It was intended to have the LNA be capable of providing enough gain within the frequency range 3 to 10 GHz with minimal noise figure.

The TSMC 0.18µm CMOS technology was used for the project. The target noise figure was less than 4 dB and simulations show that the proposed architecture has succeeded in achieving that. The noise figure is 3.98 dB for at 5.4 GHz frequency.

References

[1] Technology demonstration of Freescale Semiconductor Inc., Tempe, Arizona.

[2] UWB parameters for EMC coexistence with legacy systems, DAPRA, Jun 2003.

[3] B. Razavi, *RFMicroelectronics.* Upper Saddle River, NJ: Prentice Hall, 1998.

[4] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits.* New York: Cambridge University Press, 2000.

[5] Devendra K. Misra, *Radio frequency and microwave communication circuits.* Wiley, 2001.

[6] Andrea Bevilacqua and Ali M. Niknejad, "An Ultrawideband CMOS Low-Noise Amplifier for 3.1 - 10.6 GHz Wireless Receivers," IEEE J, Solid-State Circuits, Vol.39, pp. 2259-2268, Dec. 2004.

[7] Yi-Jing Lin, Shawn S. H. Hsu, Member, IEEE, Jun-De Jin, and C. Y. Chan, "A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier With Current-Reused Technique"*IEEE Microwave And Wireless Components Letters*, Vol. 17, No. 3, March 2007.

[8] Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon- Tae Kim, and Sang-Gug Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 3–5-GHz UWB System ",*IEEE Journal Of Solid-State Circuits*, Vol. 40, No. 2, February2005.

[9] Qiang Li, Member, IEEE, and Yue Ping Zhang,"A 1.5-V 2– 9.6-GHz Inductorless Low-Noise Amplifier in 0.13-m CMOS",*IEEE Transactions On Microwave Theory And Techniques*, Vol. 55, No. 10, October 2007.

[10] Mahdi Parvizi, Student Member, IEEE, Karim Allidina, Student Member, IEEE, and Mourad N. El-Gamal, Member, IEEE,"A Sub-mW, Ultra-Low-Voltage, Wideband Low- Noise amplifiers Design Technique",*IEEE Transactions On Very Large Scale Integration (Vlsi) Systems*, Vol. 23, NO. 6, June 2015.

[11] Ke-Hou Chn, Jian-Haeo Lu, Bo-Jin Chen, and Shen-Iuan Liu,"An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18nm CMOS", *IEEE Transactions On Circuits And Systems—Ii: Express Briefs*, Vol. 54, No. 3, March 2007.

[12] Y.-H. Yu, Y.-J. Emery Chen, and D. Heo, "A 0.6-V low power UWB CMOS LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 229–231, Mar. 2007.

[13] Y. Wang, A. -Ho, K. -Iniewski and V. -Gaudet, "Inductive ESD protection for narrow band and ultra-wideband CMOS low noise ampli□ers", *Proc. IEEE Int. Symp. Circuits Syst.*,May 27–30, 2007, pp. 3920–3923.

[14] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low power low-voltage applications", *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.

[15] J.-F. Chang and Y.-S. Lin, "0.99 mW 3–10 GHz common gate CMOS UWB LNA using T-match input network and self-body-bias technique" ,*Electron. Lett.*, vol. 47, no. 11, pp. 658–659, May 2011.

ISSN: 2321-8169
17 - 20

[16] Louis E. Frenzel(Sep 14, 2006)Electronic Design The ElusiveSoftwareDefinedRadio,Available: http://electronicdesign.com/communications/ elusive-software-defined-radio
[17] Behzad Razavi, "RF Microelectronics",2nd Edition, Behzad Razavi, May 19, 2006
[18] Jongsoo Lee, Member, IEEE, And John D. Cressler, Fellow, IEEE, "Analysis And Design Of An Ultra- Wideband Low-Noise Amplifier Using Resistive Feedback In Sige HBT Technology", *IEEE Transactions On Microwave Theory And Techniques*, VOL. 54, NO. 3,MARCH 2006
[19] R. J. Fontana, E. A. Richley et.al, "An Ultra Wideband Radar for Micro Air Vehicle Applications", Reprinted from 2002 *IEEE Conference on Ultra Wideband Systems and Technologies*, May 2002.
[20] Johor Bahru, Wireless Commun. Centre, Univ. Teknol. Malaysia, "Ultra wideband technology and its applications "*IEEE Wireless and Optical Communications Networks*,. WOCN '08. 5th IFIP International Conference on 2008
[21] Allstot, David J., Xiaoyong Li, and Sudip Shekhar. "Design considerations for CMOS low-noise amplifiers." *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE.* IEEE, 2004.