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Design of VGA and Implementing On FPGA

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***Abstract*—**This research paper presents how to design a VGA controller using a Field Programmable Gate Array (FPGA). Video Graphics Array (VGA) is widely used as a standard display interface. Detailed information of this research paper is on the architecture, hardware and software development. This controller is implemented and developed using Verilog HDL based in an IEEE standards, to ensure the ease to use with any user. The system has the potential to display any image. The FPGA used in this implementation is Nexys 4 DDR FPGA board and the software used is Xilinx Vivado.

Keywords*-Nexys 4 DDR, FPGA, VGA Controller, Verilog HDL, Xilinx Vivado.*

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I. INTRODUCTION

Research and development for a specific task are increasing day by day nowadays. VGA is used in many applications such as embedded systems, ATM machines, video conferencing, and video surveillance systems. Video Graphics Array controller is used as a logic circuit which control the VGA interface. FPGA can be used to implement the logic of VGA interface which results in less cost and more flexibility. Flexibility is an important quality of today's industrial produced machines so that it can deliver all unplanned demands. FPGA is small sized equipment and has very low power consumption which satisfies all the need of today's requirement.

II. FIELD PROGRAMMABLE GATE ARRAY(FPGA)

FPGA (Field Programmable Gate Array) is an integrated circuit designed to be configured by the designers after manufacturing- hence field programmable [1]. FPGAs contain an array of programmable logic blocks, and a progressive programmable logic interconnects which allow the blocks to function together, like many logic gates that are connected in different ways and configurations. Logic blocks can be programmed to performed simple logic gates like NAND and NOR or to perform a complex combinational functions such as an ALU. Usually FPGA are used to make a prototype building because changes are easy to make on a FPGA board. This saves a lot of money as hardware is not thrown away after a single change. Moreover, FPGA can be used to perform different functionality [2].

The general internal structure of an FPGA is shown in Fig. 1. It contains mainly: logic blocks, Input/output blocks for interfacing and interconnection switches.

Here in this paper we are going to use Nexys 4 DDR FPGA board made by Xilinx.

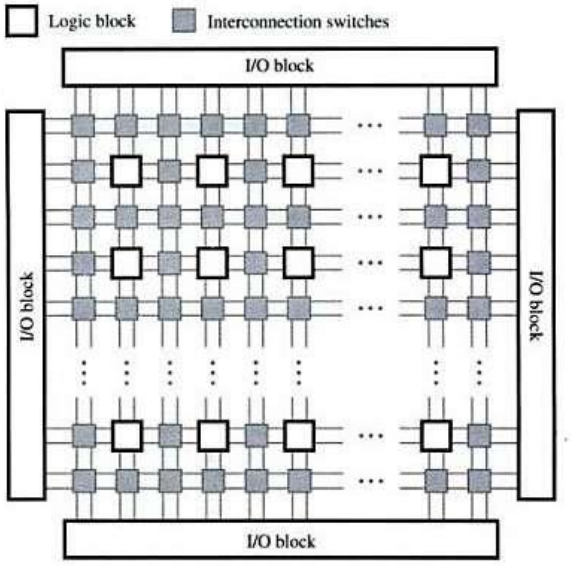

Fig. 1 The general structure of an FPGA [8]

III. VIDEO GRAPHICS ARRAY(VGA)

VGA (Video Graphics Array) is standard for video display. It has a simple method to connect a system with any display hardware such as monitor for showing images, videos, and any kind of data. The monitor screen for a standard VGA format contains 480 rows by 640 columns of picture element called pixel. Display of an image can be done on the screen by turning on and off set of pixels at a time. Turning on a one pixel will not make a difference, but combining many pixels will generate an image. A continuous scan occurs on entire monitor screen, turning individual pixels on and off. Even if pixels are turned on one at a time, it shows that all pixels are turned on as the monitor scans very fast. This is the reason behind flicker of old monitors having slow scan rates. The scanning process starts from the top left corner of the screen from row0, column0 and ends to the right until it reaches the last column [8]. The scan process is horizontal one row after another row. This means the scan reaches the end of row, it again starts from beginning of

the next row. When last pixel is scanned which is at the bottom right corner of the screen, it again starts scanning from the top left corner and do whole scanning process again. The entire screen must be scanned 60 times in one second so that there is less flicker on the screen. This scanning rate is known as refresh rate of screen. By research, a human eye can detect flicker for screens having less than 30Hz refresh rates. During the horizontal and vertical retraces, all pixels are turned off [7]. Refer fig2

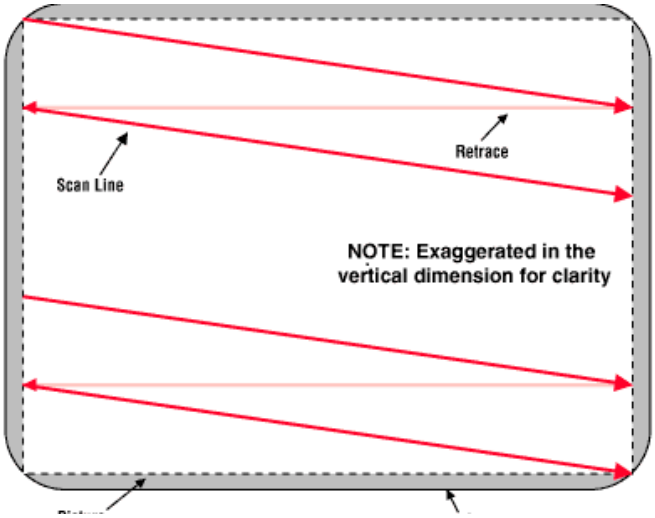

Fig 2 Scanning pattern for VGA Controller

IV. VGA CONTROLLER

Block diagram of VGA controller is shown in fig. 3 and fig.4.There are three blocks- reset, clock generator and a VGA controller. The VGA controller block is again made up of four different blocks-VGA synchronization, address generator, image data block and image index block. Input signals are reset and clock which are given to VGA controller which gives RGB (red, green, blue), horizontal synchronization, vertical synchronization and black signals as output. The reset signal is given out by reset blocks. Clock generator block reduce the input clock frequency to 25 MHz so that 640X480 resolution is maintained. At the same time, the VGA synchronization block generate timing and synchronization signals. As the horizontal synchronization signal specifies the required time to scan a row, and the vertical synchronizationsignal specifies the required time to scan the entire screen. This block also generates the "blank" signal which indicates retrace period of the display [9].

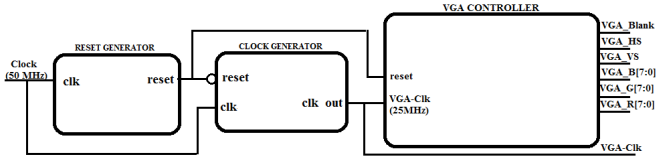

Fig 3 Proposed block diagram [8]

The addresses are created by address generator block with the outputs of VGA synchronization block and gives it to the image data block whose outputs gives inputs to the image index block. Image index block gives out red, blue and green signal. The red, blue and green data consist of 24-bits, whereas "q [23:16]", "q [15:8]" and "q [7:0]" indicate the "R_VGA", "G_VGA" and "B_VGA" respectively [8]. These three color signals control the color of a pixel at a given location on the screen. The analog voltage range vary from 0.7 volt to 1.0 volt. Varying these voltage different color intensities can be obtained. These three color signals are treated as digital signals so that each one go on and off by user [4]. Fig. 4 shows that the color signals use resistor-divider circuits that work in conjunction with the termination resistance of 75-ohm of the VGA display to create 16 different levels each on three colors.

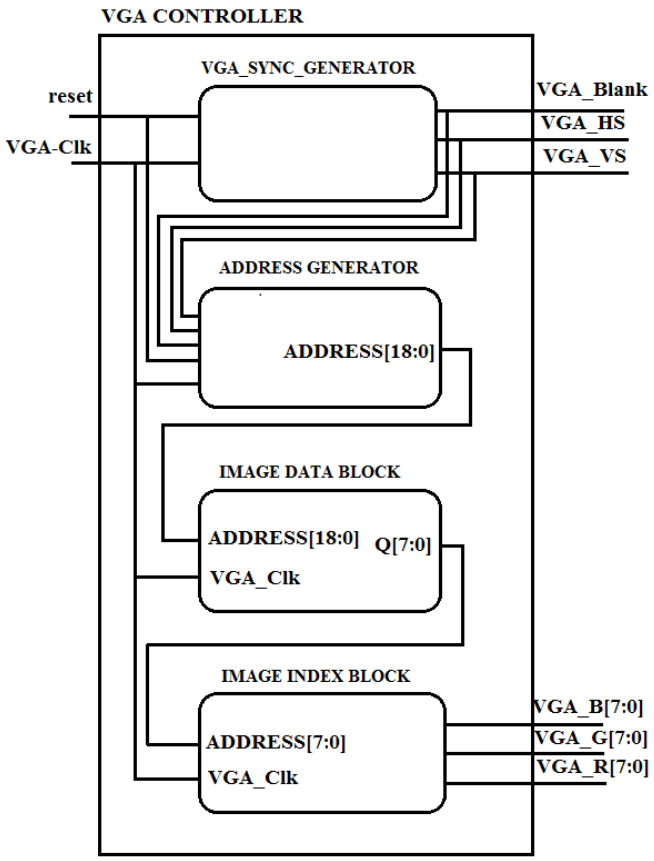

Fig.4 Internal Block diagram of VGA Controller [11]

V. TIMMING FOR VGA SIGNALS

Cathode Ray Tube (C.R.T) – based VGA display screen use modulation of amplitude of the moving electron beams which is known as cathode rays to display data on a phosphor-coated screen. Liquid Crystal Display is a type of screen which use an array of switches that can apply a voltage across a small amount of liquid crystal, this changes light permittivity through one crystal on a pixel-by-pixel basis [6]. The discussion below revolves around both CRTs and LCDs.

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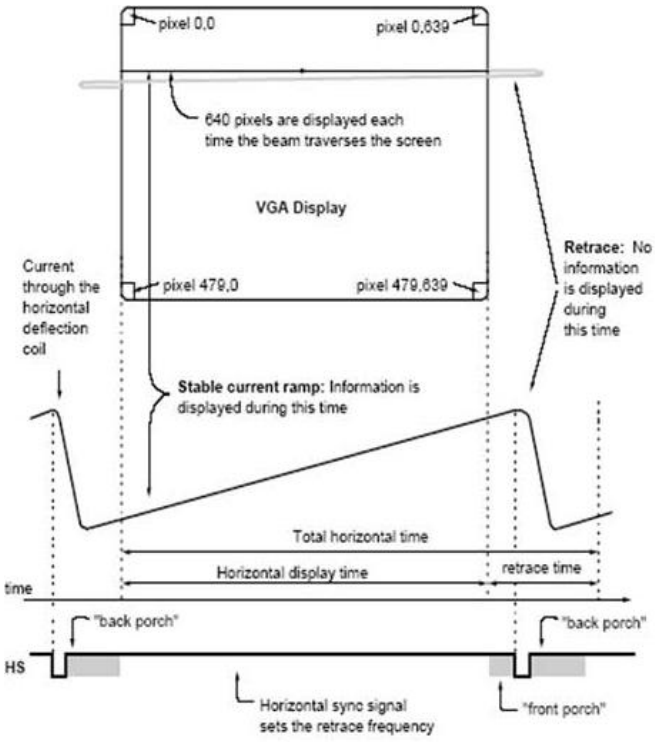

Fig. 5 CRT Display Timing Example

The VGA timing signals can be divided into two parts- Horizontal timing and Vertical timing. (640X480 resolution).

A. Horizontal Timing

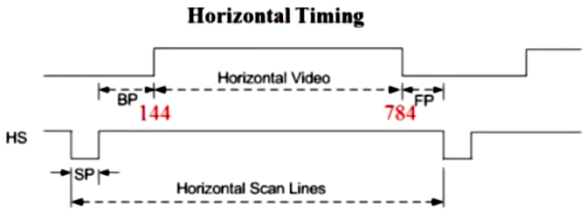

Fig. 6 Horizontal Timing Pulse

Pixel Clock = 25 MHz
Pixel time = 0.04 us

Horizontal video, HV = 640pixels x 0.04 us = 25.60us (1)
Back porch, BP = 16pixels x 0.04us = 0.64us (2)
Front porch, FP = 16 pixels x 0.04us = 0.64us (3)
Sync pulse, SP = 128pixels x 0.04us = 5.12us (4)
Horizontal scan lines (pixels) = SP+BP+FP+HV
= (128 + 16 + 16 + 640) pixels
= 800 pixels
Horizontal scan 800 x 0.04us = 32us (5)
So, scan lines per frame = 1/ (60 x 32) = 521 (6)

B. Vertical Timing

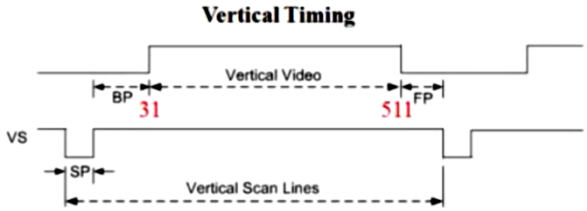

Fig. 7 Vertical Timing Pulse

Pixel Clock = 25 MHz
Horizontal scan time = 32 us
Vertical video, VP = 480pixels x 32us = 15.360ms (7)
Back Porch, BP = 29pixels X 32us = 0.928ms (8)
Front porch, FP = 10pixels x 32us = 0.320ms (9)
Sync Pulse, SP = 2pixels x 32us = 0.64ms (10)
Vertical Scan lines (pixels) = SP+BP+VV+FP
= (2+29+10+480) pixels
=512 pixels

Vertical scan time = 512pixels X 32us = 16.67ms (11)

Back Porch is defined as the delay time following the time when the horizontal timing pulse goes high and Front Porch is the delay time before the horizontal timing pulse goes low again during the retrace.

VI. FLOW CHART FOR VGA DISPLAY

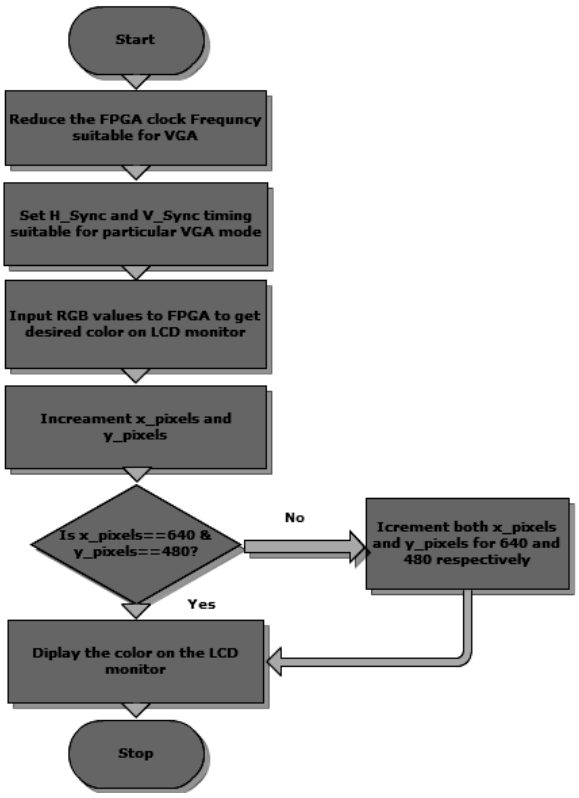

Fig. 8 Typical flow diagram [6]

Above is the flowchart which decribes the flow operation of thye VGA ccontroller IP core [8]. The steps are:

1) FPGA Clock reduction: The clock frequency of FPGA is reduced from 60 MHz to 25 Mhz so that it matches frequency of VGA.

2) Syncronisation: This step setsthe horizontal and vertical timing syncronization accoring to the target VGA mode.

3) Input to VGA: In this step user should give a input in terms of RGB (Red, Blue, Green) in order to get desired output on screen.

4) Scanning: This step increment pixels in horizontal(x) and vertical(y) diretions one location after location.

5) Checking end points: Check he condition, X= 640 && Y=480? If condition is not matched then increment both x direction pixel and y direction pixel for 640 and 480 respectively. If Condition is matched then VGA will display the colour.

6) Stop the process

VII. NEXYS 4 DDR

The NEXYS4 DDR is a ready to use digital circuit development platform designed to bring additional industry applications into the classroom environment [3]. I have used Xilinx FPGA (part number is XC7A100T-1CSG324C). I used 14 FPGA signals to create a port of VGA with 4-bits for one color and the two standard synchronization signals[2].

VIII. IMPLEMETATION

I am going Vivado suite by Xilinx. The designed VGA controller [9] is implemented on our FPGA using Vivado design suite by keeping the design constraint in mind of Xilinx. The quality of program in term of synthesis is first check by Vivado. Then by execution of program it makes a virtual circuit diagram based on the code provided. Then the software generates a bit pattern which is given and written on the hardware. It has constraint file which is FPGA specific. It specifies what connections are made to the FPGA. The design constrain file is given in fig. 9.

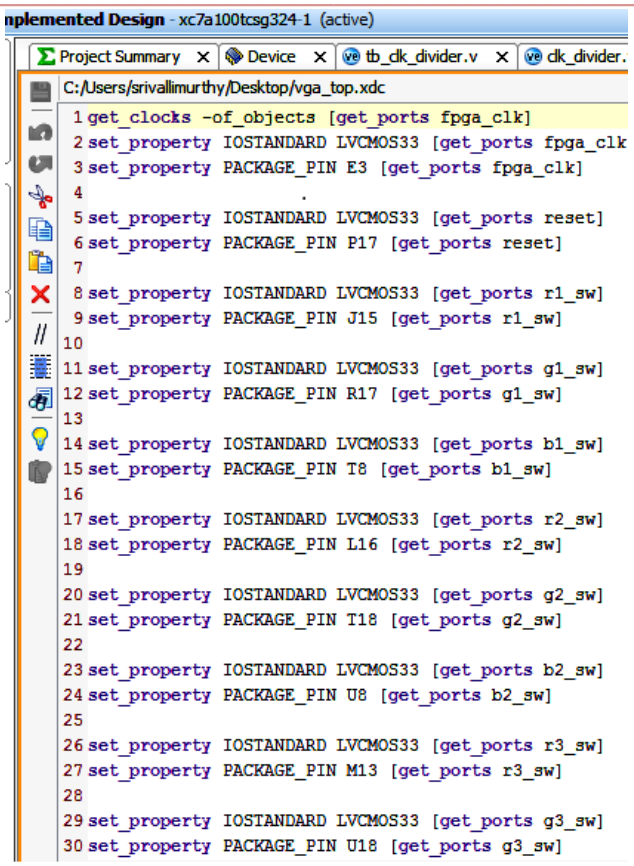

Fig.9 Design Constrained File [6]

IX. CONCLUSION

Hence the FPGA is very useful for designing and implementation of many logic circuits including VGA controller by using hardware description language such as Verilog . Thus, Controller circuit can be made by just simulation and synthesizing the the program code in the Vivado. It also feeds the program to the FPGA. The proposed VGA control shows the systematuc used for FPGA to develop this system, which display colors on a VGA screen. This can be used in any FPGA device.

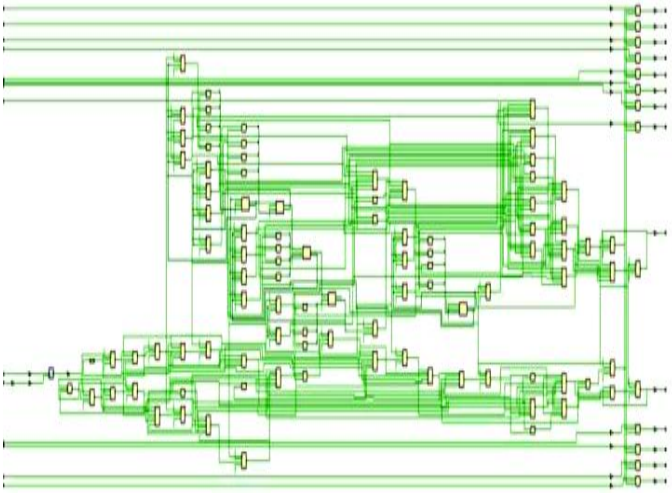

Fig. 10 Schematic of VGA Controller [6]

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