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Design and Testing of High Speed Multipliers by using Reversible Liner Feedback Shift Register

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Abstract:- In recent designs of IC's (Integrated Circuits) BIST (Built-In Self-Test) is becoming vital for memory where memory is essential part of SoC (System on Chip). BIST design technique allows circuit for self testing. A technique may provide the short test-time as compared to test which applied externally and it allows a use of the low cost test instruments throughout the all production stages. Because of LFSRs randomness properties, it requires less hardware overhead. In particular dissertation, optimization and structure design of BIST design is based on the Reversible LFSRs, which are described. As well Reversible LFSR and Proposed LT LFSR are used to design and test Architecture of different Multipliers such as Array Multipliers and Booth Multipliers.

Keywords— *LFSR, BIST, Power Dissipation, Booth Multiplier, Array Multiplier, Test Patterns.*

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I. INTRODUCTION

LFSR is a register for shift which intakes the capacitance of linearity as the input of bit. Majorly the capacitance of linearity that is deployed in the singlet bits is XOR. Also LFSR is termed as register of shift in which the bit of input is determined by XOR of some bots accumulated in the value of a standard register of shift.

The figure that commences in LFSR is termed as seed & the function that register performs on ground of deterministic nature & the earlier stages determine the current figures. Moreover, in light of the fact that there are some determined stages that are accumulated in the register & it must in the end enter a rehashing cycle. Nonetheless, the LFSR that possesses a chosen function of report may furnish some bits in a defined order that can have a greater cycle of clock & random nature. The wield of LFSRs incorporate creating whitening sequence, fast-digital counters, pseudo noise sequences, and pseudo random numbers. Both the software and hardware usage of LFSRs are pre deterministic. The calculation performed to find out redundancy also helps to identify flaws that are accumulated with LFSR.

In electronics (consumer), LFSR may be utilized as a counter. At the point when utilized as a part of this way, are attractive on the grounds that they perform the function with less assets and normally much faster than conventional type counters, for example binary counters or gray code counters. Despite the fact that it conflicts with instinct, LFSRs can likewise be utilized to create pseudo-noise which is utilized like digital cable and cell-phones as consumer-electronics to build the dependability of the signal. LFSRs can likewise be as a part of spread spectrum systems. A spread spectrum system uses the entire bandwidth signal; which can use to transfer information (data) by spreading the data-frequency over numerous frequencies in the bandwidth. The following frequency to be used is controlled by the LFSR sequence. Other more basic applications of a LFSR is the utilization in devices with white noise & producers of music, where they are utilized to make the electrically delivered music sound more natural.

Another application of LFSRs is the production of pseudo-random sequences that can be utilized as a part of cryptography. LFSR-sequence is pseudo random number-sequence which may connected to a message as a cipher, as clarified in example 3 underneath. All through particular paper, cipher may be the binary terms sequence which is added to binary-message to give the encoded message, otherwise called cipher text. Cipher encodes message hence to know somebody with the key knows the correct approach to decode the message and is then ready to peruse the message; anybody without the key gets the cipher text and reads just gibberish. The key is a bit of information that permits a user to focus the specific type cipher to utilize as a part of encrypting message. In the digital communication, enciphering of message with LFSR-sequence is same as including pseudo random noise. The correct beneficiary with a key expels the noise from the message, however a third-party without key which interprets message just as the noise.

II. PREVIOUS WORK

A. LFSR is a circuitry that is constituted of various flip flops linked to each other in series to each other. The outcome generated by one is taken to be as an input for the proceeding. The polynomial of feedback which is also termed as polynomial which is characterized is implemented to concentrate on the taps which determines how long the pattern which is random will be formulated.

The scenario as represented in the figure is implemented to obtain a relation of LSFR with the theory of matrix & polynomial that is characterized. In this circuitry the forms of feedback are deployed to be resultant as an outcome from the 4^{th} & 1^{st} register. Some defined taps points in the direction of the bigger polynomial. By implementing the theory of matrix, an adjoining matrix is required to be deployed to inter relate it

with the proceeding stage. The real series of LFSR will be BT, BT2 & onwards. Here B is termed as vector of seed. The determinant of matrix T is termed as producer polynomial while the polynomial which is characterized is inverse of it. The elaborated absorption of power to produce an environment for assessment by the lines may as a rule surpass the attainment of greater absorption of power by IC which reduces the losses in device which cannot be repaired. It commences by a design formulated by making use of a traditional LFSR which eliminates the loss in out-put. Prior to techniques for decreasing the power dissipation amid the testing is formulation of assessment by RSIC that is deployed to produce patterns of assessment in minimal power. A defined formulation of absorption of power is made minimal though at some extra price of around 19%, an extra procedural step is suggested which is the LFSR with lessen transitions. This eventually brings down the extreme & aggregated power of amid the assessment. In next step, algorithm of ATPG & model of flaws is picked to start with, and after that the designs of tests are formulated to attain the needed flaw. A production of the lessen power design of assessment is recommended by F.corno_et_al for a circuitry which is sequential. In the research, while assessing the circuitry, redundancy can be obtained. This will minimize the absorption os power by not enhancing the flaws eventually.

III. BASIC LFSR

It is some sort of producer of numbers which are random & faked. A register which have 4 bits is counted to display working of LFSR. It is commenced by taking some value of seed. It is then transferred to right & bit of XOR at the outcome of extreme & initiating F/F. At that point the outcome generated by logical gate of XOR is intended to give an input to the initial FF. as an illustration seed is taken as 0101.

Shift of 0101 is 1010 & fell off of 1.
Shift of 1010 is 1101 & fell off of 0.
Shift of 1101 is 0110 & fell off of 1.
Shift of 1100 is 0011 & fell off of 0.

There are numerous qualities of LFSR that is possesses before it rehash or repeat the cycle. The maximum period of time of LFSR is 2^n-1 that is before any repentance & n is the register's width. In a defined approach, the transactions are much higher & then minimize the link of patterns of tests that are adjoining & determined by LFSR. The deducing of relations enhances the decadence of power while in the process of assessment, in this manner builds power consumed by BIST.

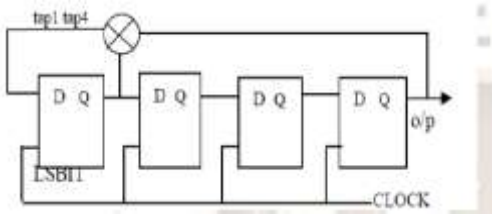

Figure 1:- LFSR Architecture (Standard)

IV. PROPOSED METHODOLOGY

It is methodology that permits to formulate substantial hardware & software attributes to IC which further permits them to assess own their own. Eventually it deduce the reliance on additional ATE.

We replace LFSR by the reversible LFSR. For reversible LFSR we design the Feyn gate for to enhance the execution. In such gates number of input & outcomes are equivalent & there lies coordinated correspondence in between vector of outputs and inputs, that is., it may produce unique output vector from every input vector and the other way around.

The vector for outcome & input abbreviated as OV & IV respectively for a 2 * 2 FG is determined in a way to take as: IV is equal to a, b where as OV equivalents to P =A, Q=A B. the figure 1 sows the diagram of FG of 2*2 values. It is also termed as CNOT. The main aspects to use this gate in a circuitry which can be reversed are:

I) replicate input & putting value of B as 0
II) inversion of bit & putting value of B as 1

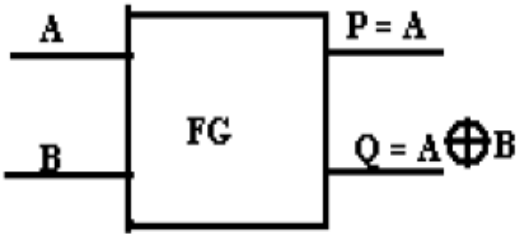

Figure 2:- Feynman Gate

We apply the reversible logic gate in the LFSR. For XOR operation we call the fey men gate for to enhance the power quality of the system. We are enhancing the outcomes as far as delay and power. We call the Feynman gate program 3 times for to complete the execution. Feynman gate contains two outputs and two input. So we characterize it in entity. Inputs are characterize by a, b and output are characterize by p,q.

```
st1: feyn port map(lfsr_reg(7),lfsr_reg(5),d1,x1);
st2: feyn port map(x1,lfsr_reg(4),d2,x2);
st3: feyn port map(x2,lfsr_reg(3),d3,x3);
```

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We apply the Feynman gate in LFSR. As the program is demonstrating that we call the Feynman gate 3 times. In the first operation LFSR (7)bit and LFSR(5) bit is as an input d1,x1 are output. Operation of XOR is coming in the x1. At that point x1 and LFSR (4) is as an input. D2 and x2 are the output. XOR operation output is coming in the x2. Presently x 2 and LFSR (3) is as an input and d3 and x3 as the output.

After this reversible LFSR is brought in final program. At the spot of LFSR we call the program of reversible LFSR.

```
library ieee;
use ieee.std_logic_1164.all;


entity feyn is
port(a,b:in std_logic;
     p,q:out std_logic);
end feyn;

architecture behav of feyn is

begin

p<=a;
q<=a xor b;

end behav;
```

V. RESULTS

	Used	Total	Utilization(%)
Slices Register	25	93296	1
Number used as Flip Flop	16		1
Number of Slices LUT's	254	46648	1
Number used as logic	249	46648	1
Number of occupied Slices	106	11662	1
Number of MUXCYs used	32	23324	1
Number with an unused Flip Flop	260	365	4

Table 1:-Synthesis Report for Proposed Design

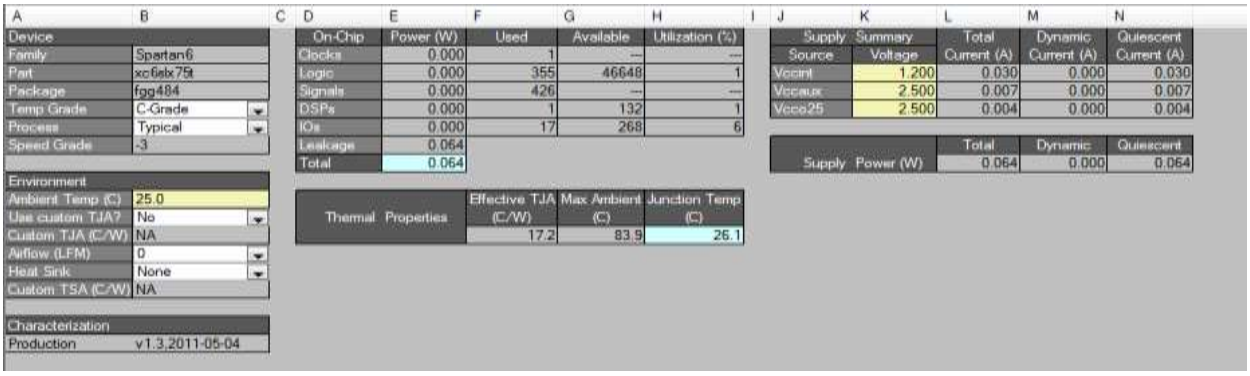

Figure 3:- For proposed design

Figure 4:-Wave form for the proposed design

As the above image is showing the values of the output. The output value is fault to detect the fault status.

4.3 COMPARISON OF THE EXISTING AND PROPOSED DESIGN

	PROPOSED LFSR	EXISTING LFSR
Slices Register	25	53
Number used as Flip Flop	16	43
Number of Slices LUT's	254	355
Number used as logic	249	354
Number of occupied Slices	106	121
Number of MUXCYs used	32	32
Number with an unused Flip Flop	260	312
Delay	2.096 ns	8.533 ns
Power	0.064 W	0.064 W

Table 2:- Comparison of the existing and proposed design

VI. CONCLUSION & FUTURE SCOPE

The recommendation is of enhancement in research on the producers of designs of assessment. The methodologies that are deployed are been transferred as the venture of switching is minimized from the designs assessed are generated by the producer. The invasion of venture of switching is to bring down the terminologies with the producers of designs of assessments in a fashion of efficiency in power. Thus the traditional LFSR will be transformed by the logical gate which can be reversed. By adjustment of this structure, assessment of the multipliers possessing greater speed in carried out to evaluate the throughput of multipliers. The main superiority of the LFSR is it can be incorporated with any devices that consume minimal power To even decrease the power.

In the future we can introduce the pipelining of the three stages and four stages for reduce the delay and area of the RTL.

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