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# Top-Down Integration Methodology for Clocking Blocks into High Speed Serial IO

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***Abstract:*** High Speed Serial Input-Output (HSIOs) design architecture is widely used for many applications in today's System-On-Chips (SOCs). SOCs integrate a number of protocols including PCIe, SATA, SD4, USB3, etc. which are based on IO architecture. Typical HSIO integrates Analog blocks such as Receiver (Rx), Transmitter (Tx) and Clocking (PLL, Clock Distribution) functions along with sea of logic gates for PCS (Physical Connectivity Sub layer), logic micro-partitions for Tx/Rx power management, encoding/decoding and Serialization/Deserialization functions. The top level design database is typically RTL leading to a sea of gates when synthesized. The top level design is implemented using standard ASIC design flow including RTL, Simulation, Synthesis, Timing, Place & Route, and Formal Verification etc. However, the partitions for Tx, Rx, PLL and Clocking are Analog/Custom hard-macros. To ensure proper functionality, integrity (for low power, timing, Place and route, Mixed Signal/IP level validation) we need to model hard-macros in a digital friendly manner. For functionality verification purpose, we model the macro behavior in Verilog, timing needs to be abstracted in industry standard liberty file format (lib file), for place and route we abstract the physical information in LEF/FRAM format etc. In HIP, while there are methods to build these individually, streamlined methodology for building these with consistency, quality and flow friendly manner is missing. The focus of this project is to formulate a methodology for hard-macro integration into top level HSIO database, and apply this for Secure Digital card (SD4) IO that is being developed in IP Blocks.

***Keywords:*** *Behavior modelling (BMOD), Electrical Rule Check (ERC), PVT (Process Variation and Temperature), Assertion.*

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## 1. INTRODUCTION

Various blocks are integrated together to form a SOC. The different blocks can be bifurcated into analog blocks and digital blocks. The various blocks that come together are like transmitter, receiver, clock distribution network, phase locked loop, SerDes, amplifier, analog to digital converter, digital to analog converter etc.

Transmitter is basically used to transmit the data over the channel. There are different functions that transmitter has to take care of like matching of the output impedance to the characteristic impedance of the channel, slew rate control of the signal to match the slew rate requirements of the channel etc.

The SerDes is basically used to serialize the parallel data that is fed to it. So it is generally a parallel to serial converter. The PLL and the Clock distribution network are responsible for the generation of the appropriate frequency clock for various blocks and its proper distribution. At the receiver end the data received is sampled at appropriate intervals and read. The serialized data is then converted to parallel and given to next block.

A SDIO (Secure Digital Input Output) card is an extension of the SD specification to cover I/O functions. SDIO cards are only fully functional in host devices designed to support their input-output functions (typically PDAs like the Palm Treo, but occasionally laptops or mobile phones). These devices can use the SD slot to support GPS receivers, modems, barcode readers, FM radio tuners, TV tuners, RFID readers, digital cameras, and interfaces to Wi-Fi, Bluetooth, Ethernet, and IrDA. Many other SDIO devices have been proposed, but it is now more common for I/O devices to connect using the USB interface.

## 2. OBJECTIVE OF THE PROJECT

The top level design database is typically RTL leading to a sea of gates when synthesized. The top level design is implemented using standard ASIC design flow including RTL, Simulation, Synthesis, Timing, Place & Route, and Formal Verification etc. However, the partitions for Tx, Rx, PLL and Clocking are Analog/Custom hard-macros. To ensure proper functionality, integrity (for low power, timing, Place and route, Mixed Signal/IP level validation) we need to model hard-macros in a digital friendly manner. For functionality verification purpose, we model the macro behavior in System Verilog to mimic the analog behavior in digital sense.

## 3. PHYSICAL LAYER INTERFACE ARCHITECTURE

Figure 1.1 illustrates an example of the interface architecture of physical layer in case of point to point connection between Host and Card. The UHS-II interface utilizes

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transmission Lines (including socket and pins) and terminations which are meant to keep the impedance matching for high speed transmission. UHS-II interface introduces the additional pins for high speed data transmission. UHS-II interface has continuous variable data rate from 39MB/sec to 156MB/sec as effective data rate.Device shall cover the whole range.

UHS-II has two data Lanes. As default, one Lane (D0) is used for downstream (from Host to Device), and another Lane (D1) is used for upstream (from Device to Host). Both data Lanes may be used for downstream Lanes or upstream Lanes at the same time by activating the 2L-HD mode (optional). The transmitted data is encoded by 8b/10b encoder. The Differential Clock (RCLK) may be tuned in the range of 26MHz to 52MHz. Regarding Card, RCLK is sent through the legacy SD transmission lines DAT0, DAT1 and corresponding Card pins. Amplitude Detectors, which detect the Lane's electrical level, are equipped to Host side of D1 Lane (optional) and Device side of D0 Lane (mandatory). Amplitude Detectors make the I/O circuits, such as receiver, to wake up when transmission is resumed at the Lane after Dormant state.

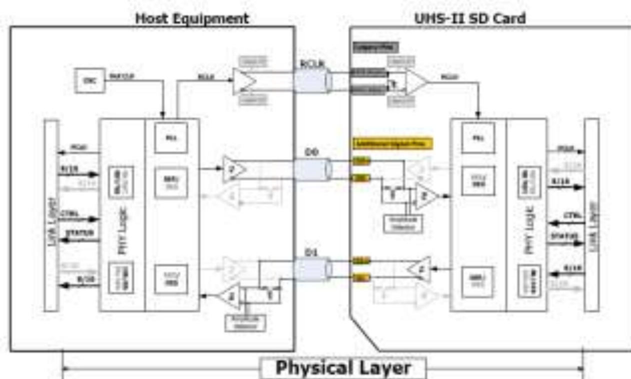


**Fig.1 – Interconnection of host device with physical layer**

D0 is used for downstream (from Host to Device), thus WRITE data and command are transferred from Host to Device on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D0 Lane as upstream (from Device to Host).

D1 is used for upstream, thus READ data and response are transferred from Device to Host on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D1 Lane as downstream. D0 and D1 Lanes are used for differential transmission between Host and Device which are dedicated to UHS-II interface only, and are separate for signals of legacy SD interface. The D0 and D1 signals are encoded by 8b/10b code before transmission, and decoded by 10b/8b after receiving.

## 4. BEHAVIORAL MODELLING AND ASSERTIONS

Any design can always be divided into two sets of blocks. Analog blocks and Digital blocks. For digital blocks we start with RTL code. RTL code is written meeting the requirements of the design. The RTL code is then synthesized to generate the schematic. This schematic is what goes onto layout. However for analog blocks we cannot follow the same process. We cannot write RTL code for analog blocks which later can be synthesized. However while testing the design at system level we will always need the analog support for the RTL code representing the digital blocks. Hence we represent analog block behavior in digital sense with the help of behavior models.Behavioral Models are representations of analog blocks. We can create analog behavioral models with Verilog AMS or digital behavioral models with System Verilog (and Verilog).

Behavioral models are created to enable logic validation, to enable SoC Customer functional validation, to enable Tops Down Design via robust means of modelling and to speed up mixed signal design and validation time.

Assertions are used to validate a specific behavior of a design. They can be used to answer the question "Is my design working properly?" Assertions can capture assumptions made on the interface, expected outputs, and local relations. They increase the ability to capture the design intent. They are a powerful validation tool and catch greater than 25% of all bugs! Assertions are more local then checkers and shorten the debug process as they point directly to the bug.

Concurrent assertions are triggered by some sampling signal, typically a clock.Require the assertion of some property.The assertion is sampled once per clock period, just before the next active clock edge.

Immediate assertions are procedural statements used in simulation, similar to if/else statements:They are assert/else error statements.Assertions check for a condition to be true: assert (true condition) else, an error is generated.

## 5. RELIABILITY VALIDATION FOR DEVICES AND INTERCONNECTS

As we know the number of devices are increasing immensely on the given chip. When we have millions of devices on the chip the current in the each net has to be maintain such that the during the operating life time of the circuits interconnect metal line can sustain the required amount of current. If the current is higher from that

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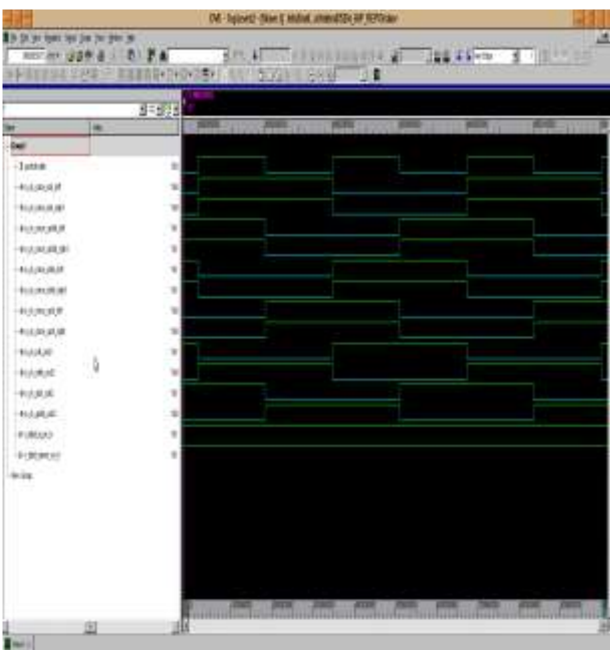
particular value than it will damage the metal line due to the phenomena like electro migration.

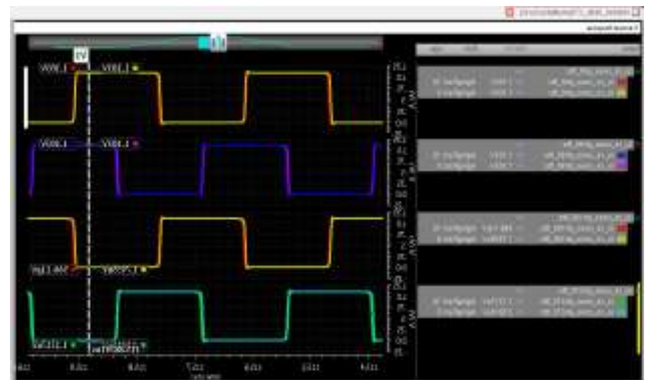
Aging, Burn in and EOS simulations: In the fresh simulation circuit will be subjected to normal operating condition in terms process, voltage and temperature. After that device will be stressed at the elevated temperature and supply, voltages. At the end stress will be removed and circuit will be analyzed to find the remnant effect of given stress on the devices. This is called playback or aged simulation.

Burn-in: In this analysis we need to qualify the circuit for the continuous operation for 10 hours. This analysis will also be carried out in post silicon validation. This is similar to aging simulation but here the devices will be stressed for shorter amount of interval. Sometimes in the circuits due to fluctuations in supply voltages, due to IR drops the performance of the circuits can degrade. So, to analyze such kind of hazardous conditions this simulation is incorporated.

EOS (Electrical Over Stress): This analysis is performed only at elevated temperatures and high supply voltage. In this the transistor will be stressed and the potential difference of each of its four terminals (i.e. drain, source, substrate and gate) will be calculated. So, the violations for vgs, vgd, vds, vsb, vdb is dumped to the text file. In the EOS only stress analysis is perform on the circuit the other two analysis (fresh and playback) are not performed. This is because in EOS analysis our goal is to find out transistor reliability under high supply voltage. According to specifications provided from the process engineers, the degradation in the saturation current of each devices must be less than 20%.

## 6. SIMULATIONS





## 7. CONCLUSION

The reliability of the each device and interconnect will be prerequisite before the actual physical placement of circuits on the silicon. The reliability measures we considering for are hot carrier injection, negative bias thermal instability, electrical over stress, electro static discharge for the devices whereas electro-migration is considered for the interconnect reliability.The clock distribution block has been validated to match all constraints like rise time, fall time, duty cycle etc. It went through the quality and reliability validation and satisfied the specifications under impact of elevated temperature and power supply fluctuations. At the same time it has been simulated for different types of process skew corners.

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