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Analog VLSI Implementation of Feed Forward Neural Network for Signal Processing

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Abstract: With the emergence of VLSI Technology in electronic industry, the numerous applications of integrated circuits in high-performance computing, consumer electronics, and telecommunications has been rising steadily, and at a very fast pace. Artificial intelligence is integral part of a neural network is based on mathematical equations and artificial neurons. The focus here is the implementation of the Neural Network Architecture (NNA) with on chip learning in analog VLSI for generic signal processing applications. The artificial neural network comprises of analog components like multipliers and adders along with the tan-sigmoid function generating circuit. The given architecture uses components such as Gilbert cell mixer (GCM), neuron activation function (NAF) to implement the functions an artificial neural network. With the balanced operation of the Gilbert cell clearer output is obtained by eliminating unwanted signals. The architecture is designed using 180nm CMOS/VLSI technology with Cadence virtuoso tool.

Keywords: *Gilbert cell mixer (GCM), Neuron activation function (NAF), neural network architecture, signal processing.*

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I. INTRODUCTION

In the modern world of global digitization most of the work by human is done using digital computers i.e, from complex digital computation to handling robotics in manufacturing unit. Though computers are widespread in use, a human brain is considered to be far more superior to a digital computer. A simple example would be the way human brain processes a visual image or a fast reflex of human muscle when it comes in contact with an extreme heat source. The human brain uses its 'intelligence' while responding to any task which is a major motivation in developing neural networks. The human brain consists of neurons that send activation signals to each other thereby creating intelligent thoughts. The electronic version of a neural network algorithm (called an artificial neural network) also consists of neurons which send activation signals to one another. The goal of a neural network is to create an artificial intelligence which could replicate the functions of a human brain. Thus neural is receiving much attention in past decade.

A neural network is a powerful data modeling which able to capture and represent complex input/output relationships. A neural network is composed of highly interconnected processing units (neurons) which work together in parallel to achieve a specific task. Artificial Neural Networks are indeed self-learning mechanisms which don't require the traditional skills of a programmer. With the advent of new technologies there is a need to develop the processor to processes the information artificially as our biological system performs inside our body. Artificial intelligence is realized based on mathematical equations and artificial neurons. Here our main focus is on the implementation of chip design for Feed-forward Neural Network Architecture (NNA) in VLSI for generic analog signal processing applications. The analog components like Gilbert Cell Multiplier (GCM), Adders, Neuron activation Function (NAF) are used in the implementation.

An elaborate representation of the artificial neural network is as shown in figure1. In this network, inputs v1, v2 are applied with the weight matrix, and then these weighted inputs of the adder are summed up. The output generated by adder blocks is given to the Neuron Activation function. The output of

activation function is multiplied by weights again and given to the input blocks of output layer.

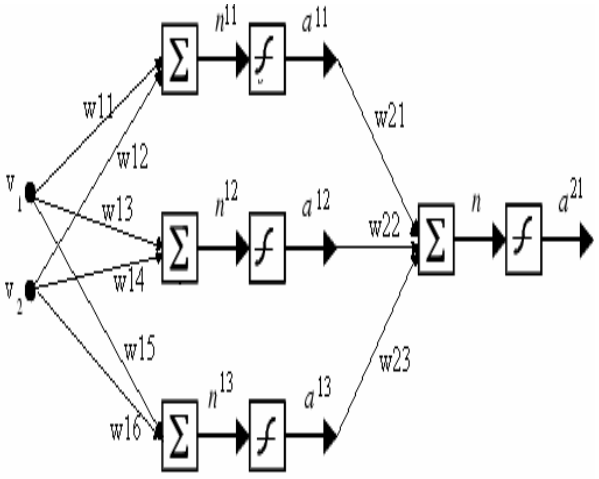

Figure 1. Layered neural network

A general artificial neural network consists of three layers:

- Input units.
- Hidden units.
- Output units.

The layers of 'input' units are connected to a layer of 'hidden' units, which is connected to a layer of 'output' units.

This layered structure of neural network is implemented in VLSI using analog components. Gilbert cell multiplier and differential amplifier are used for different blocks.

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II. IMPLEMENTATION OF GILBERT CELL MIXER FOR PROPOSED NEURAL NETWORK ARCHITECTURE

There exist several multiplier circuits operating in weak inversion. Multiplication can be performed by various circuits. Important issues when choosing multiplier are linear range, noise figure, offset problems, size and type of input/output signals.

The Gilbert cell uses the linear, time varying circuit to achieve time domain multiplication. Gilbert cell multiplier is also known as double balanced mixer. The major components of a GCM are differential pair transistor and current mirror circuits. There are several GCMs using different number of balancing (Differential pair transistor) stages for signal isolation. The multiplier and adder block of the neuron is implemented using a Gilbert cell multiplier.

The general block diagram of a GCM is as shown in figure2.1. Here radio frequency and local oscillator signals are given as input to the mixer for producing the required output frequency signal.

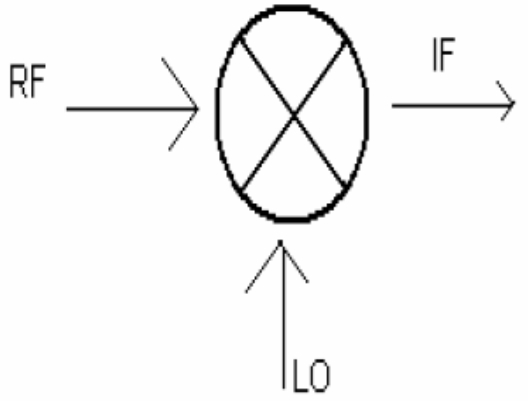

Figure 2.1. Mixers in Integrated circuits

The mixing result produces two signal located at the LO+RF and LO-RF frequency. One signal is the wanted IF signal and the other is the unwanted signal as shown in the following equations:

$$RF = A\cos(RF)* t \quad (1)$$

$$LO = B\cos(LO)* t \quad (2)$$

$$IF = A\cos(RF)*t + B\cos(LO)*t \quad (3)$$

$$IF= 1/2 *AB [\cos(LO+ RF)*t +\cos(LO- RF)*t] \quad (4)$$

A double balanced mixer is used in the proposed architecture. It is basically a combination of two single balanced mixers. The current mirror network at the bottom of the mixer is used to increase the linearity and stability of the mixer. The double balanced mixer prevents any LO products from reaching the output, thereby eliminating the susceptibility found in single balanced mixer. The circuit schematic of transistorized CMOS double balanced mixer is as shown in figure2.2.

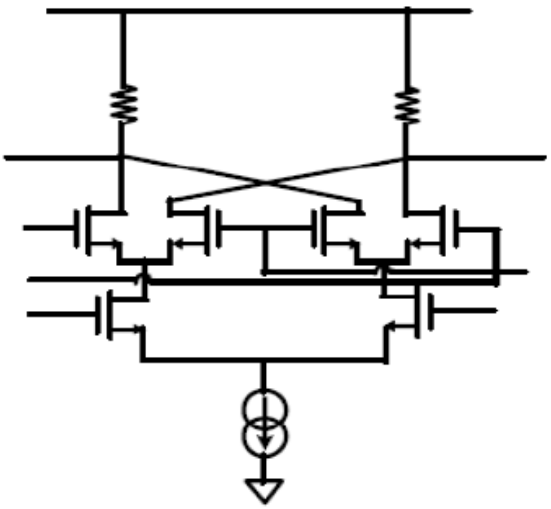

Figure 2.2. Double balanced mixer

III. IMPLEMENTATION OF NEURON ACTIVATION FUNCTION FOR PROPOSED FEED FORWARD NEURAL NETWORK ARCHITECTURE

Complex surfaces can be described by simple networks using Sigmoid type activation function. Nonlinear activation functions of neurons are essential for neural network operation. Such Sigmoid functions can be created in the differential pair. The differential amplifier is used as NAF to obtain the tan-sigmoid function. It is used at the of each neuron i.e, after GCM. The circuit schematic of a GCM is as shown in figure3.

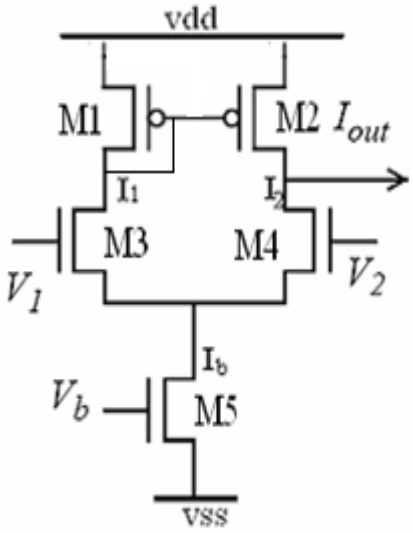

Figure 3. Neuron activation function

The NAF network could output zero and one, one and minus one, or other numeric combinations. So the simple transfer function that handles all these combinations is a sigmoid function.

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IV. RESULTS AND DISCUSSIONS

The following figure 4.1 shows the circuit schematic of a GCM designed using cadence virtuoso tool. The entire circuit design is carried out using 180nm VLSI technology.

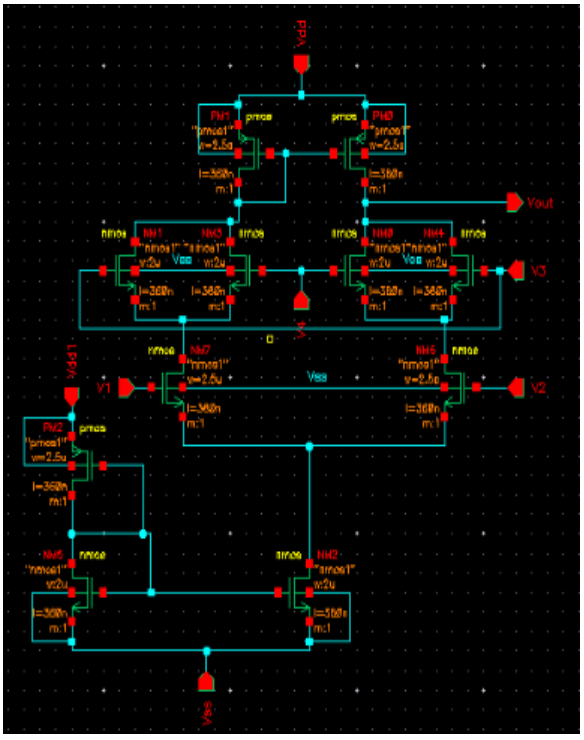

Figure 4.1. Schematic of GCM

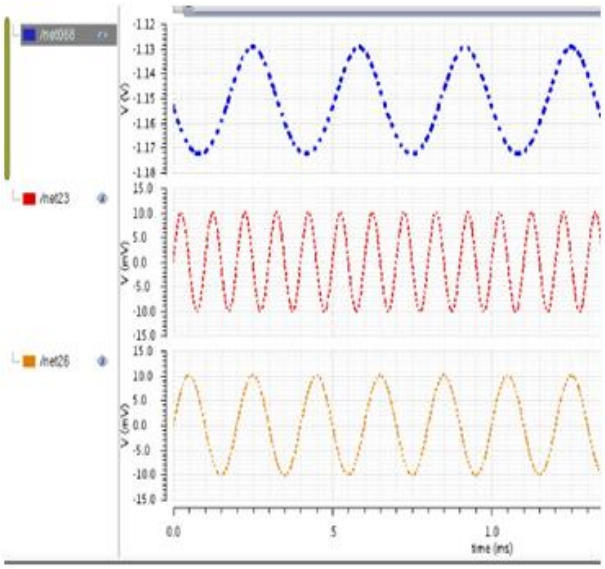

Figure 4.2. Voltage v/s time response of GCM

The figure 4.2 shows the output response of a Gilbert cell multiplier. Here the two inputs are provided with 50mv Vpp and the obtained output signal is 0.625v Vpp. The circuit schematic of a neuron activation function which is essentially a modified differential amplifier is as shown in fig4.3.

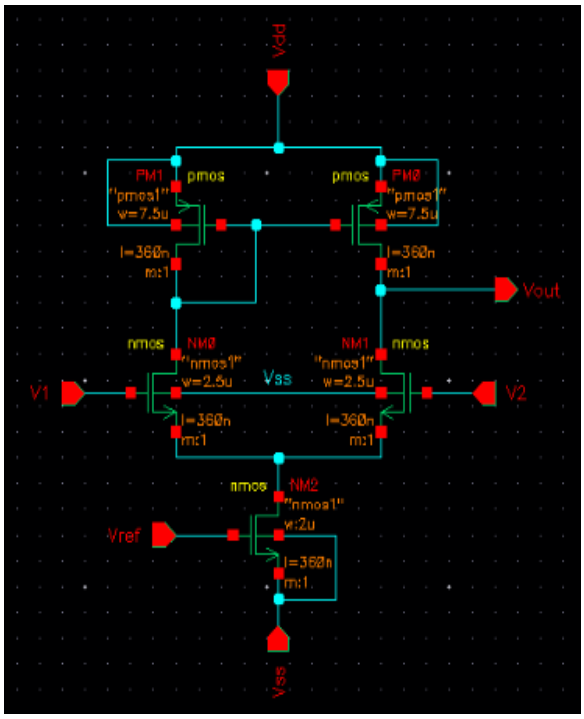

Figure 4.3. Schematic of NAF

The nonlinear tan-sigmoid function required at the output node each neuron is obtained using NAF is as shown in figure 4.4.

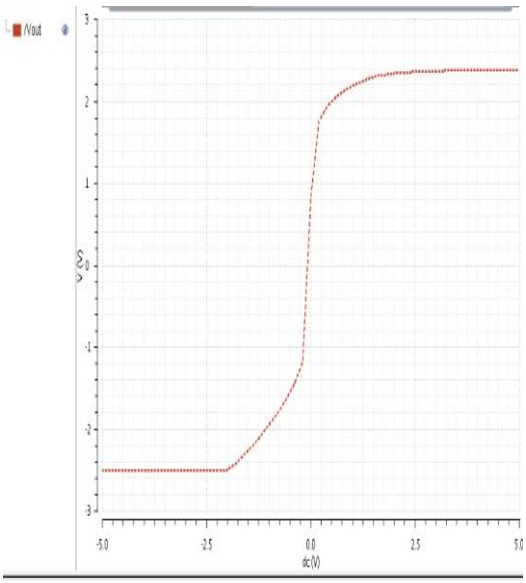

Figure 4.4. DC response of NAF

The schematic design of feed forward neural network for signal compression is as shown in figure 4.5.

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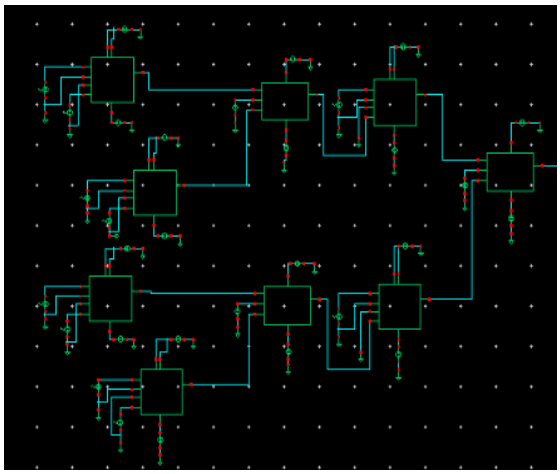

Figure 4.5. Schematic of neural network for signal compression

The simulation result of feed forward neural network for signal compression is as shown in figure 4.6. The result obtained is evident for bandwidth reduction in analog domain.

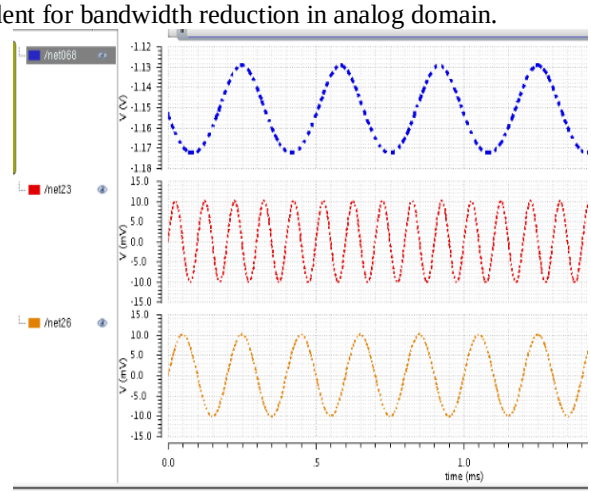

Figure 4.6. Voltage v/s time response of signal compression in neural network

The schematic design for signal decompression is as shown in figure 4.7.

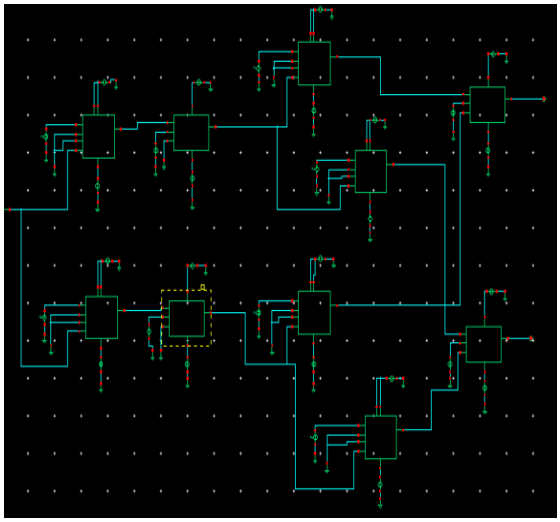

Figure 4.7.Schematic of neural network for signal Decompression

Figure 4.8 shows the voltage response of signal decompression in neural network where the input signals are regenerated at the output.

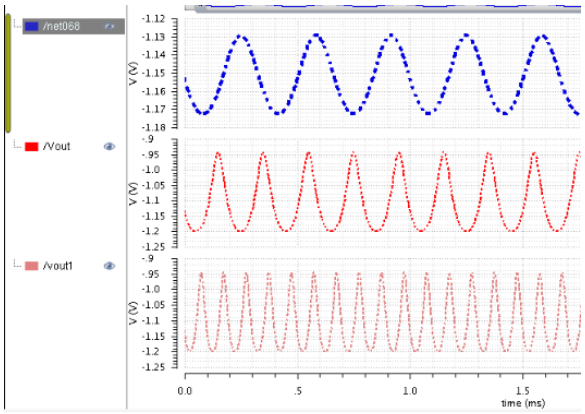

Figure 4.8: voltage v/s time response of signal Decompression in neural network.

V. CONCLUSION

The VLSI implementation of feed forward neural network is successfully demonstrated in this paper. To replicate the function of synapse a analog multiplier known as GCM is used. Differential amplifier was used to generate sigmoid function. The feed forward network was successfully implemented in signal compression, where two analog signals were used as input to obtain a single output signal. In decompression technique the obtained output signal was used to regenerate the input signals.

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