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A Network Structure for Diagnosis of Four Types of Faults in Reed-Muller Canonical Circuits

V. Geetha
Associate Professor, EEE
GCT, Coimbatore
Tamilnadu, India
e-mail: geetha@gct.ac.in

P.N. Neelakantan
Principal (Retd.)
ACCET, Karaikudi
Tamilnadu, India
e-mail: pnn1012@gmail.com

Abstract—In this paper, a new network structure and its associated universal test set, independent of the circuit function, and dependent only on the number of function variables, with good fault diagnosing capabilities have been proposed for single stuck-at, double stuck-at, AND-bridging and OR-bridging faults in Exclusive-OR Sum of Products (ESOP) Reed-Muller Canonical (RMC) circuits.

Keywords-*Reed-Muller canonical; ESOP; stuck-at faults; bridging faults*

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I. INTRODUCTION

Logic networks are usually designed by using 'AND' and 'OR' gates. However, the networks using AND-EXOR gates have some advantages over the conventional AND-OR networks. In general, any arbitrary logic function can be expressed in Exclusive-OR Sum of Products (ESOP) Reed-Muller Canonical (RMC) form as, $F = a_0 \oplus a_1x_1^* \oplus a_2 x_2^* \oplus \ldots \oplus a_nx_n^* \oplus a_{n+1} x_1^* x_2^* \oplus \ldots \oplus a_m x_1^* x_2^* \ldots x_n^*$ where, x_n^* can be x_n or its complement, a_n is either 0 or 1 and $m = 2^n-1$. However, there can be variations in such forms. The different types are Fixed Polarity RMC (FPRM), Positive Polarity RMC (PPRM), Generalised RMC (GRM) and Exclusive-OR Sum-of-Products RMC (ESOP). The FPRM has a restriction that the variables in any of the product terms have to be of the same type namely complementary or non-complementary. For PPRM, the complementary form of variables is not allowed. The GRM may contain both complementary and non-complementary types but the combination of the variables should be unique. The ESOP form does not have any such restriction. Such networks often require fewer gates and interconnections than those designed using AND and OR gates. Second, they can be made easily testable. The ESOP form has the least number of product terms and hence needs the least number of AND gates and is very much suitable for hardware implementation. Examples of such networks include arithmetic, telecommunication and error correcting circuits.

II. LITERATURE SURVEY

A PPRM network for detection of stuck-at faults with a universal test set of size n+4, n being the number of data inputs, was proposed in [1]. Though quite good for self-testing, the method is economical only for the specified form, which obviously has more number of product terms than the other forms in most cases. Multiple stuck-at fault detection for ESOP circuits was carried out in [2]. However, since the cardinality is $2n+6+ \sum nC_e$, e = 0 to j, the order of ESOP expression, the test set is not universal and also is too large to be practical for large input functions. Stuck-at and bridging faults with a universal test set for PPRM network has been reported in [3]. Multiple fault detecting GRM realizations was proposed in [4]. Reference [5] described an ESOP implementation with a universal test set of size n+6 for single stuck-at faults only.

In [6] it was demonstrated that single stuck-at fault detection can be achieved with only n+5 test vectors. It was shown in [7] that 2n+s+3 test vectors are required for single stuck-at fault detections in GRM / ESOP circuits while 2n+s vectors are required for detection of AND/OR-bridging faults in such circuits , where s is the number of product terms in the logic function. Here too, the test set is not universal as it depends on s, the number of product terms of the function. References [8], [9] proved that a test sequence of length 2n+8 vectors is sufficient to detect all single stuck-at and bridging faults. Two new methods, each with a small modification in this scheme with ESOP RMC circuits had been proposed for analysis and diagnosis of single stuck-at faults [10], [11].

In [12],[13],[14], it was demonstrated how the RMC forms help in the detection of various digital faults and how to determine the best polarity among them. It was proved that test vectors for multiple fault detection and diagnosis in digital circuits could be generated using Neural Network with different training algorithms [15]. Reference [16] proposed a new test pattern generation algorithm using Neural Network which requires additional gates. The analysis and diagnosis of OR-bridging faults in any of the pairs of data and control lines and OR-bridging faults including intermediate gate outputs of the ESOP RMC circuits was proposed in [17], [18].

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In [19], a modification regarding auxiliary outputs of the network given by [6] was proposed for four types of faults namely single stuck-at, double stuck-at, AND-bridging and OR-bridging. The network structure and test set proposed by [6] was extended for double stuck-at, AND-bridging and OR-bridging types of faults [20]. It was proved by the authors that the same network structure with limited test set can be used for the other three types of faults also. The two auxiliary outputs of the structure in [20] were replaced by a single auxiliary output in [21] by the same authors. The simulation results were found to be much better than in [20].

The literature survey shows that research is being carried out for the past 45 years in the field of fault detection in digital circuits, especially with the network structure of Reed-Muller canonical form. Test vectors for determining various types of faults such as the basic single stuck-at, multiple stuck-at, bridging and stuck-open categories had been tried out with various modifications of the basic ESOP networks. The cardinality of the test vectors proposed by many authors become prohibitively excessive for a large number of input variables.

III. MATERIALS AND METHODS

A. Network Structure

The proposed network structure is shown in Figure 1. The complementary variables x_1', x_2'... are represented as zl_1, zl_2... and serve as additional inputs. An AND block, an XOR function tree block which implements the required logic function F and also an additional output O obtained through a separate XOR gate are also present. The actual data inputs to the system are x_1, x_2 …. x_n. Additionally, the scheme requires three control inputs c_1 to c_3 from which one of them is connected to each AND gate of the AND block as per the logic mentioned in a succeeding section. Finally, all the data inputs, complementary variable inputs present in the function and the control inputs are applied to a separate XOR gate producing the auxiliary output O to aid in the detection of faults which cannot be differentiated by the main function output F alone.

B. Test Vectors

The generalized test set for the proposed structure is shown in Table I. The test set has (n+5) vectors; each of the vectors is (n+nzl+3) long, 'n' being the number of data inputs and 'nzl' being the number of complementary variables.

The first three columns of the matrix represent the three control inputs c_1 to c_3, the next 'n' columns that of the data inputs x_1 to $x_n$followed by nzl columns corresponding to the number of complementary inputs available in the function.

The test vectors are applied as the logic values of the input, complimentary and control variables; the resulting outputs F and O are converted to decimal values and tabulated for convenience and easy comparison.

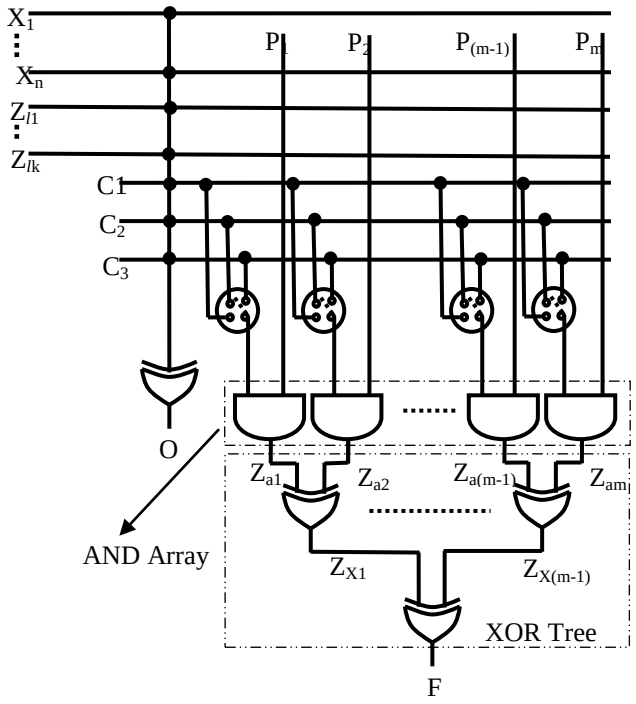

Figure 1. Generalized Proposed Network.

TABLE I. GENERALIZED TEST SET

c_1	c_2	c_3	x_1	x_2	…	x_n	zl_1	zl_2	...	zl_{nzl}
0	0	0	0	0	. . .	0	0	0	...	0
0	1	1	1	1	. . .	1	1	1	...	1
1	0	1	1	1	. . .	1	1	1	...	1
1	1	1	1	1	. . .	1	1	1	...	1
1	1	1	0	1	. . .	1	0	1	...	1
1	1	1	1	0	…	1	1	0	…	1
1	1	1	1	1	…	1	1	1	…	1
.	.	.	.	.			.	.		.
.	.	.	.	.			.	.		.
.	.	.	.	.			.	.		.
1	1	1	1	1	. . .	0	1	1	...	0
0	0	0	0	0	. . .	0	1	1	...	1

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C. Control Signal Assignment

The assignment of control signals for the network is represented in Figure 2.

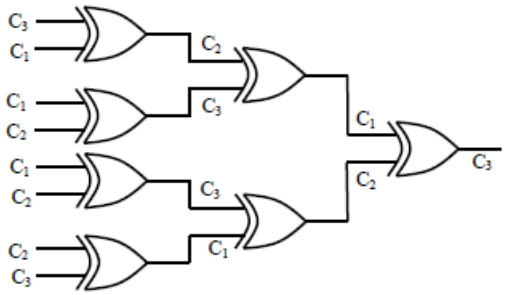

Figure 2. Control Signal Assignment

The algorithm for assigning the control lines is as follows:

Step 1: Draw the circuit for the required function.
Step 2: Assign the numerals 1, 2 and 3 respectively to the two inputs and the output of the final XOR gate producing the function output F.
Step 3: Consider each XOR gate connected to the inputs of the final XOR gate considered in *Step* 2. Assign the outputs of these XOR gates with the same numbers as the
inputs of the final XOR gate of *Step* 2.
Step4: If the output of the XOR gate considered is 1, then assign 2 and 3 to its inputs; else if the output is numbered 2, assign 3 and 1 to its inputs.
*Step 5:*Consider the next earlier input stage and assign the same numerals as the output points connected from the previous steps.
*Step6:*Assign cyclic numerals as discussed in previous steps.
Step 7: Repeat until the basic input stage of the XOR gate tree is reached.

The numerals indexing this input stage incremented by 1 indicates the cardinality of the control line to be connected to the AND gate block.

D. Algorithm for Fault Diagnosis

Step 1: Set up the circuit as in Figure 1.
Step 2: Connect the control lines c_1 to c_3 as explained in the preceding section.
Step 3: Apply the test vectors as given in the Table 1, one by one.
Step 4: For each test vector applied, determine the three fault-free outputs F and O.
*Step*5: Simulate the single stuck-at type of fault and determine the corresponding outputs F and O.
Step 6: Compare the sets of outputs with the predetermined fault-free outputs.

If the two output sets match exactly, it implies that a fault, if present, is not
identifiable or detectable; else, the fault is a detectable one.
Step 7: Repeat *Step*s 4 to 6 for all inputs and outputs of all gated except those of auxiliary output, which is assumed to be fault-free.
Step 8: Repeat *Step*s 4 to 7 for Double stuck-at, OR-bridging and AND-bridging faults for other possible combination pairs of control inputs, data inputs and intermediate gate outputs in the network.

E. Identifiabilty and Distinguishability Factors

For all the faults, the identifiability factor and distinguishability factor are calculated as explained below.
Step 1: The set of Boolean outputs (Main and auxiliary) for each test vector is determined for the given circuit assuming it to be fault free.
Step 2: The output Boolean vectors are each considered separately and their decimalequivalents are determined by standard binary to decimal conversion process.
Step 3: The above two *Step*s are repeated for single stuck-at faults at various locations of the circuit.
Step 4: The total number of faults for which the decimal equivalents of the outputs sets are identical to the output set of the fault-free operation is counted.
Step 5: The total number of possible faults is determined from a knowledge of input and output points including intermediate gates of the circuit.
Step 6: The ratio in percentage of the total number of faults obtained in *Step* 4 to the total number of possible faults as known in *Step* 5 gives a measure of the unidentifiable faults, from which the identifiability factor can be determined.
Step 7: The number of total faults for which the decimal equivalents of the output sets F and O are different from the fault-free output sets are counted.
Step 8: The ratio of the number counted in *Step* 7 to the total number of possible faults is the indistinguishability index.
Step 9: The distinguishability factor is determined by subtracting the percentage indistinguishability from 100%.

IV. FUNCTIONS CONSIDERED FOR SIMULATION

The following ten random functions F_1 to F_{10} have been considered and simulated for two reference structures and the proposed structure using MATLAB coding for Single-stuck-at, Double-stuck–at, AND-bridging and OR-bridging faults:

$F_1 = x_1 \oplus x_2x_3 \oplus x_1'x_2x_3$
$F_2 = x_1x_2 \oplus x_2'x_3 \oplus x_3'x_4 \oplus x_1x_2x_3$
$F_3 = x_1' \oplus x_2x_3'x_4 \oplus x_3x_4' \oplus x_2'x_3 \oplus x_1x_4x_5$
$F_4 = x_1x_2' \oplus x_2x_3x_4' \oplus x_4x_5'x_6 \oplus x_2x_5 \oplus x_2'x_5' \oplus x_3'x_2x_1 \oplus x_4x_6$

$F_5 = x_1'x_2x_3 \oplus x_4x_5x_6 \oplus x_4'x_6'x_7 \oplus x_3x_5x_7$
$F_6 = x_1x_2'x_3 \oplus x_4'x_5x_6' \oplus x_7x_8' \oplus ' \oplus x_1'x_6 \oplus x_3'x_4 \oplus x_1x_5 \oplus x_4x_5' \oplus x_5x_7 \oplus x_8x_3x_1 \oplus x_3x_5'x_8$
$F_7 = x_1x_2'x_3' \oplus x_4x_5'x_6 \oplus x_7'x_8x_9 \oplus x_1'x_4'x_9' \oplus x_2x_5' \oplus x_3x_5$
$F_8 = x_1'x_2x_3' \oplus x_4'x_5'x_6 \oplus x_7x_8'x_9' \oplus x_{10} \oplus x_6'x_7 \oplus x_8x_{10}$
$F_9 = x_1 \oplus x_2'x_3x_4' \oplus x_5'x_6x_7' \oplus x_8x_9x_{10} \oplus x_{10}'x_{11} \oplus x_1x_3x_9$
$F_{10} = x_1'x_2 \oplus x_3x_4'x_5 \oplus x_6x_7'x_8x_9 \oplus x_{10}x_{11}'x_{12} \oplus x_1x_2x_3' \oplus x_4'x_7$

Table II shows some of the features of the reference and proposed network structures.

TABLE II. CERTAIN FEATURES OF REFERENCE AND PROPOSED NETWORK STRUCTURES

Network Structures	No. of Control lines	No. of Outputs		No. of Inputs for Auxiliary output(s)	No. of Test Vectors	Length of Test Vectors
		Main	Auxiliary			
Reference Structure 1 [6]	4	1	2	n+nzl	n+5	n+4
Reference Structure 2 [21]	3	1	1	n+nzl	n+5	n+nzl+3
Proposed Structure	3	1	1	n+nzl+3	n+5	n+nzl+3

where n is the number of data inputs
nzl is the number of complementary inputs

V. NUMERICAL ILLUSTRATION

Thefunction $F_1 = x_1 \oplus x_1x_2 \oplus x_1'x_2x_3$ having three variables is taken as an example for numerical illustration.
In addition to the give data and control inputs, there is an additional data input zl_1, which differs from the data input x_1 only in the last test vector.
The main function output expression is given by
$F = c_2x_1 \oplus c_3x_1x_2 \oplus c_2x_1'x_2x_3$.
There is one auxiliary output O having the logic expression $x_1 \oplus x_2 \oplus x3 \oplus c_1 \oplus c_2 \oplus c_3 \oplus zl_1$.

A. Single Stuck-at Faults

The total number of possible single stuck-at faults is,
2*(n+nc+nzl+nza+nzx) = (3+3+1+3+2) = 2*12 = 24.
where, n is the number of data inputs = 3 (for function F1)
nc is the number of control inputs = 3
nzl is the number of complementary inputs = 1
nza is the number of AND gate outputs = 3 and
nzx is the number of XOR gate outputs = 2

B. Double Stuck-at Faults

Double stuck-at faults can occur easily due to the shorting of any two of the lines, especially the adjacent lines of the circuit. The network structure and test vectors are the same as those for the single stuck-at fault. However, in the test procedure, two lines at a time have been considered and made as stuck-at-0 or stuck-at-1 and simulated. Since two lines are involved, four possible combinations, viz.(0,0), (0,1), (1,0) and (1,1) for each pair of lines including the data lines, the control lines, the intermediate gates and the output.
The total number of fault location pair combinations
=4* (n+ nc+nzl+nza+nzx) C_2 = 4*12C_2= 264.

C. AND-Bridging Faults

The bridging faults are considered as a special case of multiple faults. In an AND-bridging fault, all the lines involved in the fault have the same post-fault values as the logical ANDing of their pre-fault values. In the present research, only two lines are assumed to be faulted at a time and of non-feedback type. Unlike the double fault, this type has only one combination of logical ANDing of pre-fault values. Hence, the number of fault possibilities is 1/4 of the double fault case = (n+nc+nzl+nza+nzx)C_2 / 4 = 66.

D. OR-Bridging Faults

In an OR-bridging fault, all the lines involved in the fault have the same post-fault values as the logical ORing of their pre-fault values. In the present research, only two lines are assumed to be faulted at a time and of non-feedback type.The total number of fault possibilities is (n+nc+nzl+nza+nzx)C_2 /4 = 66.

The fault-free outputs and the total number of fault possibilities in the proposed network structure for the four types of faults mentioned above is shown in Table III.

TABLE III. FAULT-FREE OUTPUTS AND NUMBER OF POSSIBLE FAULT COMBINATIONS FOR FOUR TYPES OF FAULTS IN THE PROPOSED STRUCTURE

Sl.No.	Function	No. of Data Inputs	Fault free outputs		Total No. of Possible Single Stuck-at Faults	Total No. of Possible Double Stuck-at Faults	Total No. of Possible AND-Bridging Faults	Total No. of Possible OR-Bridging Faults
			F	O				
1	F_1	3	126	25	24	264	66	66
2	F_2	4	206	44	32	480	120	120
3	F_3	5	496	386	42	840	210	210
4	F_4	6	978	188	52	1300	325	325
5	F_5	7	1728	405	40	760	190	190
6	F_6	8	4032	1022	80	3120	780	780
7	F_7	9	6204	2027	60	1740	435	435
8	F_8	10	14276	12819	62	1860	465	465
9	F_9	11	26098	5541	60	1740	435	435
10	F_{10}	12	49598	51643	62	1860	465	465

VI. SIMULATION RESULTS

Adopting the algorithms outlined in previous sections, the percentage identifiability and distinguishability are determined for the four types of faults in the circuits for ten functions mentioned above, the simulation results are shown in Tables IV toVII as also the respective inferences.

TABLE IV. CONSOLIDATED IDENTIFIABILITY ANDDISTINGUISHABILITY FACTORS FOR SINGLE STUCK-AT FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

Fn.	% Identifiability			% Distinguishability		
	Ref. Struct. [6]	Ref. Struct. [21]	Proposed Structure	Ref. Struct. [6]	Ref. Struct.[21]	Proposed Structure
F1	84.62	83.33	**100**	84.62	91.67	**100**
F2	97.06	96.88	**100**	82.35	87.50	**100**
F3	95.45	95.24	**100**	95.45	95.24	**100**
F4	96.30	96.15	**100**	92.59	96.15	**100**
F5	97.62	97.50	**100**	73.81	90.00	**100**
F6	96.34	96.25	**100**	97.56	97.50	**100**
F7	98.39	98.33	**100**	83.87	96.67	**100**
F8	98.44	98.39	**100**	78.13	96.77	**100**
F9	98.39	98.33	**100**	79.03	96.67	**100**
F10	98.44	98.39	**100**	78.13	96.77	**100**
Average	**96.11**	**95.88**	**100**	**84.55**	**94.49**	**100**

Inference: The identifiability as well as the distinguishability for all the ten random functions considered are 100%. Hence single stuck-at fault in any of the input lines, control lines, output lines or the intermediate gate lines is completely identifiable by the proposed method.

TABLE V. CONSOLIDATED IDENTIFIABILITY ANDDISTINGUISHABILITY FACTORS FOR DOUBLE STUCK-AT FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

Fn.	% Identifiability			% Distinguishability		
	Ref. Struct. [6]	Ref. Struct. [21]	Proposed Structure	Ref. Struct. [6]	Ref. Struct.[21]	Proposed Structure
F1	98.40	98.11	**100**	30.13	32.20	**68.18**
F2	100	100	**100**	31.25	42.29	**66.67**
F3	99.89	99.88	**100**	33.98	55.12	**70.95**
F4	99.93	99.92	**100**	33.26	52.23	**65.23**
F5	100	100	**100**	29.64	55.79	**75.79**
F6	100	99.90	**100**	32.50	59.46	**65.74**
F7	100	100	**100**	32.80	67.30	**77.30**
F8	100	100	**100**	31.50	69.14	**78.82**
F9	100	100	**100**	33.12	68.45	**78.05**
F10	100	100	**100**	31.10	69.14	**78.44**
Average	**99.82**	**99.78**	**100**	**31.93**	**57.11**	**72.52**

Inference: The identifiability for all the ten functions is 100%. Hence the proposed method completely detects a double stuck-at fault in any of the 264 possible fault combinations. Further, the average distinguishability factor has improved by about 127%, compared to the Structure[6] and by about 27% over the Structure[21].

TABLE VI. CONSOLIDATED IDENTIFIABILITY ANDDISTINGUISHABILITY FACTORS FOR AND-BRIDGING FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

Fn.	% Identifiability			% Distinguishability		
	Ref. Struct. [6]	Ref. Struct. [21]	Proposed Structure	Ref. Struct. [6]	Ref. Struct.[21]	Proposed Structure
F1	85.90	87.88	**98.48**	47.44	57.58	**80.30**
F2	95.59	94.17	**100**	36.76	76.67	**86.67**
F3	89.18	95.71	**99.52**	47.62	76.67	**87.62**
F4	90.88	97.54	**100**	52.42	78.77	**87.38**
F5	86.19	93.16	**98.95**	48.10	81.58	**93.16**
F6	91.59	97.69	**99.74**	58.66	85.51	**89.74**
F7	91.40	97.01	**99.77**	47.74	83.22	**89.43**
F8	90.52	97.20	**99.78**	33.06	83.87	**90.54**
F9	90.75	96.09	**99.54**	38.49	86.90	**94.71**
F10	89.11	95.48	**99.57**	47.98	86.88	**90.54**
Average	**90.11**	**95.19**	**99.54**	**45.83**	**79.77**	**89.01**

Inference: The fault detection is very close to 100% on an average, for the functions considered. The proposed method also has shown an improvement in distinguishability by about 94% compared to the Structure[6] and by about 11% over the Structure[21].

TABLE VII. CONSOLIDATED IDENTIFIABILITY ANDDISTINGUISHABILITY FACTORS FOR OR-BRIDGING FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

Fn.	% Identifiability			% Distinguishability		
	Ref. Struct. [6]	Ref. Struct. [21]	Proposed Structure	Ref. Struct. [6]	Ref. Struct.[21]	Proposed Structure
F1	84.62	84.85	**92.42**	58.97	59.09	**74.24**
F2	98.53	100	**100**	52.21	78.33	**85**
F3	96.54	98.10	**99.52**	59.74	64.29	**81.43**
F4	96.58	99.08	**100**	67.24	70.46	**84.31**
F5	98.57	100	**100**	85.71	78.42	**87.89**
F6	98.29	99.62	**100**	70.12	74.49	**84.74**
F7	98.28	100	**100**	79.14	76.55	**83.68**
F8	98.59	100	**100**	85.89	86.67	**91.40**
F9	98.71	99.77	**99.77**	86.88	88.74	**91.95**
F10	98.79	**100**	**100**	80.85	80.43	**87.31**
Average	**96.75**	**98.14**	**99.17**	**72.68**	**75.75**	**85.2**

Inference: The fault detection is closer to 100% than the other two network structures compared, on an average. The proposed method also has shown an improvement in distinguishability by about 17% compared to the Structure[6] and by about 12% over the Structure[21] for the functions considered.

Summary: From the simulation results presented above, it can be seen that the proposed structure outperforms the other two structures in both the identifiability as well as distinguishability for all the four types of faults considered. The role of the control function in a network aiding in the identification and distinguishing the fault is highlighted from the test results. Here, all the lines viz. input lines, output lines and intermediate gate output lines are considered in fault simulations.

VII. CONCLUSION

In this paper, a new network structure and its associated universal test set, independent of the circuit function, and dependent only on the number of function variables, with good fault diagnosing capabilities have been proposed for single stuck-at, double stuck-at, AND-bridging and OR-bridging faults in ESOP RMC circuits.

For stuck-at faults, a line has been assumed to be either stuck-at-0 or stuck-at-1 at a time. For double stuck-at faults, only two lines have been assumed to be involved at a time. However, the two lines can be any pair of lines involved. The bridging faults have been assumed to be of single (involving only one pair of lines at a time) and of non-feedback type. Tree type EXOR function block has been assumed for the reduction of propagation delay. The gates of auxiliary output are assumed to be fault-free.

All the primary input lines, primary output line and all the inputs and outputs of the various gates of the circuit have been considered for the simulation of the various types of faults considered.

The analysis and diagnosis of the various types of faults have been performed through the use of two quantification indices. Ten random ESOP RMC functions from three to twelve variables have been simulated in MATLAB and compared for fault detection capability. A result compaction technique has been used for the ease of tabulation and comparison of the results.

The identifiability factor, is almost 100% for all the functions considered randomly and the distinguishability factor also has improved very much compared to the reference structures.

The tabulated distinguishabilty factor is an overall value. Though the overall factor may be poor in some cases, its value for an individual output set is much higher. Further, the detection capability is not affected by this factor. It is also easy to identify the actual faulty line from the set of outputs measured.

REFERENCES

[1] Reddy S.M., “Easily Testable Realizations for Logic Functions”, IEEE Trans. on Computers, vol.21, no.11, Nov.1972, pp. 1183-1188.

[2] Pradhan D.K., “Universal Test Sets for Multiple Fault Detection in AND-EXOR Arrays”, IEEE Trans. on Computers, vol.27, no.2, Feb.1978 pp. 181-187.

[3] Bhattacharya B.B., Gupta B., Sarkar S and Choudhury A.K. “Testable Design of RMC Networks with Universal Tests for Detecting Stuck-at and Bridging Faults”, IEE Proc.Computers and Digital Techniques, Vol.132, Part E., no.3, May 1985. pp. 155-162.

[4] Sasao, T., “Easily Testable Realization for Reed-Muller Expressions”, IEEE Trans. on Computers, vol.46, no.6, Jun.1997, pp. 709-716.

[5] Kalay U, Hall D.V. and Petrowski M.A., “A Minimal Universal Test Set for Self-Test of EXOR-Sum-of-Products Circuits”, IEEE Trans. on Computers, vol.49, no.3, Mar.2000 , pp. 267-276.

[6] Zhongliang P., “Testable Realizations of ESOP Expressions of Logic Functions”, Proc. of 11th Asian Test Symposium (ATS”02), IEEE Computer Society, 2002, pp 140-144.

[7] Zhongliang P.,“Bridging Fault Detections for Testable Realizations of Logic Functions”, Proc of 16th International Conference on VLSI Design, Jan. 2003, pp. 423-427.

[8] Hafizur Rahaman, Debesh K.Dass,’Bridging Fault Detection in Double Fixed-Polarity Reed-Muller (DFPRM) PLA’ IEEE Proceedings Asia and South Pacific Design Automation Conference (ASP-DAC’05), 2005, pp 172-177.

[9] Hafizur Rahaman, Debesh K.Dass ,’Universal Test Set for Detecting Stuck-at and Bridging Faults in Double Fixed-Polarity Reed-Muller Programmable Logic Arrays’, IEE Proc.-Comput. Digit. Tech., Vol.153, No.2, March 2006. pp. 109-116.

[10] Neelakantan P.N. and Ebenezer Jeyakumar A., "Stuck-at Fault Test Vectors for Exclusive-OR Sum Reed-Muller Canonical Boolean Functions", GESTS International Transactions on Computer Science and Engineering, Vol. 27, No.1, Jan. 2006 pp. 139-147.

[11] Neelakantan P.N. and Jeyakumar A. E., "Single Stuck-At Fault Diagnosing Circuit of Reed-Muller Canonical Exclusive-Or Sum of Product Boolean Expressions", Journal of Computer Science, USA,Vol.2,Issue7, July 2006, pp. 595-599.

[12] Pan Zhongliang and Chen Guangju, "Fault Detection Test Set for Testable Realizations of Logic Functions with ESOP Expressions", Journal of Electronics (China), Vol. 24(2), 2007, pp. 238-244.

[13] Ling Chen, and Zhong Liang Pan, "Fault Detection of Bridging Faults in Digital Circuits by Shared Binary Decision Diagram", Key Engineering Materials, Tans Tech Publications (Volumes 439 - 440), June, 2010, pp. 1235-1240.

[14] Wenjin Wu, Pengjun Wang, Xiaoying Zhang, Lingli Wang and Dai Jing "Search for the Best Polarity of Multi-Output RM Circuits Base on QGA", Second International Symposium on Intelligent Information Technology Application, Vol. 3, pp. 279 – 282, 2008.

[15] Zhong Liang Pan, Ling Chen and Guang Zhao Zhang, "Test Pattern Generation of VLSI Circuits Using Hopfield Neural Networks", Applied Mechanics and Materials, Trans Tech Publications (Volumes 29 - 32), August, 2010, pp. 1034-1039.

[16] Zhao Ying and Li Yanjuan, "A Multiple Faults Test Generation Algorithm Based on Neural Networks and Chaotic Searching For Digital Circuits", International Conference on Computational Intelligence and Software Engineering (CISE), December 2010.

[17] Geetha V., Devarajan N. and Neelakantan P. N., "OR-Bridging Fault Identification and Diagnosis for Exclusive-OR Sum of Products Reed-Muller Canonical Circuits", Journal of Computer Science, USA, Issue 7(5),July 2011, pp. 744-748.

[18] Geetha V., Devarajan N. and Neelakantan P. N., "OR-Bridging Fault Analysis and Diagnosis for Exclusive-OR Sum of Products Reed-Muller Canonical Circuits", European Journal of Scientific Research, USA, Issue 71, No.4March 2012, pp. 482-489.

[19] Geetha V, Devarajan N, Neelekantan P N, " Analysis of Different Types of Faults in a Class of Boolean Circuits", International Journal of Engineering and Innovative Technology, Volume 2, Issue 4, October 2012, pp. 145-149.

[20] Geetha V., Devarajan N. and Neelakantan P.N., "Single Network Structure for Stuck-at and Bridging Fault Analysis and Diagnosis for Exclusive-OR Sum of Products in Reed-Muller Canonical Circuits", Elixir International Journal, Elec. Engg., 57 (2013), pp. 14080-14085.

[21] Geetha V., Devarajan N. and Neelakantan P.N., "Network Structure for Testability Improvement in Exclusive-OR Sum of Products Reed-Muller Canonical Circuits", International Journal of Engineering Research and General Science, Volume 3, Issue 3, May-June 2015, pp. 368-378.