# Mismatched Load Protected Solid State Amplifier of 1W CWRF Output in Frequency Range of 28 - 46 MHz

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***Abstract***— This project work is associated with the concept, design, fabrication and testing of a continuous wave radio frequency (cwrf) solid state amplifier. This amplifier of gain more than 20dB with 10mW input, will be developed for general application in the frequency range of 28 to 46 MHz. This Low Power Amplifier (LPA) will be made to exhibit a feature of protection from finite mismatched load that causes Voltage Standing Wave Ratio (VSWR) and consequent failure of the solid state device. The rf and microwave circuits including amplifiers are designed for standard 50 transmission line components and load. In case of perfectly matched load, only incident waves exist without any reflection i.e. 1:1 VSWR and maximum power is transferred to the load. In practice, mismatched load persists where reflected waves along with the forward waves gives rise to standing waves that cause damage to the solid state devices due to various reasons. In order to protect the device, the amplifier to be developed, will be treated with various protections so that load mismatch is managed in the most optimised manner.

***Keywords***- *VSWR, load mismatch*

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## I. INTRODUCTION

The cwrf LPA is most important and custom made module in almost all communication systems. This is one of the most demanding, both in terms of development and while operating in the system. These demands have encouraged the development of custom design methodology using traditional and rugged devices along with protective circuits as well as high efficiency and protective operating modes.

RF amplifiers must have a standard nominal output impedance of 50 and ideally would only be used with 50 load impedance. This result in maximum power transfer i.e. 0% power reflected back to the amplifier. It doesn't take a perfect open or short circuit to cause the reflected wave but any mismatch between output impedance and the load.

The amplifier must withstand this impedance mismatch even while operating at rated values of bias voltage, operating current and input power. In order to select a device with the specified ruggedness, it is necessary to understand the root cause mechanism of rf amplifier device failure. An effective protection mechanism including various concepts and circuits must also be designed and included for the expected VSWR.

## II. MOTIVATION AND OBJECTIVE

In general, solid state amplifiers have to encounter mismatched load which causes standing waves due to interference of reflected waves with forward waves in the output line and circuitry.

Standing wave causes high output voltage peaks to appear and device may fail due to junction breakdown. Maximum power is not transferred to load therefore causes overheating of device and consequent lower efficiency or complete failure. This unreliable operation needs frequent replacement of device. Thus, operation time and cost increases.

A universal solution with the objective to protect the rf amplifier device from the mismatched load and above mentioned generally existing problem is essential.

## III. MISMATCHED LOAD IMPEDANCE

The presence of standing wave is an indication of the imperfect condition i.e. load mismatch with part of the power meant for radiation or to be coupled being returned towards source. If there is no mismatch with only forward travelling wave then there is no standing wave and the voltage at any point in the line is the same to that at source or load end.

Standing wave pattern is observed in case of full or partial reflection. If the reflected wave is not as strong as the forward wave then the nulls will neither be as deep nor the peaks as high as for a perfect reflection or complete mismatch. The intensity of the standing wave is referred to as the Voltage Standing Wave Ratio or VSWR.

There are various quantities that describe the quantum of mismatch or power transfer effectiveness to the load or antenna. These are VSWR, reflection coefficient, mismatch loss and the return loss as following,

$$\textbf{VSWR} = E_{max}/E_{min} = (E_{inc} + E_{ref})/(E_{inc} - E_{ref}) = (1 + \Gamma)/(1 - \Gamma) \quad [8]$$

$$\textbf{Reflection Coefficient} = (Z_2 - Z_1)/(Z_2 + Z_1)$$

$$\textbf{Return loss} = 10 \log (P_r / P_i) = 20 \log (E_r / E_i)$$

$$\textbf{Mismatch Loss} = 10 \log (1 - \Gamma^2)$$

The amount of power delivered to the load can be calculated using the above mentioned formulae where,

$E_{max}$ = maximum voltage on the standing wave
$E_{min}$ = minimum voltage on the standing wave
$E_{fwd}$ = incident voltage wave amplitude
$E_{ref}$ = reflected voltage wave amplitude
 = the absolute value of reflection coefficient
$Z_2$ = Larger of the load or source impedance
$Z_1$ = Smaller of the load or source impedance
$P_i$ = incident power
$P_r$ = reflected power

Jacobi's Law, also known as the maximum power theorem state that "Maximum power is transferred when the internal resistance of the source equals the resistance of the load, when the external resistance can be varied, and the internal resistance is constant." This effect is clearly observed when load impedance differs i.e. greater or lesser from the amplifier's output impedance. As VSWR increases, a greater portion of the forward power is reflected back to the amplifier. Since net power is calculated by subtracting the reflected power from the forward going power, it is apparent that any VSWR other than 1:1 will reduce the actual power absorbed by the load. The amplifier must be designed to routinely sink this reflected power without adversely affecting performance or reliability.

With output mismatch of VSWR 10:1, 67% of the output power is reflected back from the load to the source i.e. transistor and remaining 33% is transmitted to the load. This reflected power must be absorbed and dissipated into heat by the rugged transistor without suffering from any damage or degradation. This is usually accomplished during the design stage of the transistor making sure that there is enough drain resistance to absorb the reflected power.

## IV. FAILURE MECHANISM IN DEVICES

There are two reasons namely breakdown voltage and thermal energy that affect the ruggedness of Heterogeneous Bipolar Transistor (HBT) and consequent failure.

The open base static collector emitter breakdown voltage ($BV_{CEO}$) is commonly considered as the voltage limit of the RF output signal swing. The collector emitter breakdown voltage depends strongly on the impedance that is presented on the base-emitter junction of the transistor, for example by the bias circuit. By providing a low impedance path for the avalanche current, resulting from high voltage at the collector-base junction, an amount of this avalanche current flows through this impedance instead of flowing through the emitter-base junction, delaying on that way the bipolar positive feedback that causes HBT failure.

Power Amplifier transistors suffer from over-heating when they operate under extreme conditions. Over heating of bipolar transistor causes destructive breakdown when thermal instability i.e. runaway of device occurs. Moreover, over heating reduces the device life time, due to acceleration of failure mechanism.

## V. PROPOSED WORK

The proposal is to design, fabricate, test and ultimately develop a 20dB gain rf amplifier for a input of 10mW maximum. The amplifier should be generally usable in the frequency range of 28 to 46 MHz. The general purpose, commercially usable, locally available, cost effective and as rugged as possible rf device will be selected for this purpose. The design and development must allow good range of stability and reliability to the operation in terms of withstanding load mismatch to a certain value within 10:1 VSWR i.e. $Z_2/Z_1$= 10.

Remaining of the protection to the device within a mismatch of 10:1 will be provided with the help of feedback controlled and self regulated power supply. The amplifier must keep functioning within $Z_2/Z_1$= 10 and deliver optimised output without sacrificing protection to the device. In case of $Z_2/Z_1$>10, the rf input and then power supply must be switched off so that the output device is unconditionally protected. The protection must be added with decreasing the rf input to the amplifier for safety of the input device and the circuitry whereas output is reduced.

A clear understanding of the aim and required steps to provide a solution will be completed. A block diagram will be generated and concept must be established. Design, fabrication, testing and development of 20dB LPA must be executed. Protections must be classified in terms of various levels depending upon priority and ease in application. As many levels of protections as possible to the input and output device of the amplifier for $Z_2/Z_1$=10 will be designed, fabricated and tested.

The modifications, completeness and expansion in the above are treated as future plan of action.

## VI. PROTECTIONS IN GENERAL

0In microwave sources and amplifiers, an isolator is used before the load to protect the output device from reflected power and consequential large voltage and current swings due to load mismatch[16]. However, isolators are not available in this desired range of frequencies. Hence, different techniques are used whereas regulated and feedback controlled power supplies are found more popular with the commercially available protected solid state amplifiers. Previous work on load mismatches has focused on ruggedness of power transistors, gain control of input device or power supply based control circuitry to protect the transistor in case of large impedance mismatch.

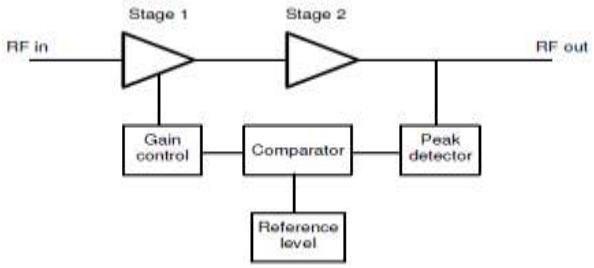


Fig.1. Schematic of a protected LPA in general.

The operating principle of one of the protection mechanism[4] is illustrated in Fig.1. At the output transistors the maximum

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voltage is measured with a peak detector. The output voltage of this detector is compared against a reference voltage corresponding to the junction withstanding voltage. If the measured peak voltage exceeds the reference level, the gain of the input stage is reduced. This reduces the drive level to the output stage. The comparator output is an error signal that represents

## VII. SCHEME AND BLOCK DIAGRAM

The proposed scheme of protected LPA and corresponding block diagram is shown in Fig.2. This is meant for LPA and the complete protection mechanism during operation within a limit of $Z_2/Z_1=10$. The operation of LPA will be cancelled for $Z_2/Z_1>10$ by switching off rf input and the power supply thereby protecting the devices.

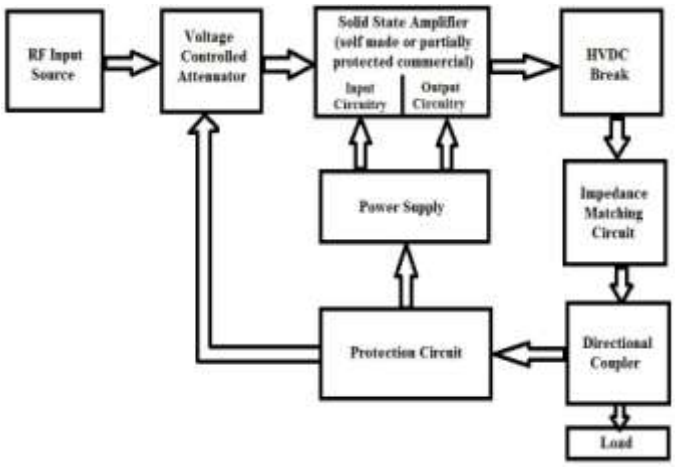


Fig.2. Block diagram for the protection scheme.

Proposed mechanism of operation of LPA for $Z_2/Z_1=10$ is to be accomplished through first level and then with second level protection. The first level protection mechanism involves the feedback controlling of biasing supply w.r.t. output device operating current, device operating voltage and output reflected power. The second level protection mechanism involves the controlling of rf output voltage w.r.t. reflected power, forward power by changing rf input and the operating point.

## VIII. EXPERIMENTAL RESULTS

### A. *POWER SUPPLY CIRCUIT:*

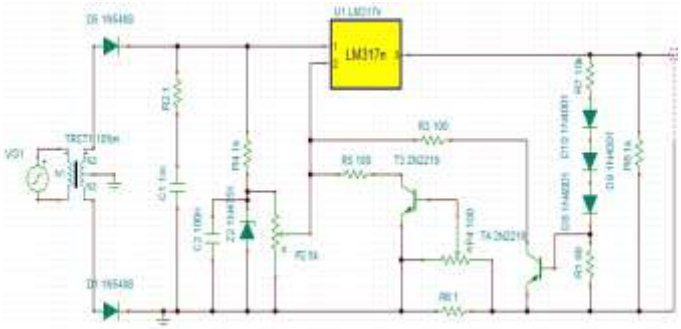


Fig.3. Simulation circuit of 24V Power supply.

Fig.3 shows the circuit diagram of 24V power supply circuit implemented on TINA software. It gives protection from over current and over voltage. This circuitry maintains the voltage level within 24±1V in case of load resistance is infinite i.e. open circuited.

Fig.4. Lab model of Power supply

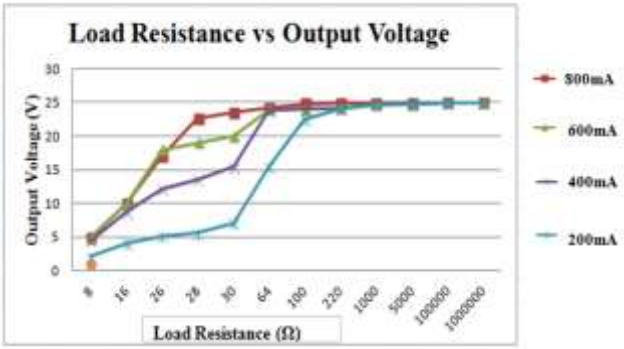


Fig.5. Graph of Load Resistance versus output voltage

Fig.4 shows the lab model of Power supply circuit tested under all load. Fig.5. shows the graph of Load Resistance versus Output Voltage under current conditions for 800mA, 600mA, 400mA and 200mA. We can observe that for open circuit conditions the output voltage regulates to around 25V and does not increase beyond that.

### B. *FIRST STAGE POWER AMPLIFIER:*

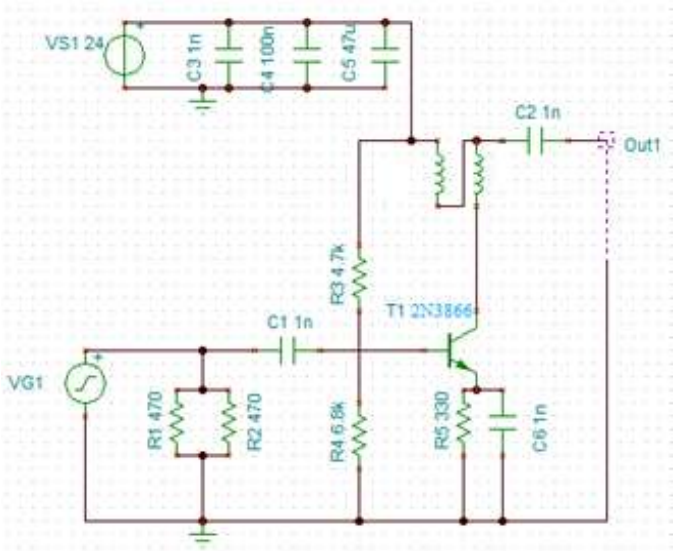


Fig.6. Circuit Diagram of first stage Power Amplifier

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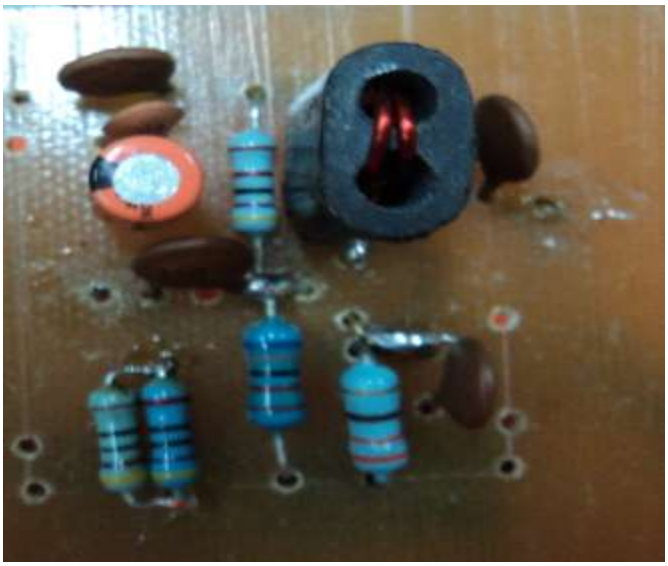

Fig.7. Lab model of first stage Power Amplifier

Fig. 6 and Fig. 7 shows the circuit diagram and lab model of first stage of power amplifier which is made using 2N3866 NPN transistor for low power and high frequency applications. It is basically a Common Emitter configuration with input matching circuitry and output matching circuitry. We have attached a centre tapped transformer made by winding a copper wire around ferrite core.

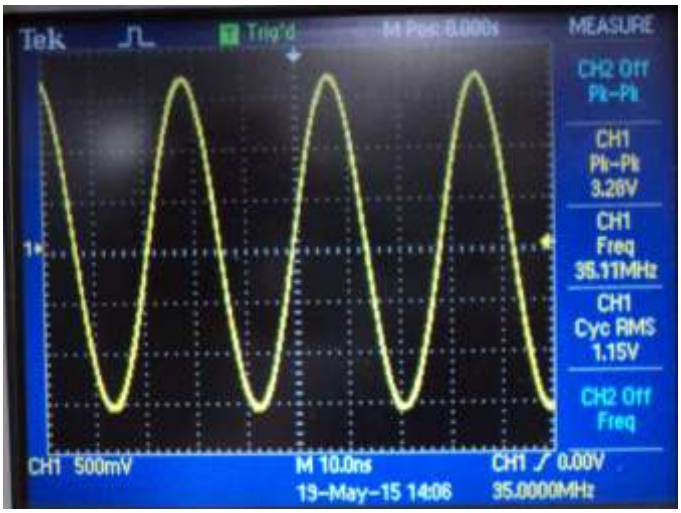


Fig.8. Amplified output of first stage power amplifier at 45MHz

It is basically a Common Emitter configuration with input matching circuitry and output matching circuitry. We have attached a centre tapped transformer made by winding a copper wire around ferrite core.

Fig 8 shows the output waveform of -16dBm input signal at 35MHz frequency, as a result we get 3.28 $V_{p-p}$ voltage. This is equivalent to power gain of 30dBm.

| Input | 28MHz | | | 35MHz | | | 45MHz | | |
|---|---|---|---|---|---|---|---|---|---|
| (dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) |
| -30 | 0.63 | 0 | 30 | 0.8 | 2.04 | 32.04 | 0.64 | 0.1 | 30.1 |
| -29 | 0.66 | 0.37 | 29.37 | 0.88 | 2.87 | 31.87 | 0.72 | 1.13 | 31.13 |
| -28 | 0.73 | 1.27 | 29.27 | 1 | 3.98 | 31.98 | 0.8 | 2.04 | 30.04 |
| -27 | 0.83 | 2.34 | 29.34 | 1.12 | 4.96 | 31.69 | 0.86 | 2.67 | 29.67 |
| -26 | 0.94 | 3.48 | 29.48 | 1.24 | 5.85 | 31.85 | 0.98 | 3.8 | 29.8 |
| -25 | 1.05 | 4.4 | 29.4 | 1.36 | 6.65 | 31.65 | 1.08 | 4.65 | 29.65 |
| -24 | 1.17 | 5.34 | 29.34 | 1.52 | 7.62 | 31.62 | 1.24 | 5.85 | 29.85 |
| -23 | 1.32 | 6.39 | 29.39 | 1.7 | 8.59 | 31.59 | 1.38 | 6.78 | 29.78 |
| -22 | 1.46 | 7.27 | 29.27 | 1.9 | 9.55 | 31.55 | 1.54 | 7.73 | 29.73 |
| -21 | 1.63 | 8.22 | 29.22 | 2.12 | 10.5 | 31.5 | 1.72 | 8.69 | 29.69 |
| -20 | 1.88 | 9.46 | 29.46 | 2.36 | 11.44 | 31.44 | 1.92 | 9.64 | 29.64 |
| -19 | 2.06 | 10.26 | 29.26 | 2.62 | 12.34 | 31.34 | 2.14 | 10.59 | 29.59 |
| -18 | 2.32 | 11.29 | 29.29 | 2.92 | 13.28 | 31.28 | 2.38 | 11.51 | 29.51 |
| -17 | 2.58 | 12.21 | 29.21 | 3.22 | 14.14 | 31.14 | 2.64 | 12.41 | 29.41 |
| -16 | 2.84 | 13.04 | 29.04 | 3.28 | 14.29 | 30.29 | 2.94 | 13.35 | 29.35 |

Table. 1. Response of first stage Power amplifier

Table 1 shows the response of first stage Power amplifier by giving RF input ranging from -30dBm to -16dBm at 28MHz, 35MHz and 45MHz. We get power gain of 30dBm at -16dBm input.

*C. SECOND STAGE POWER AMPLIFIER:*

Second stage power amplifier is also has common emitter configuration using 2N3866 transistor. It has input matching circuitry, amplifier stage and output matching circuitry. In the output matching circuitry, we have used a centre tapped bi-filler coil.

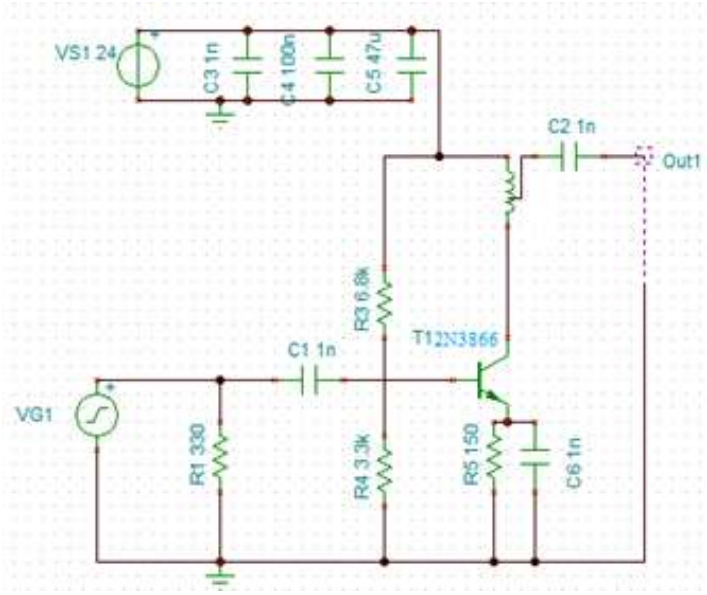


Fig.9. Circuit Diagram of second stage Power Amplifier

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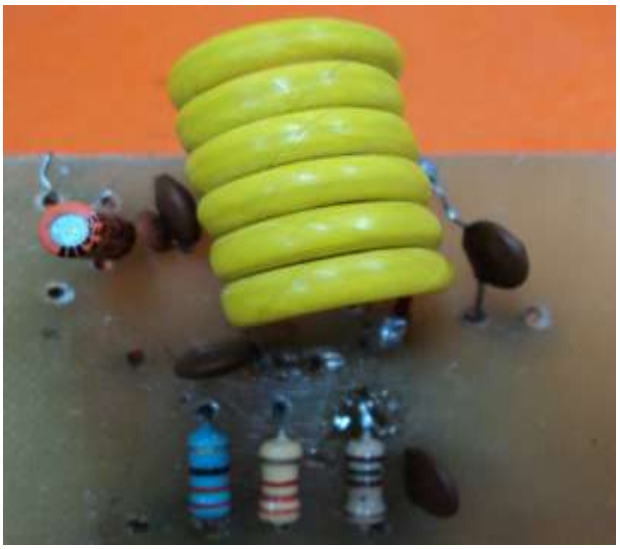

Fig.10 Lab model of second stage Power Amplifier

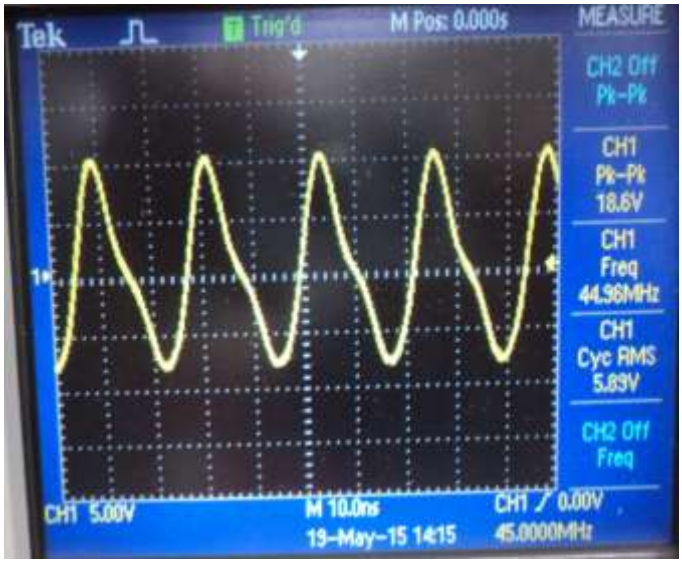


Fig.11Amplified output of second stage power amplifier at 28MHz

Fig 9 and Fig 10 shows the circuit diagram and Lab model of second stage power amplifier made using 2N3866 transistor of gain 10dB. Fig 11 shows the amplified waveform for 13dBm input and giving 18.6$V_{p-p}$ output at 45MHz.

| Input | 28MHz | | | 35MHz | | | 45MHz | | |
|---|---|---|---|---|---|---|---|---|---|
| (dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) | $V_{out}$(V) | $P_{out}$(dBm) | Gain(dBm) |
| 4 | 17.8 | 28.99 | 24.99 | 17 | 28.59 | 24.59 | 15 | 27.5 | 23.5 |
| 5 | 18.4 | 29.27 | 24.27 | 17.4 | 28.79 | 23.79 | 15.2 | 27.61 | 22.61 |
| 6 | 18.6 | 29.37 | 23.37 | 17.8 | 28.99 | 22.99 | 15.8 | 27.95 | 21.95 |
| 7 | 19 | 29.55 | 22.55 | 18 | 29.08 | 22.08 | 16.2 | 28.16 | 21.16 |
| 8 | 19.8 | 29.91 | 21.91 | 18.4 | 29.27 | 21.27 | 16.4 | 28.27 | 20.27 |
| 9 | 20.2 | 30.09 | 21.09 | 18.8 | 29.46 | 20.46 | 16.8 | 28.48 | 19.48 |
| 10 | 20.6 | 30.25 | 20.25 | 19.2 | 29.64 | 19.64 | 17.4 | 28.79 | 18.79 |
| 11 | 21.2 | 30.51 | 19.51 | 19.8 | 29.91 | 18.91 | 17.8 | 28.99 | 17.99 |
| 12 | 21.6 | 30.67 | 18.51 | 20 | 30.00 | 18.00 | 18 | 29.08 | 17.08 |
| 13 | 21.8 | 30.75 | 17.75 | 20.2 | 30.09 | 17.09 | 18.6 | 29.37 | 16.37 |

Table. 2. Response of second stage Power amplifier

Table 2 shows the response of second stage Power amplifier by giving RF input ranging from 4dBm to 13dBm at 28MHz, 35MHz and 45MHz. We get output voltage around 20 $V_{p-p}$ at 10dBm RF input which leads to around 1W output power which is desired.

## IX. FUTURE WORK PLAN

In future, we can execute the second level protection i.e. by controlling output voltage w.r.t. reflected power which can be measured by directional coupler and develop the circuit which would control the reflected power and deliver maximum output to the load.

## X. CONCLUSION

Hence, we developed the power supply protection circuit, two stage power amplifier of power gain 10dB each and getting maximum output power of 1W.

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