Design and Implementation of High-Speed Data Transmission on Multi-Gigabit Transceivers in Spartan 6 FPGA

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Abstract— This paper gives the design of link where the parallel digital data are transmitted serially at the rate of 3.125Gbps on the Spartan 6 evaluation board. The implemented design is to test Aurora 8b/10b protocol in order to transfer 16-bit parallel data serially over the fiber optic cable in full duplex mode. The 16-bit Parallel data are transmitted and received by the Serialized/De-serialized (SERDES) using Multi-Giga bit transceiver (MGT) at the clock rate of 156.25MHz.Aurora protocol converts the parallel data to serial and serial to parallel. The proposed design is simulated in Xilinx 14.2 and implemented on Spartan 6 FPGA. The serial data are transmitted at the rate of 3.125Gbps over the fiber optic link.

Keywords-*Aurora protocol, Multi-Gigabit transceiver, clock wizard*

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I. INTRODUCTION

The field signal from any test facility gives the analog signals. To analyze that number of field signals far from the test facility, the high-speed analog data converted into digital form using analog to digital converters. The analog signals can multiplex and feed to the analog to digital converter. The digital data are transmitted serially through fiber optic cable and converted serial to parallel at the end of the receiver side. So number of the fiber optic link can be reduced to transfer each field signals by using wave division multiplexing. Reconstructed parallel data at the receiver side are input for digital to analog converter to generate an original analog signal.

The paper gives the solution to encode the parallel data into the serial form and also gives the solution for the PLL based clock and data recovery at the end of receiver side with the use of Aurora 8b/10b encoder.

A Multi-Giga bit transceiver (MGT) is an SERDES capable of operating at serial bit rates above 1 Gigabit/second. MGTs are used increasingly for data communications because they can run over longer distances, use fewer wires, and thus have lower costs than parallel interfaces with equivalent data throughput.

II. APPLICATION DESIGN

As Shown in figure 1, the 16-bit high-speed parallel data are given to the FMC board. The high-speed parallel data are coming from the circuitry like analog to digital converter which converts the analog data into digital form. The parameter of ADC may vary with the application. That parallel data are processed, encoded, serialized at higher bandwidth and transmitted over the fiber cable through the small form factor pluggable module (SFP).At the receiver side that serial data are recovered back and converted into serial to the parallel data form. Now that parallel data are input to the circuitry like digital to analog converter. The analog signal can generate back through DAC. The implemented design is divided in parts such as Aurora 8B/10B protocol, Multi-Gigabit transceiver, clock signal parameter selection through clocking wizard and communication channel.

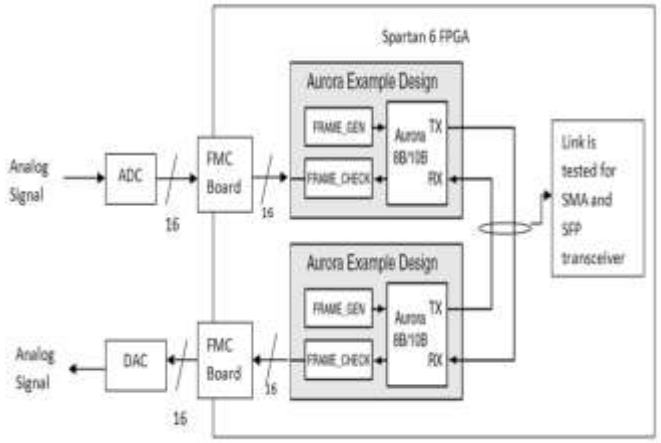

Figure. 1. Block Diagram of Implemented Design.

III. AURORA PROTOCOL

This LogiCORE IP Aurora 8B/10B [1, 4] is lightweight, scalable, link layer protocol for high-speed serial communication. This protocol is very useful for low-cost, high-rate data channels applications. This IP core is open and can be implemented through the Xilinx environment. The user application interface of the protocol can be seen in figure 2.

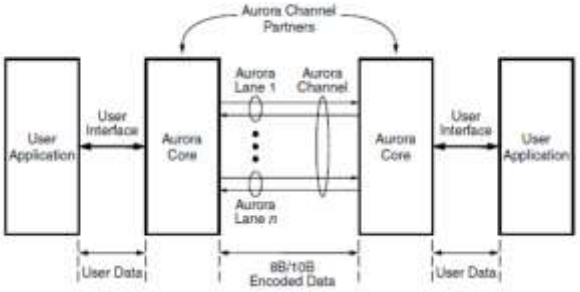

Figure.2 User Application Interface

As per the specification, the protocol contains one more lanes. Each lane is full duplex serial data connection. That can transmit the serial data at the rate from 0.6 Gb/s to 3.125 Gb/s. With the help of channel partner, the user device can communicate together. Those channels are

automatically initiated a channel when they are connected to a channel partner. After the initialization, the user application can transfer the data across the channel as a stream of the framing data structure. The Aurora protocol provides two type of transmission mode:

1. Full Duplex mode,
2. Simplex Mode (Tx- only simplex and Rx- only simplex)

The transmission mode for this design is full duplex mode. The protocol can be customized as per the design. Lane width decides the number of bytes transmitted during the period of one clock cycle. This Aurora protocol supports 2 and 4 lane width. Here for this design the decided lane width is 2 because lane width of 4 is more complex than 4. If the selected lane width is 4 then the user clock (USRCLK) should be half of reference clock (REFCLK). There are two types of data path interfaces used for the core which are Framing and Streaming. Streaming interface is simple word based interface with data valid signal to stream the data through Aurora channel. Framing is a local link interface that allows encapsulation of data frames of any length. Since as per the design to transmit data continuously over the channel link, the streaming interface is selected. The multi-Giga bit transceiver is configured using Aurora 8B/10B protocol that converts each byte of data i.e. 2 byte of data into 20bits (each byte i.e. 8 bits into 10 bits). Here GT REFCLk is 156.250 MHz, which is generated through PLL. So the Line rate will be 156.250 MHz * 20 (bits) equal to 3.125 Gb/s. At this data rate, the serial data are transmitted over the fiber optic channel using SFP module..

IV. CLOCK GENERATION

The clock signal for implemented design is generated through LogiCORE IP Clocking Wizard [9]. This clocking wizard generates clock signals, according to the design specification needs. The Spartan 6 (SP605) board has one 2.5V LVDS differential 200MHz crystal oscillator with 55ppm frequency stability. The clock network parameters are linearly organized in such a way that desired parameters are only been selected for the implementation. As per the clocking wizard, the two things is important for the design which are the allowance of the larger input jitter and minimization of the output jitter. Using the timing parameter of the input clock in the specific unit, the wizard will configure the output clock. Here two output clock is selected for the design, After specifying the input clock parameters such as frequency, phase, and the duty cycle, the wizard configures the output clock signals as per the primitives. For the design, CLK_IN1 is input clock and CLK_OUT1 and CLK_OUT2 are output signals. Parameters which are selected into the clocking wizard are:

1. Clocking features and the output clock: Selection of the check buttons for frequency synthesis and selecting phase alignments.
2. The clock manager type mode is auto selection that wizard select primitives.
3. Jitter optimization is to be selected for the balanced mode.
4. Input clock is of 27 MHz and the input jitter is 0.010ns, source is selected at single ended clocked capable pin.

There are two output frequencies CLK_OUT1 and CLK_OUT2 selected at the output clock setting in clocking. The output frequency of CLK_OUT1 is 200.000MHz requested and 195.750 MHz actual frequency with 50% duty cycle. And CLK_OUT2 is at 156.250 MHz requested and 156.000 MHz actual frequency also with 50% duty cycle. The clock feedback source is set as the automatic control on a chip. The voltage control oscillator frequency is 783.001MHz. The pk to pk jitter for CLK_OUT1 and CLK_OUT2 is 225.658 ps & 238.613 ps respectively with 204.788 phase error. There are 1 divider counter, 29 Multi counter, 5 CLK_OUT1 dividers are used.

V. MULTI-GIGA BIT TRANCEIVER.[5]

Multi-Gigabit-transceiver/Multi-Gigabit-serialize /Deserializer receives parallel data and allows transportation of high-speed data over the serial link design, Spartan 6 have provided 4 MGTs to access. From that four MGTs two MGTs are used, one for SFP module connector and the second one for MGT SMA Connectors, which are used in this designs.

In serializer, the encoder will modify the parallel data & adds some overhead bit. It helps in synchronization and channel transmission in serial. Also, it used to achieving DC balancing, error detection, and clock recovery. In 8B/10B encoding scheme, 8-bit input data is serialized at 10x serial clock. PLL is used to generate serial clock (10x) from the parallel clock. And that serial data transmitted over the differential channel, where at receiver side Deserializer word synchronizer finds word packet boundaries from serial data. The main function of Deserializer is clock and data recovery (CDR). It receives serial data and extracts the synchronized clock either from data itself or generates the synchronized serial clock from reference parallel rate clock. For that phase lock loop is required for both options.

In PLL based clock and data recovery, a phase-frequency detector generates two output signals which are UP and DOWN signals and depends on the phase difference between the input data and the generated clock. A phase difference will be detected as a phase difference and the PDF will generate steady UP-DOWN signal. Now this signals cause the charge pump (CP) to output or source a current, which is converted into the voltage and filtered by the loop filter. This voltage controls the output frequency of VCO. This voltage controlled oscillator output is recovered clock; it will feed back to the phase frequency detector. This PLL's negative feedback faces phase & frequency of the recovered clock to be same as the phase, bit rate, and clock condition.

GTP transceiver is a power efficient transmitter-receiver for Spartan 6 FPGA. In the physical implementation of MGTs; it takes the form of differential based electrical interface. There are three differential methods such as:

1. Current Mode logic (CML),
2. Low voltage differential signaling (LVDS) &
3. Low voltage Pseudo emitter coupled logic (LVPECL).

CML is most common and preferable for the Giga-bit link for AC or DC termination and selectable output drive. GTP provides programmable Tx_pre emphasis, linear continuous time Rx equalization. The GTP transceiver has the line rate of 3.125 Gb/s, which is implemented tested for the SMA link of 2.5 Gb/s line rate.

VI. SFP MODULE INTERFACE [6]

The Small Form factor pluggable (SFP) is compact and hot-pluggable transceiver used for both telecommunication also for data communication, Due to the small size SFP obsolesces the formerly iniquitous gigabit interface converter (GDIC).

The Spartan 6 board contains an SFP connector and cage assembly that accepts SFP module. The high-grade fiber optic cable connected between the transmitter and receiver port that is SFP_TX_P and SFP_RX_P pins.

A. Software and Hardware Resources:

1. Xilinx ISE 14.1 tool.
2. Xilinx Core Generator.
3. Xilinx LogiCORE IP Aurora 8b/10B core.
4. Xilinx Spartan 6 (SP605) hardware development board.[7]
5. SMA cable.
6. SFP transceivers. [6]
7. Optical fiber cable.

VII. RESULTS

The testing results give the transmitted and received bit pattern on the input data. The transmitted input sequence can be seen at the end of the listing table in chipscope pro analyzer tool [3] (Figure 3). Figure 4 shows the lane_up_i, channel_up_buffer signal, Aurora input sequence and the received signal.

VIII. CONCLUSION

The implemented design gives the perfect and points to point description to transfer the high-speed serial data over the higher bandwidth serial cable. The design is giving the results for Aurora 8B/10B protocol in full duplex mode. The design proposed to make a simplex transmitter and receiver link on the individual Spartan 6 board. The transmitted signal marked as x cursor at sample 0 and the input sequence can be seen at sample 22 marked by o cursor. From their onwards input sequence can receive at the receiver side.

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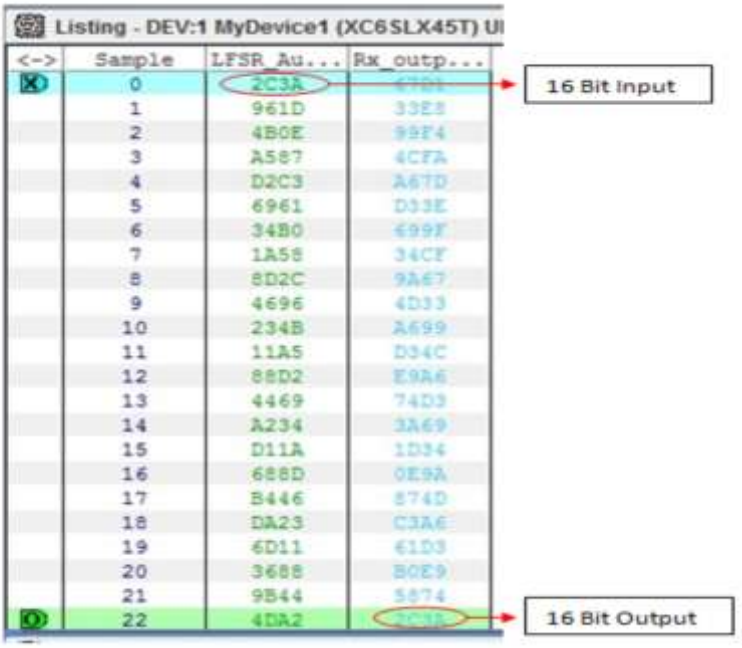

Figure.3 listing of the 16-bit input and output data sequence.

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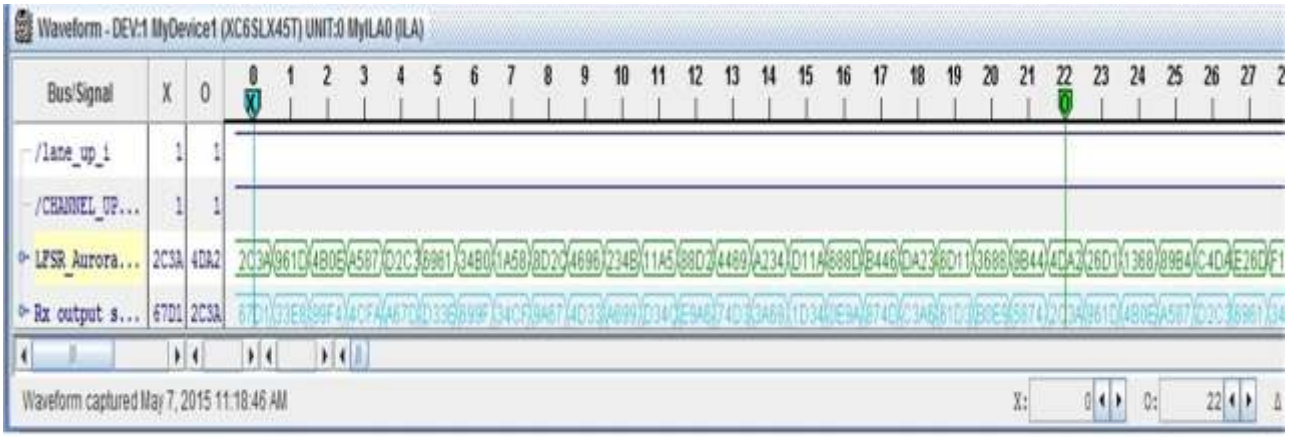

Figure.4 Sequence of Aurora input and output data