# Design Of Ternary Logic Arithmatic Circuits Using CNTFET

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***Abstract*—** This paper presents a design of ternary arithmetic circuits like half-adder, full-adder and 1-bit comparator using Carbon Nano-Tube field effect transistors. Carbon nano-tube has unique characteristics of behavior according to its arrangement of atoms. Threshold voltage of CNTFETs can vary by changing its diameter and also one intermediate state between two normal stable ON and OFF states introduced for multi-valued logic computation. Moreover ternary logic is a promising alternative to the conventional binary logic design technique, since it is possible to produce three states (FALSE, UNKNOWN, TRUE), and also reduces the number of interconnects and chip area and increases efficiency. In this paper we have proposed novel circuit design of half-adder and comparator based on ternary logic CNTFETs. Increased number of states in CNTFETs will increases the number of bit handling capacity in the device.

***Keywords-*** *Carbon Nano-Tube Field Effect Transistor (CNTFET), MVL(multi valued logic), Half-Adder, Full-adder,Comparator.*

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## I. INTRODUCTION

Traditionally, digital computation is performed on two-valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [1] or fuzzy logic [2]. Ternary logic (or three-valued logic) has attracted considerable interest due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area [3]. Furthermore, serial and serial-parallel arithmetic operations can be carried out faster if the ternary logic is employed.

There are two kinds of MVL circuits based on MOS technology, namely the current-mode MVL circuits and the voltage mode MVL circuits. Voltage-mode MVL circuits have been achieved in multi threshold CMOS design [4]. The carbon nanotube (CNT) FET (CNTFET) is a promising alternative to the bulk silicon transistor for low-power and high-performance design due to its ballistic transport and low OFF-current properties [5]–[8]. A multi threshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multi threshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs.

The design of ternary arithmetic circuits such as half adder, full adder, comparator are designed by using basic ternary logic gates because of the ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation [8].

The rest of this paper is organized as follows. Section II starts with a review of ternary logic, followed by the brief introduction of CNTFET in Section III. Then ternary arithmetic circuits is proposed, analysed, and evaluated ations in Section IV and simulation results by HSPICE in Section V, which is followed by conclusion in Section VI.

## II. REVIEW OF TERNARY LOGIC

Ternary logic functions are defined as those functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any *n* variable *{X*1, . . . , *Xn }* ternary function *f*(*X*) is defined as a logic function mapping *{*0, 1, 2*}n* to *{*0, 1, 2*}*, where *X* = *{X*1, . . . , *Xn}*. The basic operations of ternary logic can be defined as follows, where *Xi*, *Xj* = *{*0, 1, 2*}* [13]:

$$Xi + Xj = \max\{Xi, Xj\}$$

$$Xi \bullet Xj = \min\{Xi, Xj\}$$

$$\overline{Xi} = 2 - Xi \quad (1)$$

Where − denotes the arithmetic subtraction, the operations +, •, and are referred to as the OR, AND, and NOT in ternary logic, respectively. The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. The assumed logic symbols are shown in Table I. The ternary gates are designed according to the convention defined by (1).

TABLE I
LOGIC SYMBOLS

| Voltage level | Logic Value |
|---|---|
| 0 | 0 |
| ½ Vdd | 1 |
| Vdd | 2 |

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TABLE II
TRUTH TABLE OF TERNARY INVERTERS

| Input X | STI | PTI | NTI |
|---|---|---|---|
| 0 | 2 | 2 | 2 |
| 1 | 1 | 2 | 0 |
| 2 | 0 | 0 | 0 |

### A. *Ternary Inverter*

A general ternary inverter is an operator (gate) with one input *x*, and three outputs (denoted by *y*0, *y*1 , and *y*2 ) such that

$$\begin{aligned} y0 = C0(x) &= \begin{cases} 2, & if\ x = 0 \\ 0, & if\ x \neq 0 \end{cases} \\ y1 = C1(x) &= \bar{x} = 2 - x \\ y2 = C2(x) &= \begin{cases} 2, & if\ x \neq 2 \\ 0, & if\ x = 2 \end{cases} \end{aligned} \quad (2)$$

Therefore, the implementation of ternary inverter requires three inverters, and they are a negative ternary inverter (NTI), a standard ternary inverter (STI), and a positive ternary inverter (PTI), if *y*0, *y*1, and *y*2 in (2) are the outputs [3]. The truth table of the three ternary inverters is shown in Table II.

### B. *Ternary NOR and NAND Gates*

The ternary NAND and NOR are two multiple entry operators used in ternary logic. The functions of the two-entry ternary NAND and NOR gates are defined by the following two equations, respectively [1]:

$$Ynand = \overline{\min\{X1, X2\}} \quad (3)$$

$$Ynor = \overline{\max\{X1, X2\}} \quad (4)$$

The truth table of ternary NAND and NOR gates shows in Table III.

TABLE III
TRUTH TABLE OF NAND AND NOR

| Input X1 | Input X2 | YNAND | YNOR |
|---|---|---|---|
| 0 | 0 | 2 | 2 |
| 1 | 0 | 2 | 1 |
| 2 | 0 | 2 | 0 |
| 0 | 1 | 2 | 1 |
| 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 0 |
| 0 | 2 | 2 | 0 |
| 1 | 2 | 1 | 0 |
| 2 | 2 | 0 | 0 |

## III. CARBON NANOTUBE FET

CNTFETs utilize semiconducting single-wall CNTs to assemble electronic devices. A single-wall CNT (or SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n*,*m*). A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (*n*,*m*): the nanotube is metallic if $n = m$ or $n - m = 3i$, where $i$ is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following [10] [11]:

$$Dcnt = \frac{\sqrt{3}a0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (5)$$

Where $a0 = 0.142$ nm is the interatomic distance between each carbon atom and its neighbour. Fig. 1 shows the schematic diagram of CNTFET [9]–[11]. Similar to the traditional silicon device, the CNTFET also has four terminals. As shown in Fig. 1, undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state [5]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

The *I*–*V* characteristics of the CNTFET are similar to MOSFET's. The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half band gap that is an inverse function of the diameter [9]–[11], i.e.

$$Vth \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eDcnt} \quad (6)$$

Where a = 2.49 Å is the carbon to carbon atom distance, $V_\pi$ =3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and DCNT is the CNT diameter. As DCNT of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs in the channel is 0.293 V from (6). Simulation results have confirmed the correctness of this threshold voltage. As the chirality vector changes, the threshold voltage of the CNTFET will also change. Assume that *m* in the chirality vector is always zero, then the ratio of the threshold voltages of two CNTFETs with different chirality vectors is given as:

$$\frac{Vth1}{Vth2} = \frac{Dcnt2}{Dcnt1} = \frac{n2}{n1} \quad (7)$$

Equation (7) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of a CNTFET using (13, 0) CNTs is 0.428 V, compared to a (19, 0) CNTFET with a threshold voltage of 0.293 V.

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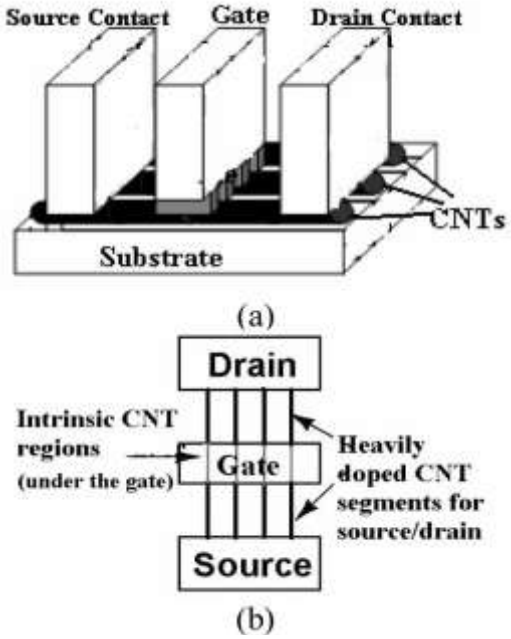


Figure 1 Basic structure of CNTFET

## IV. ARITHMETIC CIRCUITS BASED ON CNTFET

### *I. 1-Bit Comparator*

A 1-bit comparator compares two input bits which are in ternary logic and gives three outputs based on the comparison between these two three valued input signals and three outputs are: A > B, A = B, and A < B in the comparator circuits. Based on the relation between two inputs (A and B), corresponding output becomes high and others remain low. The logic block diagram and the input–output waveform of a ternary comparator is shown in Fig. 2, and (5) respectively. The truth table of the ternary logic 1-bit comparator is shown in Table IV.

### *II. Half Adder*

A ternary half adder adds two ternary inputs and gives output as ternary sum bits and carry bits. The truth table of a ternary half adder is shown in Table V. The logic function for sum and carry bit can be derived from the truth table V.

$$\text{Sum} = A_2B_0 + A_1B_1 + A_0B_2 + 1\cdot(A_1B_0 + A_0B_1 + A_2B_2)$$
$$\text{Carry} = 1\cdot(A_2B_1 + A_2B_2 + A_1B_2) \quad (8)$$

TABLE IV
TRUTH TABLE OF TERNARY 1BIT-COMPARATOR

| A | B | A < B | A = B | A > B |
|---|---|---|---|---|
| 0 | 0 | 0 | 2 | 0 |
| 0 | 1 | 2 | 0 | 0 |
| 0 | 2 | 2 | 0 | 0 |
| 1 | 0 | 0 | 0 | 2 |
| 1 | 1 | 0 | 2 | 0 |
| 1 | 2 | 2 | 0 | 0 |
| 2 | 0 | 0 | 0 | 2 |
| 2 | 1 | 0 | 0 | 2 |
| 2 | 2 | 0 | 2 | 0 |

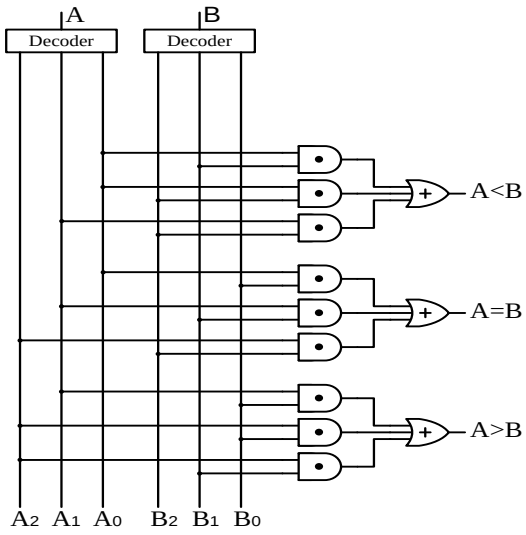


Figure 2 Ternary 1-Bit Comparator

TABLE V
TRUTH TABLE OF TERNARY HALF-ADDER

| A | B | SUM | CARRY |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 2 | 2 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 2 | 0 |
| 1 | 2 | 0 | 1 |
| 2 | 0 | 2 | 0 |
| 2 | 1 | 0 | 1 |
| 2 | 2 | 1 | 1 |

In equation (8), $A_k$ and $B_k$ are the outputs from the ternary decoder corresponding to the inputs A and B shown in Fig. 3. The schematic diagram of a ternary half adder is shown in Fig. 3 which consists of T-Decoder, two input T-AND gates, three input T-OR gates and T-Buffers.

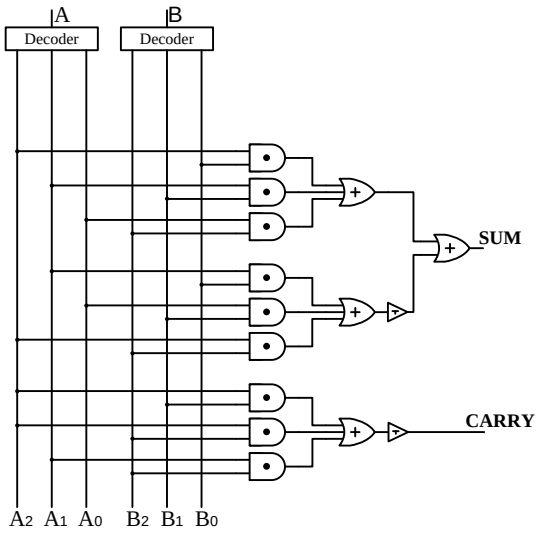


Figure 3 Ternary half-Adder

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*III. Full Adder*

A 1-bit ternary full adder adds two ternary numbers and previously calculated carry which here denoted as Cin. This circuit produces a 2-bit output sum represented by the signals Cout and SUM. A ternary full adder can be implemented by cascading two ternary half adder circuits. Fig.4 shows the ternary full adder block diagram using two ternary half adders block. Here the first half adder adds 2 input bits A and B. The following half adder adds the sum output of A and B inputs with past carry (Cin) and generates sum bit and one carry bit in its output. The final carry bit (Cout) is generated by the OR operation between the two carry bits generated from the two stages (first half adder and the second half adder). Fig. (7) shows the waveforms of the designed ternary full adder circuit. Table VI shows the truth table of the Ternary full-adder.

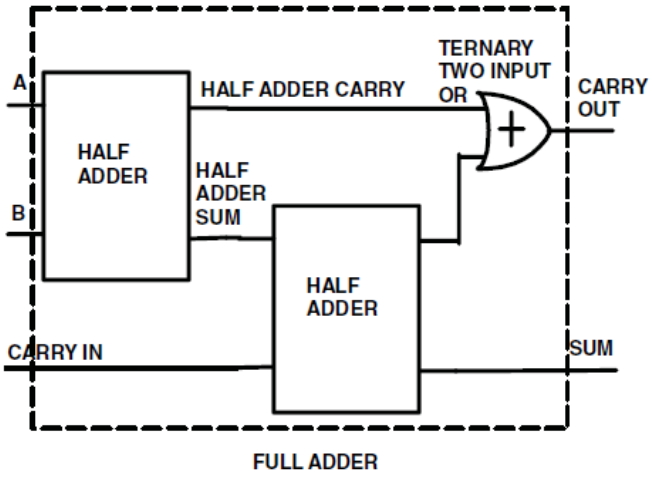


Figure 4 Ternary Full-Adder

TABLE V
TRUTH TABLE OF TERNARY FULL-ADDER

| A | B | CIN | SUM | COUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 2 | 2 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 2 | 0 |
| 0 | 1 | 2 | 0 | 1 |
| 0 | 2 | 0 | 2 | 0 |
| 0 | 2 | 1 | 0 | 1 |
| 0 | 2 | 2 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 2 | 0 |
| 1 | 0 | 2 | 0 | 1 |
| 1 | 1 | 0 | 2 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 2 | 1 | 1 |
| 1 | 2 | 0 | 0 | 1 |
| 1 | 2 | 1 | 1 | 1 |
| 1 | 2 | 2 | 2 | 1 |
| 2 | 0 | 0 | 2 | 0 |
| 2 | 0 | 1 | 0 | 1 |
| 2 | 0 | 2 | 1 | 1 |
| 2 | 1 | 0 | 0 | 1 |
| 2 | 1 | 1 | 1 | 1 |
| 2 | 1 | 2 | 2 | 1 |
| 2 | 2 | 0 | 1 | 1 |
| 2 | 2 | 1 | 2 | 1 |
| 2 | 2 | 2 | 0 | 2 |

## V. SIMULATION RESULTS

Figures (5),(6), and (7) shows the simulation results of proposed ternary Arithmetic circuits such as ternary 1-bit comparator, ternary half adder and ternary full adder using HSPICE. So from the simulated results we can say that proposed ternary arithmetic designs are working, based on CNTFET model given by Stanford university [9], and gives appropriate output.

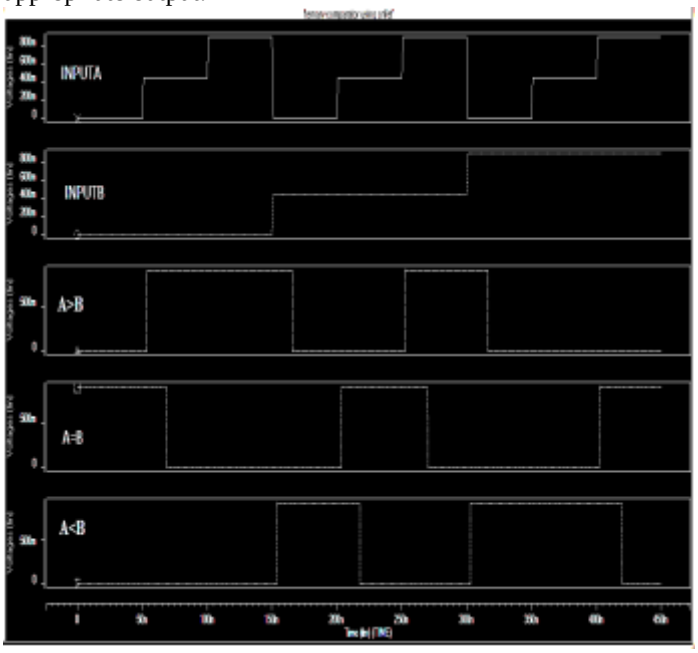


Figure 5 Simulated result of Ternary 1-bit Comparator


Figure 6 Simulated result of Ternary Half-Adder

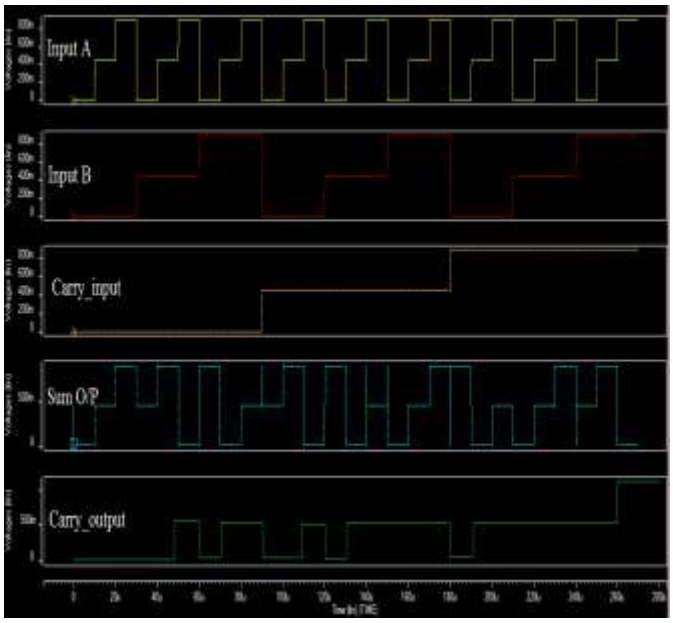

Figure 7 Simulated result of Ternary Full-Adder

## VI.CONCLUTION

This paper presented the design of ternary logic arithmetic circuits based on Carbon Nano-tube Field Effect Transistor (CNTFET). This is the future technology to the predominant CMOS Technology, the major drawback of traditional CMOS technology is scaling of its size. Less power dissipation was observed in the CNTFET-based ternary logic circuits than the CMOS technology. The threshold voltage of CNTFET is depends on its diameter, so we can easily control on threshold voltage rather than CMOS. By the above points we conclude that, CNTFET based ternary circuit design is a promising circuit element in MVL circuits in the near future.

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