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Low Power Design Bi – Directional Shift Register By using GDI Technique

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Abstract—The paper presents to design the Bi-directional shift register by taking the advantage of concept called Gate Diffusion Input Technique (G.D.I). To design Bi-Directional shift register D-Flip Flop is required. By using GDI technique the numbers of transistors were reduced so that the area required will be less and low power consumption. The simulation results were taken using the Digital Schematic tool in 120nm technology. The optimized Area and Power is calculated by using Micro Wind tool in 120 nm technology. The simulation results tells that the design is more efficient compared with the other logic techniques with less area and power consumption.

Keywords- *GDI Technique,Shift Registers, D- Flip Flop, Bi-directional shift register.*

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I. INTRODUCTION

In VLSI technology the number of transistors is reducing day to day life. By using the GDI Technique we designed the Bi-directional shift register. In GDI technique the numbers of transistors were reduced to design the bi-directional shift register with less propagation delay, low area and low power consumption. To design bi-directional shift register D- Flip Flop is required. The D- Flip Flop is also designed by using the concept called GDI technique. D-Flip Flop is used as a one bit storage memory element. Flip Flops are of two types Edge triggered flip flop and Level sensitive Flip flop. D-Flip Flop is also used to design the Sequential circuits. By using GDI technique we can also design sequential circuits with low area, less propagation delay and low power consumption.

The paper designs a very efficient implementation of Bi-directional shift register. Section 2 explains about the Gate Diffusion Input. Section 3 tells about the design of D – Flip Flop. Section 4 describes about the different types of Shift Registers. Section 5 explains about the Design of Bi – Directional Shift Register with less power consumption and less propagation delay with the power analysis table. Section 6 gives the simulation results and finally Section 7 gives you the Conclusion of the Paper.

II. GATE DIFFUSION INPUT

Gate Diffusion Input Technique is a new technique to reduce propagation delay, area and power dissipation. The best method to design low power digital combinational circuits is GDI Technique. GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating conditions.

The main feature of GDI cell is the VDD source will not connect to the source of PMOS transistor and the GND will not connect to the source of NMOS transistor. In the place of VDD and GND pins input signals are used to make more flexible than CMOS design. Figure 2 shows the Basic GDI cell.

The figure 1 explains that there are three inputs in a Basic GDI cell. G(common gate input to NMOS and PMOS), p(input to the source/drain of PMOS) and N(input to the source/drain of NMOS). Table 1 shows the different logic functions implemented with less power consumption and less propagation delay compared to other design techniques.

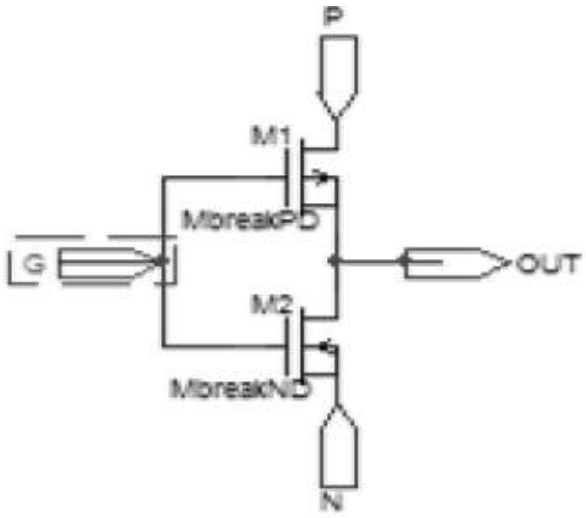

Figure- 1: Basic GDI cell

Table- 1: Logic functions of Basic GDI cell

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

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III. DESIGN OF A D – FLIP FLOP

D- Flip Flop is a one bit storage element. To design D- Flip Flop four number of NAND gates are required. By using GDI technique NAND gates are designed with less propagation delay and low power consumption. Figure 2 shows the implementation of NAND gate and Figure 3 shows the Layout design of NAND gate. Figure 16 shows the simulation result of the GDI based NAND gate.

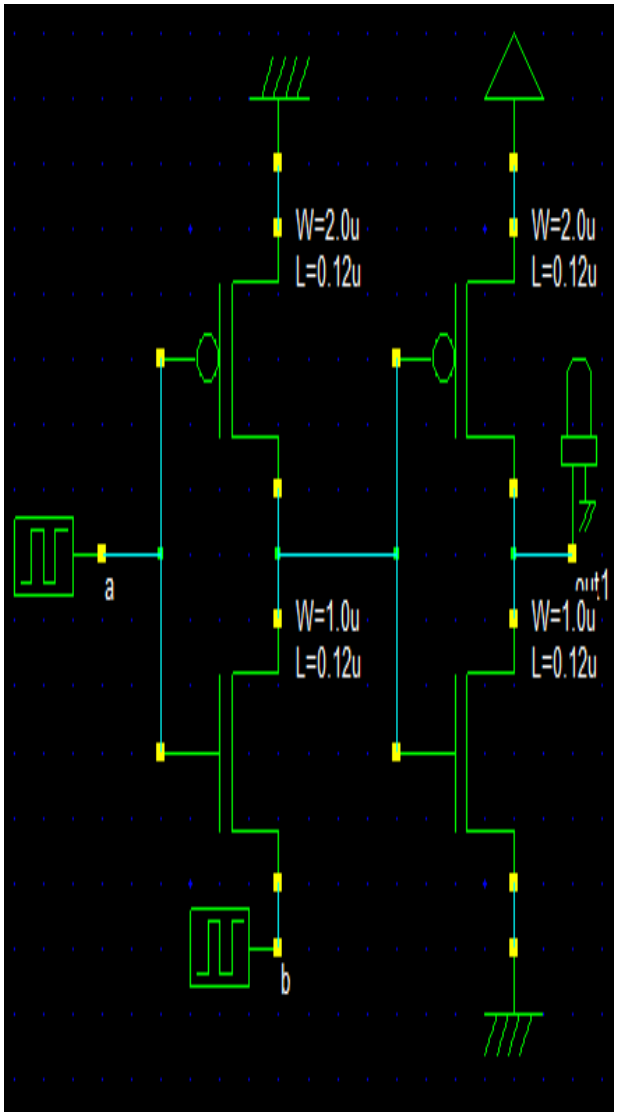

Figure- 2: GDI based NAND gate

To design D- Flip Flop four numbers of NAND gates are required. D is a one input to the first NAND gate and inverted D input is given to the second NAND gate. The output of the first NAND gate is given as input to the first NAND gate. The output of the second NAND gate is given as input to the fourth NAND gate.

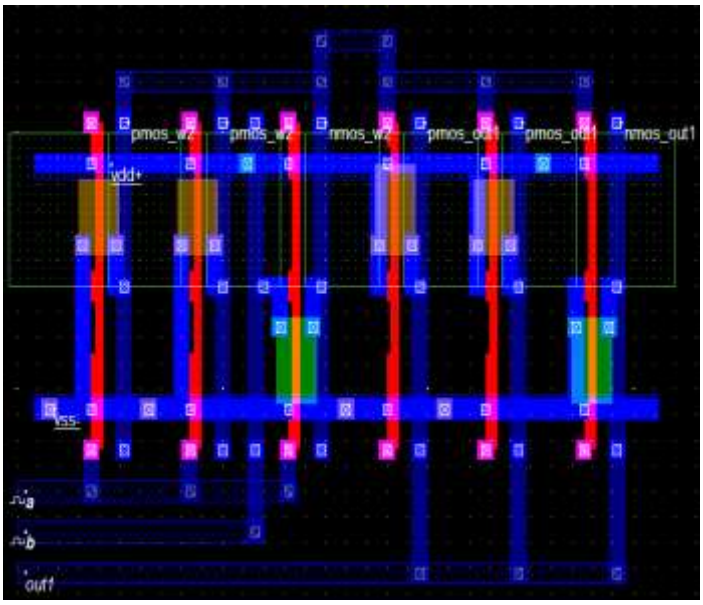

Figure- 3: Layout design of GDI based NAND gate

Common clock pulse is given to the first and second NAND gate. The output of the third NAND gate given as feedback input to the fourth NAND gate (that is q to the third NAND gate input a). The output of the fourth NAND gate given feedback as input to the third NAND gate (that is qbar to the third NAND gate input b). Figure 4 shows the implementation of the D- Flip Flop and Figure 5 shows the Layout design of the D- Flip Flop. Figure 17 shows the simulation result of D-Flip Flop.

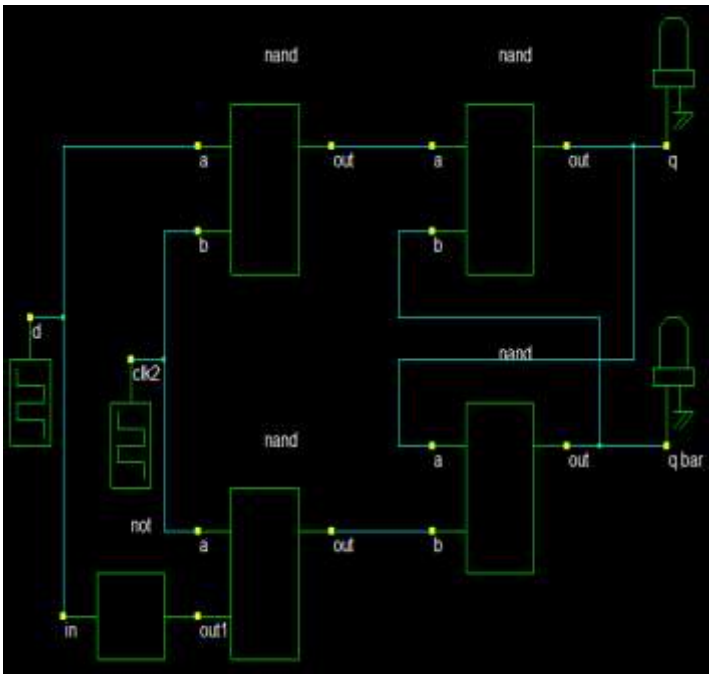

Figure- 4: GDI based D- Flip Flop

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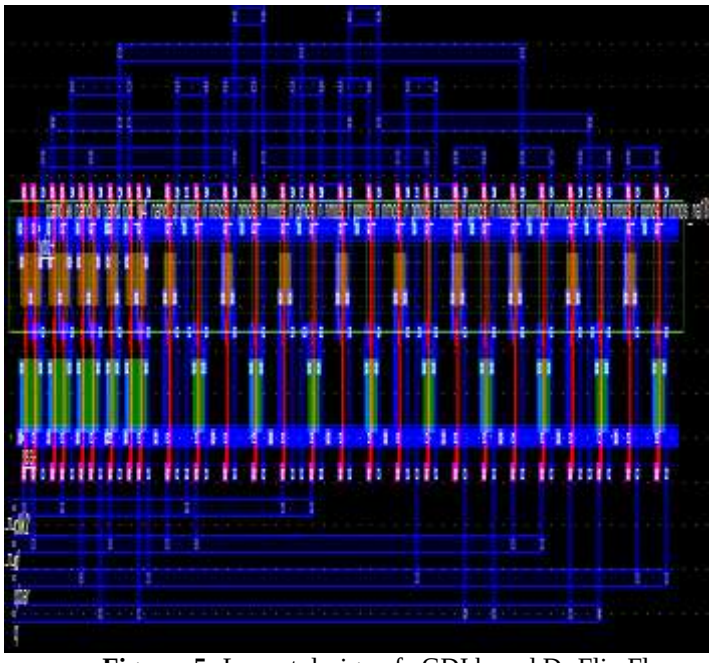

Figure- 5: Layout design of aGDI based D- Flip Flop

IV. DESIGN OF A SHIFT REGISTERS

Shift registers are also used as storage of digital data. It is also a type of sequential logic circuits. Group of D- Flip Flops connect in a chain to form a shift registers. Output of one flip flop is given input of the next flip flop. There are four types of shift registers there are. Serial in Serial out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel out. Figure 6 shows the implementation of the serial in and serial out shift register. Figure 7 shows the layout design of the serial in and serial out shift register. The simulation results for serial in and serial out is shown in figure 18.

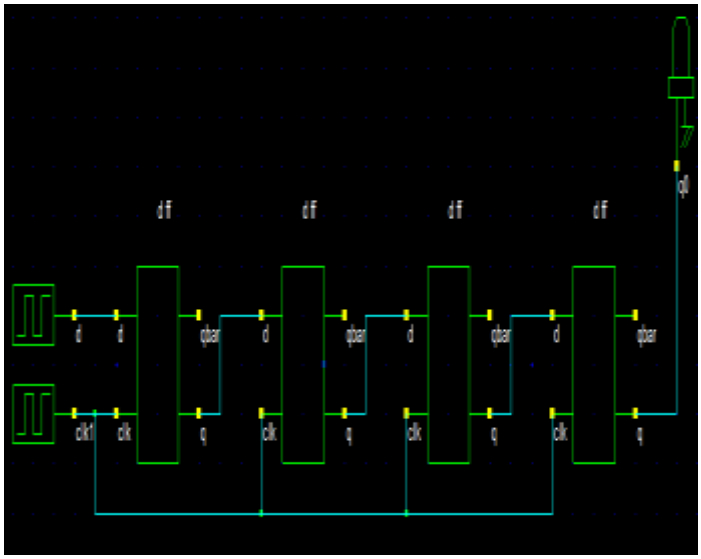

Figure- 6: GDI based Serial in Serial out shift register

Serial in Serial out explains you that the output q of one D- flip flop out is taken as input d to the next D- flip flop. Common clock pulse is given to the all four D- flip flops. Q0 is taken as the serial output after the fourth flip flop execution. Figure 8 shows the implementation of Serial in Parallel out and Figure 9 shows the Layout design of Serial in and parallel out.

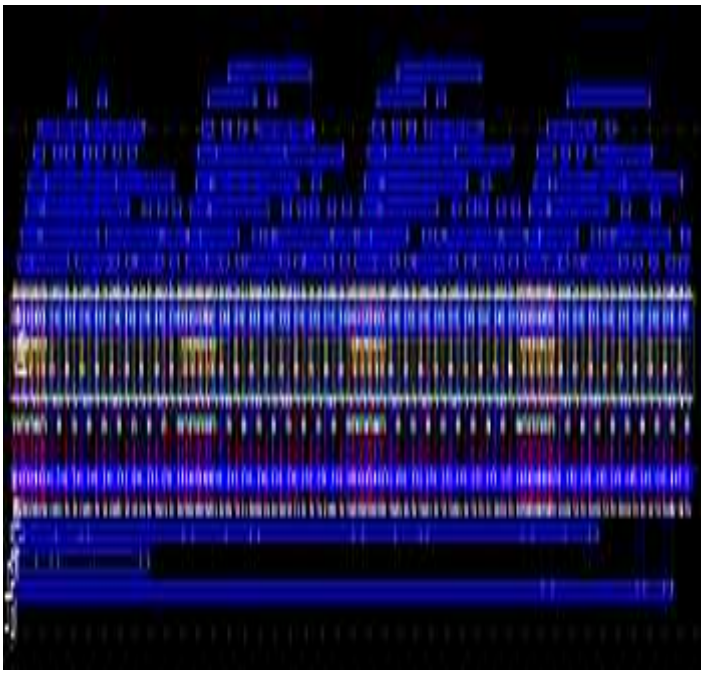

Figure- 7: Layout design of GDI based Serial in Serial out shift register

From the figure we can explain that the d input is given to the first D- flip flop and output is taken as the first parallel out q0 with respect to the first clock pulse. q0 is taken as second input to the next D-flip flop and output is taken second parallel out q1 with respect to the second clock pulse. q1 is taken as third input to the next D-flip flop and output is taken third parallel out q2 with respect to the third clock pulse. q2 is taken as fourth input to the next D-flip flop and output is taken fourth parallel out q3 with respect to the fourth clock pulse. The simulation results for serial in and parallel out is shown in figure 19.

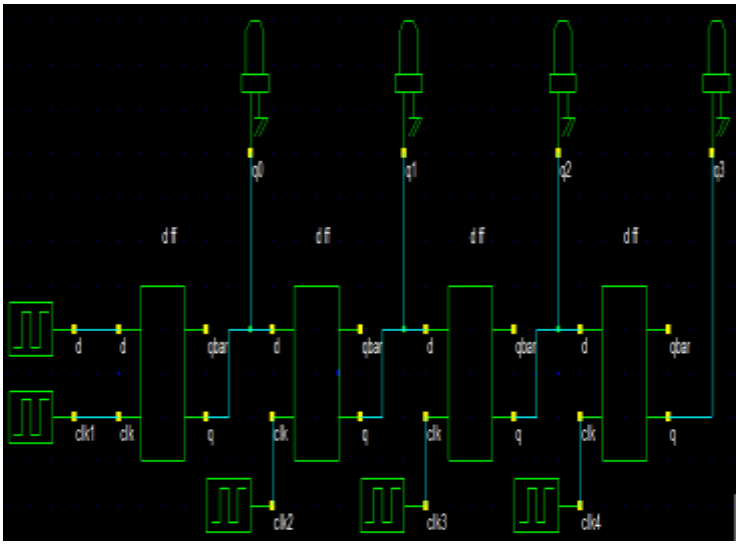

Figure- 8: GDI based Serial in Parallel out shift register

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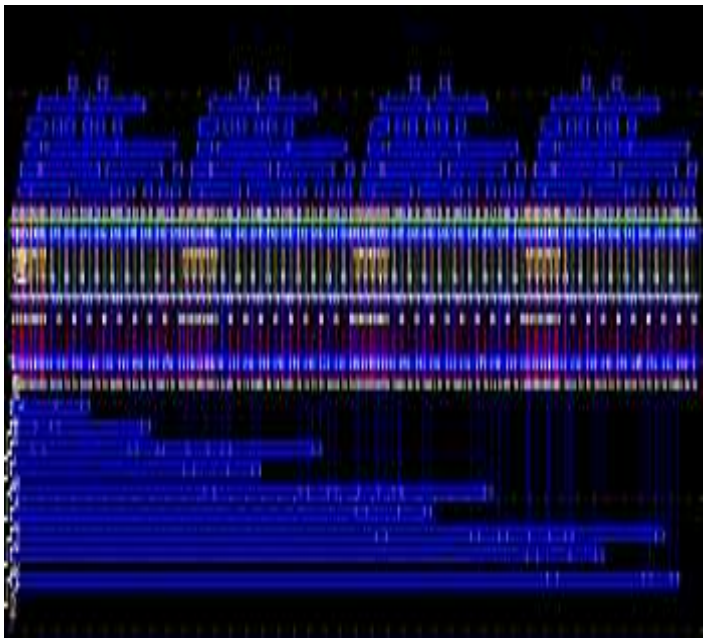

Figure- 9: Layout design ofGDI based Serial in Parallel out shift register

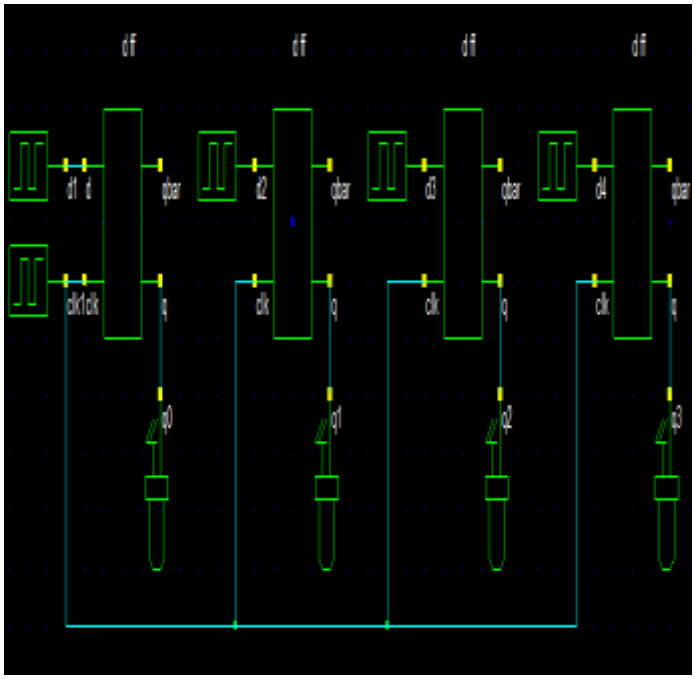

Figure- 10: GDI based Parallel in Parallel out shift register

Figure 10 shows the implementation of Parallel in and Parallel out shift register. From the figure we can explain that the first input d1 is given to the first flip flop and output taken as first parallel out q0 with respect to the first clock pulse. The second input d2 is given to the second flip flop and output taken as second parallel out q1 with respect to the second clock pulse. The third input d3 is given to the third flip flop and output taken as third parallel out q2 with respect to the third clock pulse. The fourth input d4 is given to the fourth flip flop and output taken as fourth parallel out q3 with respect to the fourth clock pulse. Figure 11 shows the Layout design of Parallel in Parallel out shift register. Figure 20 shows the simulation result of the Parallel in Parallel out shift register.

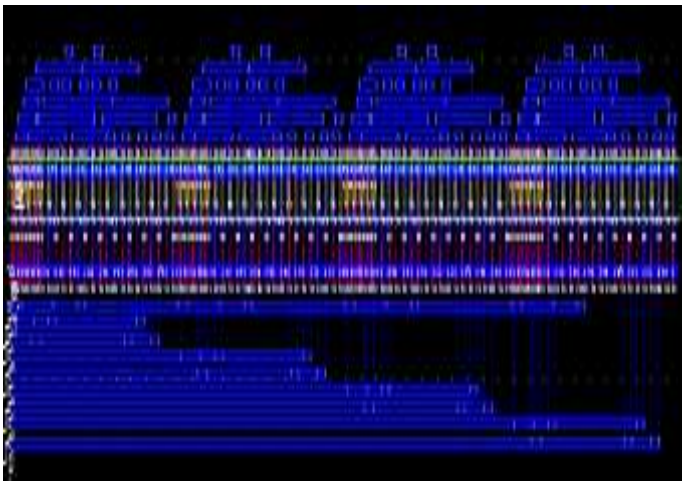

Figure- 11: Layout design of GDI based Parallel in Parallel out shift register

V. DESIGN OF A BI-DIRECTIONAL SHIFT REGISTER

The abouve shift registers shows only righ shift operations. Each right shift operation has the effect of successively dividing the binary number by two. For the left shift operation this has the effect of multiplying by two. The Bi-directional shift register has the both features of Right shift and Left shift operations. Figure 12 shows the implementation of the bi-directional shift register.

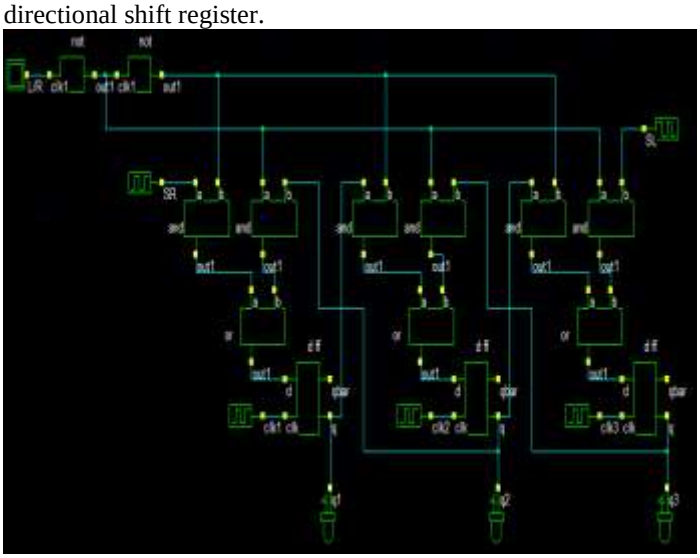

Figure- 12: Schematic design of GDI based Bi-Directional Shift Register

From the figure 13 we can explain that the complete operation of the bi-directional shift register is depending on L`/R input. If the input L`/R = 1 then the operation is Right shift operation and if the L`/R = 0 then the operation is Left shift operation. To design bi-directional shift register we require two numbers of NOT gates, six number of AND gates, three number of OR gates and three number of D-Flip Flops. SR and SL are two data inputs that need to shift the data from left to right or right to left with respect to the input L`/R. The inverted L`/R output acts as input to the, 'a' input of the '2', '4', '6' AND gate and the second inverted L`/R output acts as input to the, 'b' input of the '1', '3', '5' AND gate. The output

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of the AND1 and AND2 gives input to the OR1 gate. The output of the OR1 gate gives input to the D-Flip Flop with respect to the first clock pulse. The output of the AND3 and AND4 gives input to the OR2 gate. The output of the OR2 gate gives input to the second D-Flip Flop with respect to the second clock pulse. The output of the AND5 and AND6 gives input to the OR3 gate. The output of the OR3 gate gives input to the third D-Flip Flop with respect to the third clock pulse. The output q3 gives feedback input to the 'b' input of AND4 gate. The output q2 gives feedback input to the 'b' input of AND2 gate. The shifted outputs have taken from the output of D- Flip Flops as q0, q1, q3. By using the concept GDI technique we design bi-directional shift register with better performance and low power dissipation than the other techniques. Figure 13 shows the Layout design of GDI based Bi-directional shift register. Figure 21 shows the simulation results of the bi-directional shift register.

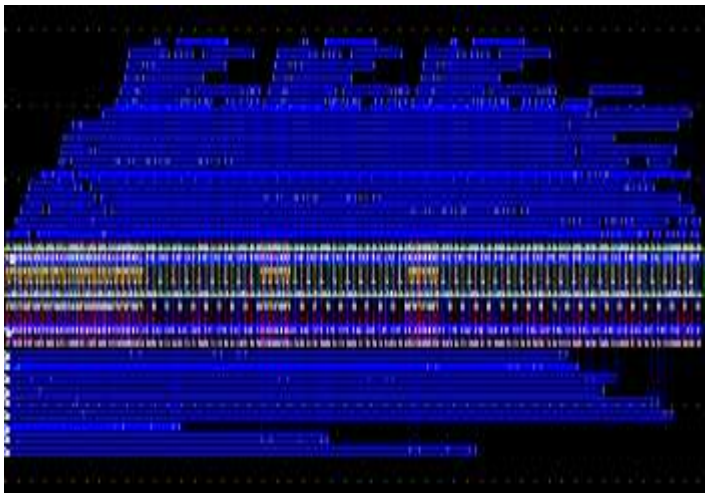

Figure-13: Layout design of GDI based Bi-directional Shift Register

VI. SIMULATION RESULTS

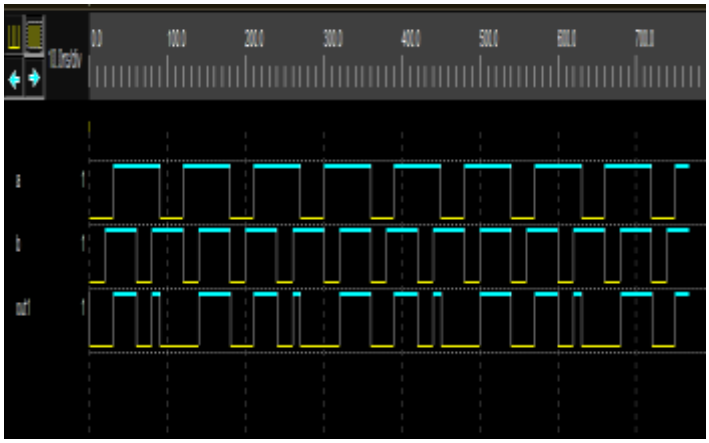

Figure- 14: Simulation result for GDI based AND gate

From the above figure we know that 'A' and 'B' are two inputs and the function output expression is A.B that is the input 'A' is multiplied with the 'B' input results 'out = A.B'. If 'A = 1' and 'B = 1' then output results 'out =1.1= 1'.

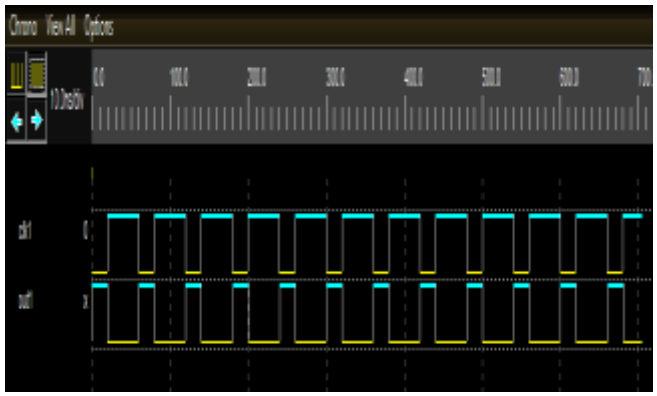

Figure- 15: Simulation result for GDI based NOT gate

From the above figure we know that 'A' is the input and the function output expression is A' that is the input 'A' is inverted and results out = A`. If A = 1 then output results 'out = A`' = 1` = 0.

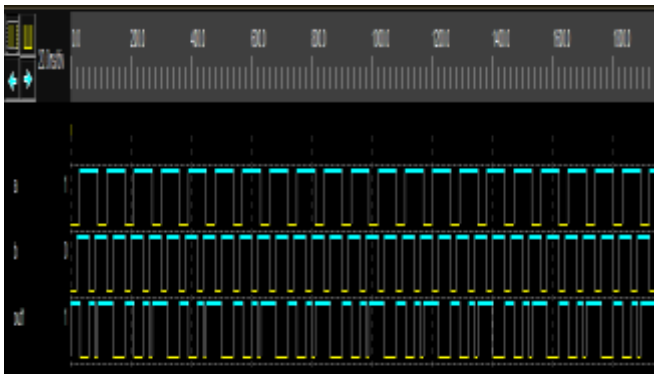

Figure- 16: Simulation result for GDI based NAND gate

From the above figure we know that 'A' and 'B' are two inputs and the function output expression is (A.B)` that is the input 'A' is multiplied with the 'B' input results out = A.B and output is inverted 'out= (A.B)`. If A = 1 and B = 0 then output results 'out = (1.0)'= 0` = '1'.

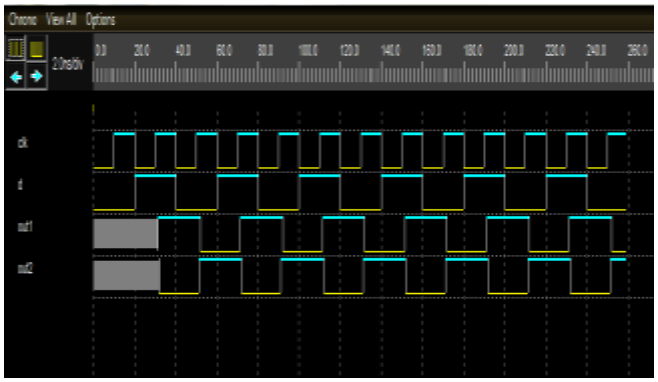

Figure- 17: Simulation result for GDI based D-Flip Flop

From the above figure we know that the D- Flip Flop is an edge triggered flip flop. For every rising edge of the clock pulse the output 'q' and 'qbar' is occurred with respect to the input'd'. If 'clk = 1' and 'd = 1' then output 'q = 1' and 'qbar = 0'. From the above figure out1 is considered as 'q' and out2 considered as 'qbar'.

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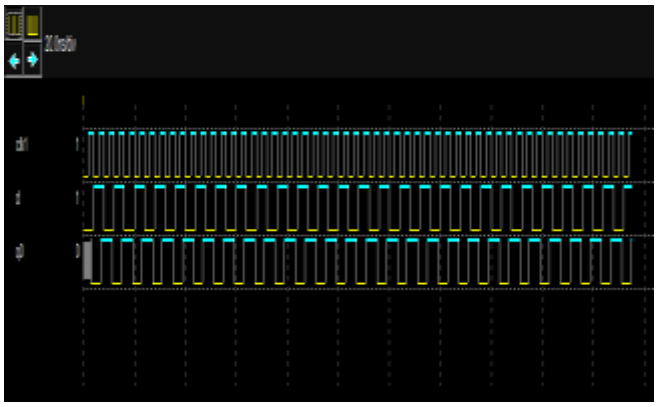

Figure- 18: Simulation result for GDI based Serial in Serial out Shift Register

From the above figure we know that the ‘d’ is inputs that given to D- flip flop serially and ‘q0’ is the output. At the output stage ‘q0’, the ‘d’ input shifts serially at rising edge of clock pulse.

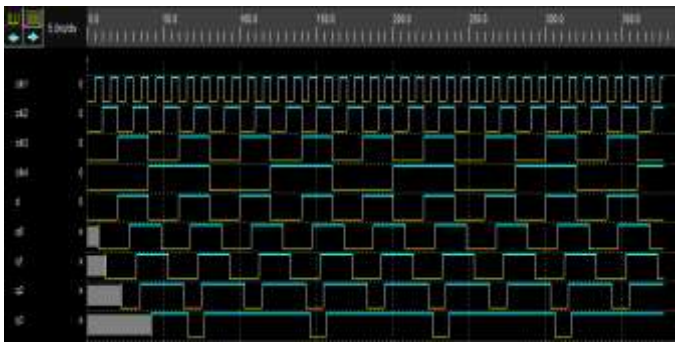

Figure- 19: Simulation result for GDI based Serial in Parallel out Shift Register

From the above figure we know that the ‘d’ is inputs that given to D- flip flop’s serially and ‘q0’, ‘q1’, ‘q2’ and ‘q3’ are the outputs. At the output stage the ‘d’ input shifts and taken as parallel out ‘q0’ and q0 is taken as input to the next flip flop that is serial input to the second D-flip flop with respect to the rising edge of second clock pulse clk2 and output is taken as parallel out ‘q1’. In the same way the remaining flip flops will be executed and taken as serial inputs and parallel outputs.

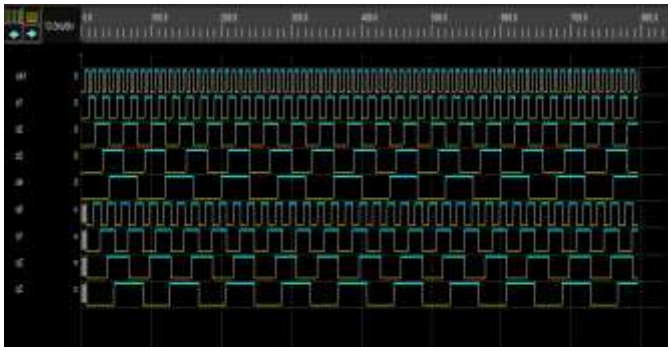

Figure- 20: Simulation result for GDI based parallel in Parallel out Shift Register

From the above figure we know that ‘d1’, ‘d2’, ‘d3’ and ‘d4’ are four parallel inputs given to four different D- flip flops with same clock pulse clk1 and outputs has taken as ‘q0’, ‘q1’, ‘q2’ and ‘q3’. The output ‘q0’ executes for the first phase clock cycle of clock1. The output ‘q1’ executes for the second phase clock cycle of clock1. The output ‘q2’ executes for the third phase clock cycle of clock1.The output ‘q3’ executes for the fourth phase clock cycle of clock1.

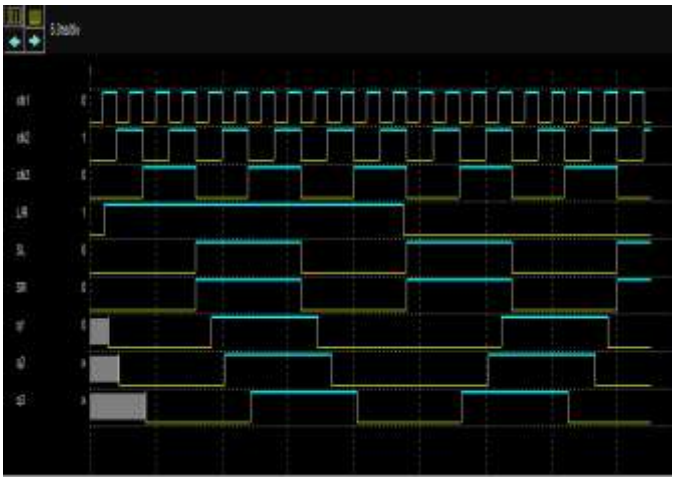

Figure- 21: Simulation result for GDI based Bi - Directional Shift Register

From the above figure we know that L`/R is the input that decides whether it is right shift or left shift. SL and SR is two data input lines that need to be shifted with respect to the clock pulses. If L`/R = 1 then the data SR is shifted right and outputs shown in ‘q1’, ‘q2’ and ‘q3’ with respect to the clock pulses. If L`/R = 0 then the data SL is shifted left and outputs shown in ‘q1’, ‘q2’ and ‘q3’ with respect to the clock pulses.

Table- 2: Power Analysis

S.No.	Design	Power(uw)
1	Design of NAND gate by using GDI technique	2.975
2	Design of D-Flip Flop by using GDI technique	8.926
3	Design of Serial in Serial out by using GDI technique	15.496
4	Design of Parallel in Serial out by using GDI technique	16.453
5	Design of Parallel in Parallel out by using GDI technique	16.627
6	Design of Bi-Directional Shift Register by using GDI technique	20.476

VII. CONCLUSION

The paper designs the Bi-directional shift register with less area, less propagation delay and low power consumption by using GDI technique. In GDI technique the number of power suppliers and ground connections are reduced so that power required to design the bi-directional shift register are very less. The numbers of transistors were reduced by using the concept called GDI technique. The power analysis was shown in table 2. To design NAND gate by using GDI technique the power required to design is 2.975uw. To design D-Flip Flop by using GDI technique the power required to design is 8.926uw. To design Serial in Serial out shift register by using GDI technique the power required to design is 15.496uw. To design Serial in Parallel out shift register by using GDI technique the power required to design is 16.453uw. To design Parallel in Parallel out shift register by using GDI technique the power required to design is 16.627uw. To design Bi-directional shift register by using GDI technique the power required to design is 20.476uw. The design gives the best performance with less propagation delay, low area and less power consumption.

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