Analysis and design implementation using VHDL and NAND circuit for Linear Feedback Shift Register (LFSR) for Low Power BIST

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***Abstract*—** This paper presents a low power Linear Feedback Shift Register (LFSR) for the Test Pattern Generation (TPG) technique which reduces power dissipation during testing. The relationship between the consecutive patterns is higher during normal mode testing. This approach uses the idea of reducing the transitions in the test pattern generated by the conventional LFSR. The change is reduced by increasing the correlation between the successive bits.

Keywords- *LFSR, Low Power, Implementation, BIST, Test Patterns*

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I. INTRODUCTION

Power dissipation is a severe problem for today's system-on-chips (SoCs) design and testing. On the whole, power dissipation of the system in test mode is a bit more in comparison to standard mode. It is because a noteworthy relationship exists between successive vectors applied during the circuit's standard mode of operation, whereas it's not always necessarily true for the used test vectors in the test mode. Low connection between the successive test vectors increases switching activity and eventually power dissipation in the circuit. The same occurs when applying low correlated patterns to the scan chains. Increasing the switching activity of scan chain can increase the power consumption in the scan chain and its combinational block. This extra power could cause problems for instance immediate power surge that can cause damage to the circuit, difficulty in performance authentication, reduction of the product yield and lifetime and formation of hot spots.

Built-In Self-Test (BIST) and scan-based BIST's have emerged as a promising answer to the VLSI testing problems. BIST is a DFT methodology that is aimed at detecting faulty components in the system by integrating the test logic on the chip.

BIST is well known due to the numerous advantages including improved testability, at-speed testing and reduced requirement of expensive external automatic test equipment (ATE). An LFSR can be used in BIST that generates a pseudorandom test pattern for the inputs, and multiple input signature registers (MISR) compacts test responses that are received from the scan chains output or primary output. Test vectors, placed on a circuit under test at nominal operating frequency, can cause more average or peak power dissipation as compared to the normal mode. The reason is random natures of the patterns that are generated by an LFSR reduce the relationship between the pseudorandom patterns and in each pattern also. This, in turn, may end in more switchings and power dissipation in test mode. [2]

II. LITERATURE CITED

By Avinash Ajane, Paul M. Furth, Rashmi Lakkur Subramanyam and Eric E. Johnson,

The authors provide a direct comparison between a fast dualistic counter, built using a classified Manchester carry chain, and a counter built by using the linear feedback shift register (LFSR). The comparison is focused on speed, power and area consumption. The authors demonstrate the use of LFSRs as an alternative to conventional binary event counters. The authors implemented 4-bit, 8-bit, 16- bit and 32-bit LFSR and binary counters in an O.5-J.lm CMOS process. [1]

By Mohammad Tehranipoor, Mehrdad Nourani and Nisar Ahmed

In this paper, the authors present a low transition test pattern generator is known as LT-LFSR, to reduce average and peak power of the circuit during test by reducing the transitions within random test pattern and between consecutive patterns. The experimental results for ISCAS'85 and '89 benchmarks, confirm up to 77% and 49% reduction in average and peak power, respectively. [2]

By Rosepreet Kaurand Nikesh Bajaj

The A5/1 is reliable algorithm, but it cryptanalysis by cryptanalysts. The authors modified concept to improve A5/1 encryption algorithm by consideration of feedback combining function of LFSRs (Linear feedback shift register) use in A5/1, and improved version of A5/1 is fast and easy to implement. [4]

By Nisha Haridas and Dr. M. Nirmala Devi

In this paper, modified genetic algorithm is used by authors to search polynomial-seed pair that produces optimum pattern for a given circuit. The experiments performed on ISCAS '85 benchmark circuits could determine a polynomial-seed pair that has fault coverage above 95% using a minimum number of vectors possible. [5]

By R. Vara Prasada Rao, N. Anjaneya Varaprasad, G. Sudhakar Babu and C. Murali Mohan4

The authors present a novel low-transition Linear Feedback Shift Register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, is known as bit-swapping LFSR (BS-LFSR),

 ISSN: 2321-8169
2030 – 2032

is composed of an LFSR and a 2 × 1 multiplexer. When used to produce test samples for scan-based built-in self-tests, it decrease the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. [6]

III. Materials and Methods

A. *BIST Architecture*

It is important to decide the proper LFSR architecture to achieve the suitable fault coverage. Every architecture requires different power even for same polynomial. Another problem connected with choosing LFSR is LFSR design issue, consisting of LFSR partitioning. The LFSR is differentiated on the first step toward the hardware cost and testing time cost. A typical BIST architecture includes a test pattern generator (TPG), generally implemented as a linear feedback shift register (LFSR), test response analyzer (TRA), implemented as multiple input shift registers (MISR) and a BIST control unit, implemented on one chip. This strategy allows applying at-speed tests and eliminates the dependence on another tester. The BIST architecture components receive below. Circuit Under Test (CUT): It is the percentage of the circuit tested in BIST mode. It is usually combinational, sequential or a memory. The Primary Input and Primary output delimit it.

a. *Multiple input signatures register (MISR):* It is made for signature analysis, which can be a way of data compression. MISR is frequently implemented in portability of alias. MISR is usually performed in BIST designs, where output responses are compressed by the MISR.
b. *Test pattern generator (TPG)*: It generates test patterns. It is a dedicated circuit or microprocessor. The patterns could be generated in pseudorandom or deterministically.
c. *BIST controller Unit (BCU):* It controls the execution of the test and manages the TPG, TRA, CUT and the multiplexer. It truly is activated by the Normal/Test signal and generates Go/No go.
d. *Test Response Analysis (TRA):* It analyses the value sequence on PO and then compares it with the expected output.

B. *Algorithm for Low Power LFSR*

As discussed in the previous section LFSR can be used to build test patterns for BIST. On this, test patterns are generated externally by LFSR that's inexpensive and high-speed. LFSR is a circuit that includes flip-flops in series. LFSR is a shift register whose output bit is a XOR function of some input bits. The initial value of LFSR is known as a seed value. LFSR's seed value has a considerable effect on energy consumption.

The output that influences the input is classified as tap. An LFSR is characterized by a polynomial, because it's referred to as a characteristic polynomial used to determine the feedback taps, which establish the length of the random pattern generation. The output of LFSR is a blend of 1's and 0's. A common clock signal is put on all flip-flops, which enables the propagation of the logical values from the input to the output of flip-flops. Increasing the relationship between bits reduces the power dissipation. This is often accomplished by adding more test vectors, while decreasing the switching activity

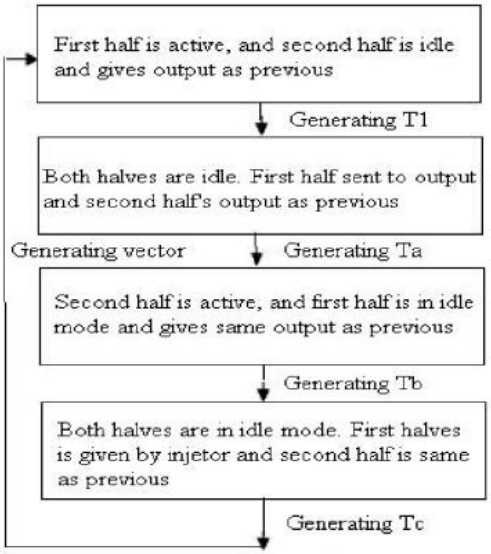


Figure 1- Algorithm for low power LFSR

LFSR is characterized by its characteristics polynomial and the inverse of these characteristics polynomial is generated polynomial. Within this approach, the three intermediate test vectors are generated by every two successive vectors (say TI, T2). The total number of signal transitions that occur between these five vectors are equal to the volume of transition occurs between the two vectors. Hence, the power consumption is reduced. Additional circuit is utilized for few logic gates as a way to generate three intermediate vectors. The three intermediate vectors (Ta, Tb, Tc) are achieved by modifying the conventional flip-flop outputs and low power outputs. The first higher level of the hierarchy from the top to the down includes logic circuit design for propagation either the present or the next state of flip-flop to second higher level hierarchy. Second level of the hierarchy is performing MUX function which is accomplished by selecting two states to propagate to the output as shown in the flow: [6]

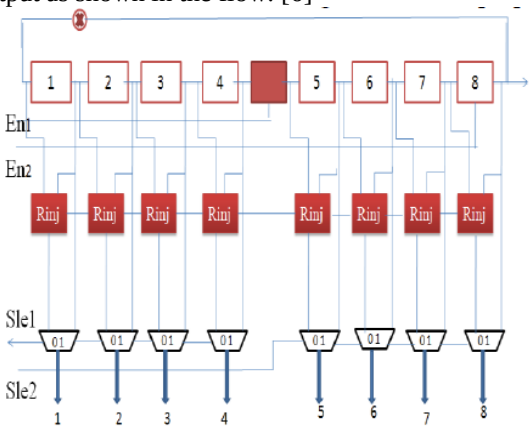


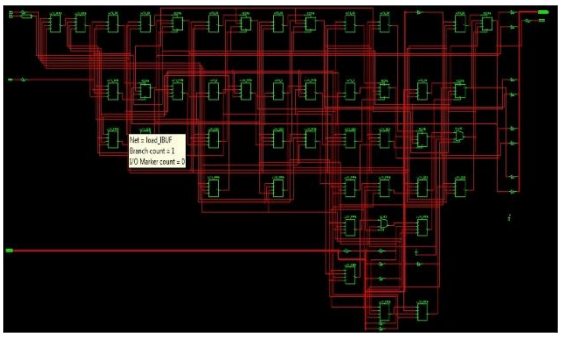
Figure 2- Low power linear feedback shift register

IV. Results and Discussion

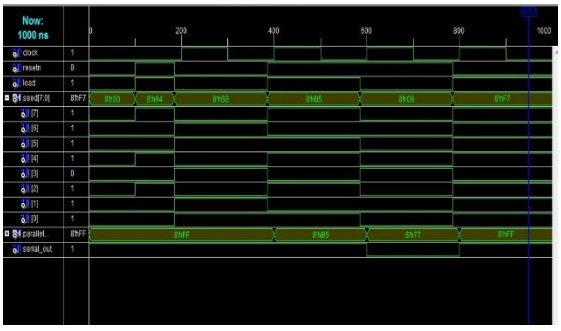
In this research work, our main aim is to design and simulate an LFSR (low power linear feedback shift register) which can reduce the power consumption while running and testing

 ISSN: 2321-8169
2030 – 2032

mode. The numbers of switching activities are also minimized for the LFSR. The comparison between the previous and implemented and simulated LFSR depends upon the relation between the bit value at the initial state and next state. Due to its power optimized characteristics, we have used it for built in self-structures to test the VLSI circuits. In this method, a single input change patterns are generated by using a counter and a gray code generator are Exclusive–ORed with the seed generated by a linear feedback shift register. The basic design of the circuit is as shown below:



Test results of the simulations confirm the assumptions that were made to decrease the power consumption of the LFSR. To get a low power computation, the LFSR counter was simulated at the faster rate than the conventional binary counter. Test results also show that as the duration of the counter increases, the maximum obtainable operating frequency of the standard counter decreases. But when we increase the duration of the cycle then it offers insignificant effect on the LFSR counter. The maximum obtainable operating frequency remains almost constant at 5.37 MHz for a power supply of 1.5 V, independent of N.



v. Conclusion

The results got from the implementation of Xilinx 9.1 with the device xc3s200-4pq208 during which, we generated simulation file after the post simulation. We now have used the simulations to calculate the power values with the cycle start and end values. The desired info is obtained per case, and comparison of power dissipation manufactured on the first step toward reports and many experts have found that total power consumed in modified LFSR is 38.3% less than the power consumed in a normal LFSR and output dynamic power is decreased by 39.6 %.

It is detected that the total power consumed in XNORed LFSR is 46% below the power consumed in a normal LFSR and output dynamic power is decreased by 52.9 %. It truly is figured that low power LFSR can be quite ideal for BIST Implementation. Low power LFSR technique can further decrease the power in BIST implementation.

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