International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 2 Issue: 5 1034 – 1037

Design of 4 bit ALU using Reversible Gates

Ravi Kant
ECE Deptt
RBIEBT, Kharar, Mohali
INDIA
ravi.kant@rayatbahra.com

Manpreet Kaur
M.Tech Research Scholar
GNE , Ludhiana
INDIA
manpreetmoney21@yahoo.com

***Abstract*—**Circuit is called as reversible if we have one to one mapping of input and output values. Reversible gates have shown promising future in low power vlsi. Their implementation using Quantum Gates further enhances their prospect for next generation VLSI applications. Authors here have successfully designed a reversible ALU which is effective in terms of number of reversible gates, garbage outputs, constant inputs, quantum cost and hardware complexity.

*****

I. II. INTRODUCTION

As digital systems are becoming faster and complex therefore the power consumption by circuits becomes the major issue. In the circuits that are not reversible, for every bit of information lost in logic computations, kT*log2 joules of heat energy is generated, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed[1]. This power dissipation can be reduced by using reversible logic. Also, Bennett[2] showed that in order to keep a circuit away from dissipating any power, it had to be composed of reversible gates. Computation that is currently carried out depends upon the number of operations that will destroy the information e.g. in AND gate there are two inputs and one output, the two inputs will be either be 1 or 0 and the output depends upon the two inputs. The output is 1 if both the inputs are 1 and the output is 0 if either of the input is 0 or both inputs are 0. Every time when the gate's output is 0 we lose information, because we do not know that the input lines are in which of the three possible states (0 and 1, 1 and 0, or 0 and 0). In fact, any logic gate that has more input lines than the output lines inevitably discards information, because we cannot deduce the input from the output.

Reversible circuits are those circuits in which we can derive the output from input and input from output. Reversible logic has received great attention in the recent years because they have ability to reduce the power dissipation which is the main requirement in low power VLSI design. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. Quantum computers are constructed using reversible logic circuits. Traditional gates such as AND, OR and XOR are not reversible gates. Out of the traditional set of gates, NOT gate is the only reversible gate. The synthesis of reversible logic differs significantly from traditional irreversible logic synthesis approaches. Fan-outs and loops are not allowed due to the target technology. There are six important parameters for determining the complexity of the circuit. These are:

- Gate count – that defines the number of reversible gates used in the circuit.
- Garbage output – that defines the outputs that are not used for further computations.
- Quantum cost – that defines the number of 1x1 or 2x2 gates that are used in the circuit.
- Logical calculation - Related to hardware complexity representing the number of NOT and two input XOR and AND gates required to implement the logic of circuit.
- Quantum depth- that defines the quantum cost of the longest path from input to output.
- Constant inputs – that defines the inputs which are to be maintained constant at 1 or 0 throughout the circuit operation depending upon the function required from the gate or circuit.

An ALU is very important part of a computer. It is basically considered as the heart of a computer. It allows the computer to add, subtract, multiply, divide and perform many other arithmetic and logic functions. Since every computer needs to be able to do these functions, they are always included in a CPU. A simple ALU consists of two operands, one control signal to select the operation to be performed and one output signal to give the result of desired operation. Reversible ALU is designed for modular arithmetic operations apart from logical operations[3]. In this paper, we will perform the logical functions such as AND, OR, XOR and arithemetic function ADD.

The rest of the paper is structured as follows-Section II contains the overview of reversible gates. Section III decribes the proposed design of ALU. Section IV is implementation Section V describes the results and discussion part followed up by conclusion in section VI.

 ISSN: 2321-8169
1034 – 1037

III. OVERVIEW OF REVERSIBLE GATES

A. NOT Gate

NOT gate is the only conventional gate that is reversible. It has one input and one output which is the basic requirement of reversible logic. NOT gate is a 1*1 reversible gate. It has a zero Quantum Cost. NOT gate is shown as follows in Fig.1. In 1*1 NOT gate there is one input i.e. A and there is one output i.e. P which is inverse of A that means if the value of A is 0 then output P is 1 and if A is 1 then P is equal to 0.

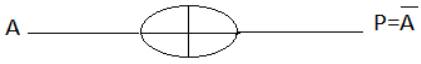

Fig. 1. NOT gate

B. Feynman gate (CNOT GATE)

Feynman gate is a 2*2 reversible gate as shown in Fig. 2[4]. It is a reversible version of the XOR gate and also called as Controlled NOT gate. It can be defined by preserving one of the inputs. Since it is a 2x2 gate, it has a quantum costof 1.

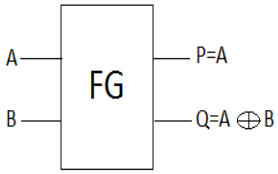

Fig. 2. Feynman or CNOT gate

C. Toffoli Gate

Toffoli gate is a 3*3 reversible gate as shown in Fig. 3[5]. Its two outputs i.e. P and Q are same as two inputs A and B and third output R is equal to A.B xor C. Toffoli gate is considered as universal gate as it is the fundamental gate to be used to realize any 3x3 gate. The quantum cost of toffoli gate is 5.

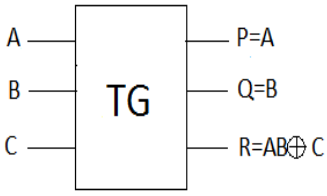

Fig. 3.Toffoli gate

D. Peres Gate

Peres gate is a 3*3 reversible gate as shown in Fig. 4[6]. One of its output P remains same as input A. Second output Q is equal to A xor B and third output R is equal to A.B xor C. Among the 3x3 reversible gates, it has the minimum quantum cost of 4.

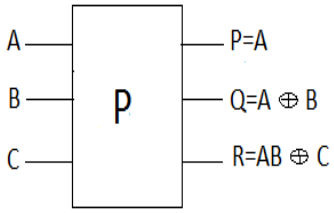

Fig. 4. Peres gate

E. Fredkin Gate

Fredkin gate is a 3*3 reversible gate as shown in Fig. 5[7]. In this the input A is obtained as first output. Inputs B and C are swapped to get the second and third outputs, which is controlled by A. If A = 0, then the outputs are simply duplicates of the inputs otherwise, if A = 1, then the two input lines (B and C) are swapped. The quantum cost of Fredkin gate is 5.

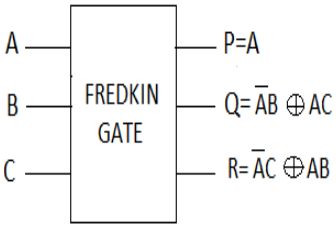

Fig. 5. Fredkin gate

III. PREVIOUS WORK

So far, large work has been done in order to implement reversible circuits. ALU is basically the brain of computer, so if we implement reversible ALU then we can save the energy to greater extent because reversible circuits consumes lesser energy as given by Landauer's principle[1]. This section first details about the implementation of reversible 1 bit ALU using reversible gates such as toffoli gate and fredkin gate which is effective in terms of number of reversible gates, number of garbage outputs, number of constant inputs, quantum cost and hardware complexity. Second section focus on the design of reversible 4 bit ALU using the same logic with which we have designed 1 bit ALU.

IV IMPLEMENTATION

A. Implementation of Reversible 1 Bit ALU

Fig. 6 shows the reversible 1 bit ALU which consists of two inputs A and B, two control lines C and D to select the operations to be performed, one output P and three garbage outputs Q, R and S. In this reversible ALU, four operations

 ISSN: 2321-8169
1034 – 1037

AND, OR, XOR and ADD are performed depending upon the value of control lines C and D. When CD = '00' then AND operation is performed, when CD = '01' then OR operation is performed, when CD = '10' then XOR operation is performed and when CD='11' then ADD operation is performed. P gives the output depending upon the operation performed and Q, R and S are the garbage outputs used to make the circuit reversible. Fig. 7 details the proposed architecture of reversible 1 bit ALU using two toffoli gates and five fredkin gates which are reversible in nature.

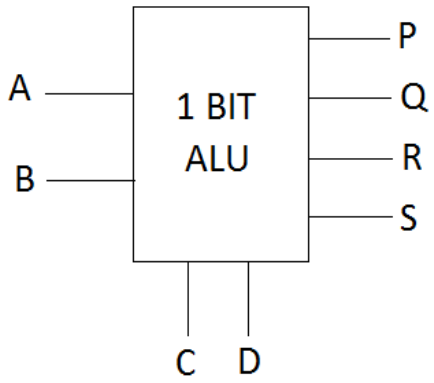

Fig. 6: Reversible 1Bit ALU

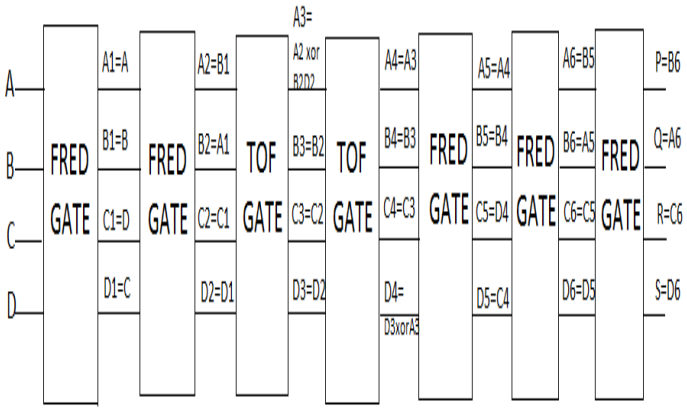

Fig. 7: Circuit of reversible 1 bit ALU

B. Implementation of Reversible 4 Bit ALU

In the reversible 4 bit ALU, 13 inputs and 13 outputs are used in which we have four constant inputs - I_1, I_2, I_3, I_4 , nine inputs- A, B, C, D, E, F, G, H, I, eight outputs – O_1, O_2, O_3, O_4, O_5, O_6, O_7, O_8 and five garbage outputs – G_1, G_2, G_3, G_4, G_5 as shown in Fig. 8. 4 bit ALU is implemented in the same manner as that of 1 bit ALU.

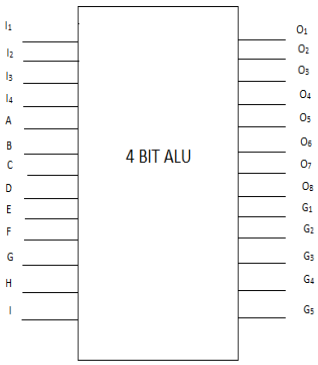

Fig. 8: Reversible 4 Bit ALU

V. RESULTS AND DISCUSSION

The implementation of design is done on Ubuntu 12.04 (LTS) / Relos tool which simulates and synthesizes the reversible logic circuit based on positive-polarity Reed-Muller expressions [11]. Simulation results of reversible 1 bit ALU are shown as follows in Fig. 9. Simulation results of reversible 4 bit ALU are shown as follows in Fig. 10.

```
ReLoS> write_netlist newalu.net

ReLoS> simulate newalu.input

Input = 0001  Output = 0001
Input = 0010  Output = 0010
Input = 0100  Output = 0100
Input = 0101  Output = 1000
Input = 0110  Output = 1001
Input = 0111  Output = 1010
Input = 1000  Output = 0101
Input = 1001  Output = 1011
Input = 1010  Output = 1100
Input = 1011  Output = 1101
Input = 1100  Output = 1110
Input = 1101  Output = 1111
Input = 1110  Output = 0110
ReLoS> print_stats

I/O: 4    # PPRM terms: 35    # Gates: 7
          Cost: 31
```

Fig. 9: Simulation Results of Reversible 1 Bit ALU

```
ReLoS> write_netlist alu4bitperes.net

ReLoS> simulate alu4bit.input

:

:

:

:

ReLoS> print_stats

I/O: 13   # PPRM terms: 29          # Gates: 20
          Cost: 68
```

Fig. 10: Simulation Results of Reversible 4 Bit ALU

Table 1 shows the reversible 1 bit ALU comparison of proposed design with the previously designed ALU using different implementing methods and synthesis tools. Comparison is made in terms of number of real and constant inputs, number of gates used, number of operations performed and the quantum cost of the circuit. In the designed 1 bit ALU, number of real inputs are 4 and constant inputs is 0 that is lesser as compared to the previous 1 bit ALU. Designed 1 bit ALU uses 7 gates and having cost of 31 that is lesser as compared to the previously designed reversible 1 bit ALU.

Table I : ALU Comparison With Earlier Results

	Constant inputs	**Garbage outputs**	**Gate Count**	**Cost**	**Operations Performed**
1 bit ALU design as in [8]	5	6	9	34	4(AND, OR, XOR, ADD)
Proposed 1 bit ALU	0	3	7	31	4(AND, OR, XOR, ADD)

VI. CONCLUSION

Reversible 1 bit ALU is designed successfully using fredkin and toffoli gates having lesser cost as compared to previous results. Similarly reversible 4 bit ALU is designed successfully using toffoli gates. Such circuits can be helpful not in terms of hardware complexity and power saving but also help in reducing cost. Any number of operations can be performed using these ALU's. More complex ALU's can be implemented using the methodology followed in the above ALU's.

REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computing process", IBM J. Research and Development, 5(3), 1961, pp: 183-191.

[2] C. H. Bennett, "Logical reversibility of computation", IBM J. Research and Development, 17, November1973, pp:525 – 532.

[3] M. K. Thomson, Robert Gluck and Holger Bock Axelsen, "Reversible Arithmetic Logic Unit for Quantum arithmetic", Journal of Physics A:Mathematical and Theoritical. 43 (2010).

[4] Feynman, R. (1985), "Quantum mechanical computers", Optical News, vol. 11, pp. 11-20.

[5] Toffoli, T. (1980), "Reversible computing", Technical Memo MIT/LCS/TM-151, MIT Laboratory for Computer Science (February).

[6] Peres, A. (1985), "Reversible logic and quantum computers", Physical Reviews. A, 32: 1985, pp: 3266-3276.

[7] Fredkin, E. and Toffoli, T. (1980),"Conservative Logic," International Journal of Theoretical Physics, vol. 21, pp 219-53.

[8] Syamala, Y. and Tilak, A.V.N. (2011),"Reversible Arithmetic Logic Unit", IEEE 978-1-4244-8679-3/11.

[9] Morrison, Matthew and Ranganathan, Nagarajan (2011), "Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures" , IEEE Computer Society Annual Symposium on VLSI.

[10] Dixit, Akanksha and Kapse, Vinod (2012), " Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6.

[11] Gupta, P.; Agrawal, A. and Jha, N. K. (2006), "An Algorithm for Synthesis of Reversible Logic Circuits," IEEE Trans. CAD, vol. 25, 11, pp. 2317–2330.

[12] A. Agrawal and N. K. Jha (2004), "Synthesis of Reversible Logic," Proceedings of Design Automation & Test, Europe, vol. 2, pp. 1384–1385.

[13] Trent and L.Robert (1952), "A Transistor Reversible Binary Counter", Proceedings of the Institute of Radio Engineering (I.R.E.),vol.40, 11, pp. 1562- 1572.

[14] H.Thapliyal and A.P.Vinod (2006), "Transistor Realization of Reversible TSG Gate and Reversible Adder Architecture", Proceedings of Asia Pacific Conference on Circuits and Systems (APCCAS), Singapore, pp. 418-421.

[15] D.P.Vasudevan; P.K.Lala; J.Di and J.P.Parkerson (2006), *"Reversible-Logic Design with Online Testability"*, IEEE Transactions on Instrumentation and Measurement, vol. 55, 2, pp. 406-414.

[16] R.Wille; D.Große; D.M.Miller and R.Drechsler (2009), *"Equivalence Checking of Reversible Circuits"*, Proceedings of 39th International Symposium on Multiple-Valued Logic (ISMVL), Naha, Okinawa, Japan, pp. 324-330.