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Design of High Speed Comparator

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***Abstract*—** A new CMOS dynamic comparator using dual input single output differential amplifier as latch stage suitable for high speed analog-to-digital converters with High Speed, low power dissipation and immune to. Back-to-back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The circuit is simulated with 1V DC supply voltage and 250 MHz clock frequency. The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a lower power dissipation, higher speed, less area, and it is shown to be very robust against transistor mismatch, noise immunity.

Keywords- *CMOS, dynamic comparator, differential amplifier, Cadence.*

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I. INTRODUCTION

Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator are shown in fig 1, this comparator can be thought of as a decision making circuit.

Nowadays high speed devices like High speed ADCs, operational amplifiers became of great importance. And for these high speed applications, a major thrust is given towards low power methodologies. Minimization in power consumption in these devices can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non idealities will greatly affect the overall performance of the device. Now analog-to-digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs. Dynamic comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration.

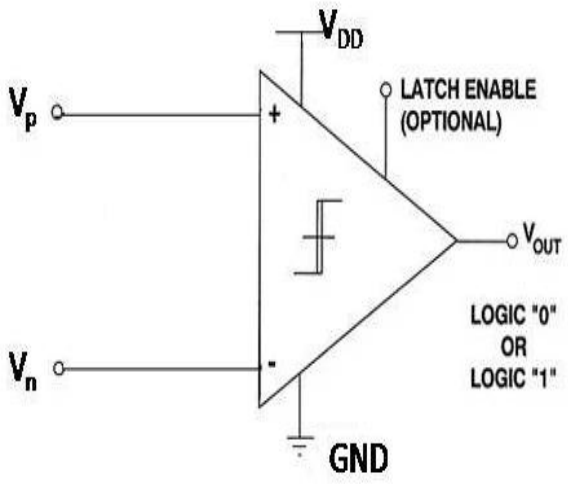

Figure 1. Voltage Comparator

It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [8]. However, the preamplifier based comparators suffer large static power consumption as

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well as from the reduced intrinsic gain with a reduction of the drain-to-source resistance rds due to the continuous technology scaling [7].

II. ANALYSIS OF COMPARATOR

Double-tail dual-rail dynamic latched comparator

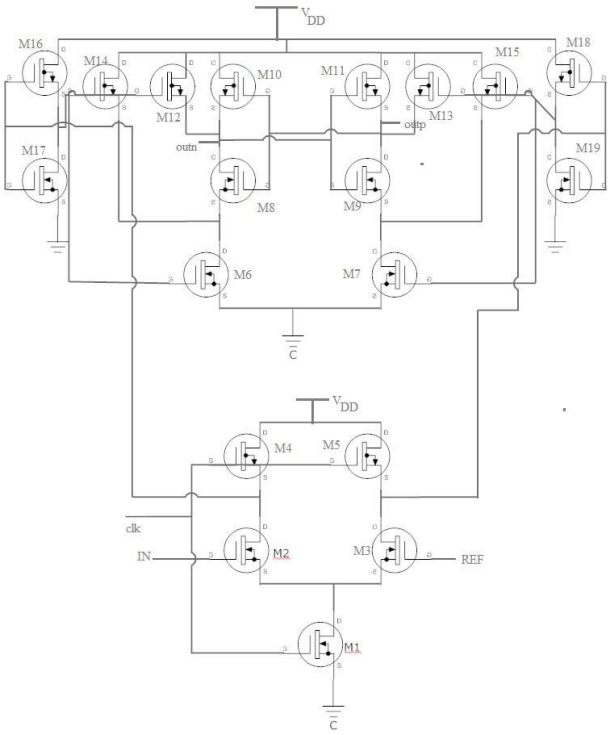

Figure 2. Double-Tail Dual-Rail Dynamic Comparator

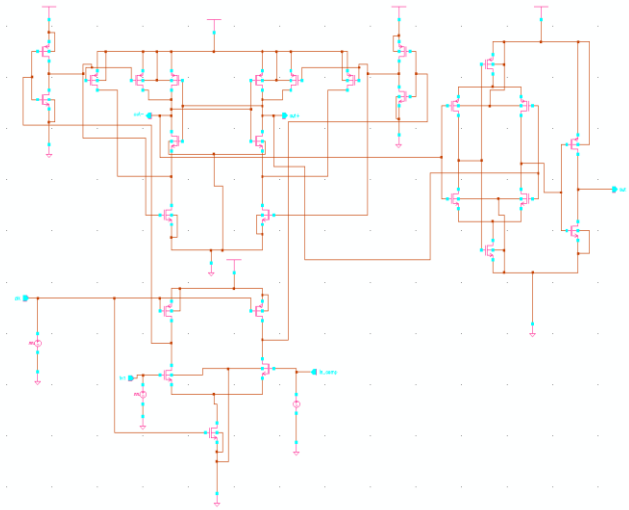

Figure 3. Double-Tail Dual-Rail Dynamic Comparator Schematic

Figure 3 shows the schematic diagram of the Dynamic Comparator without Calibration (designed in Cadence). This circuit also comprises of latch stage followed by buffer stage.

DC Characteristics

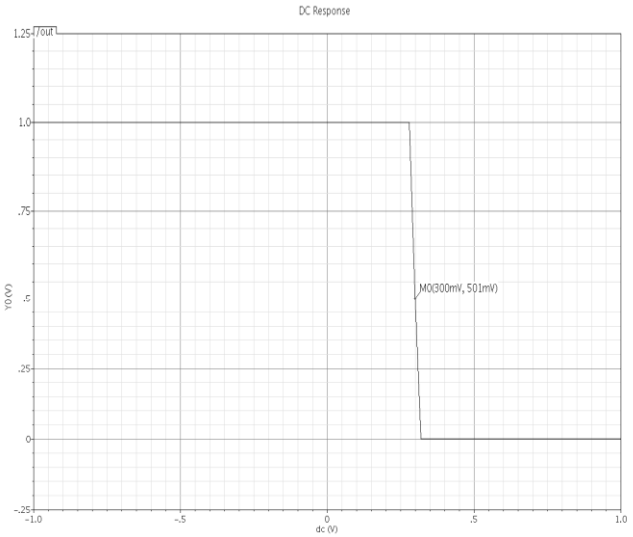

Figure 4. DC Characteristics of the Comparator.

Figure 4 shows the DC response of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as .4V. From the graph we can conclude that the comparator is working fine.

Transient Analysis

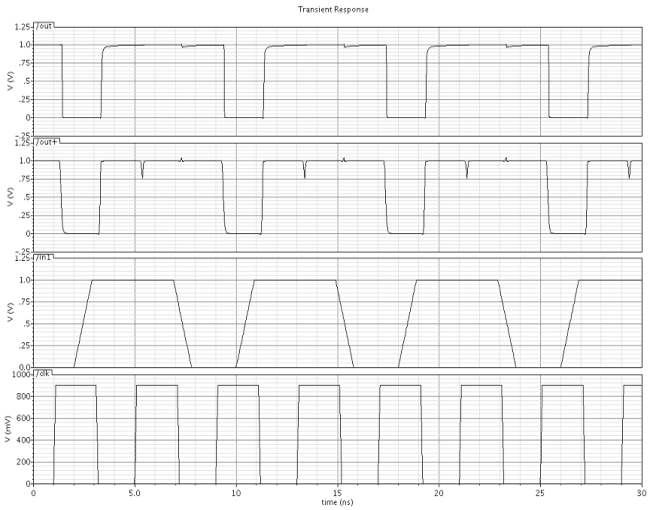

Figure 5. Transient Response of the Comparator

Figure 5 shows the transient analysis of the circuit. From this analysis we can say that the output of *out+* node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

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Results:

Before Layout Simulation:
Dynamic Power Dissipation: 57.37 µW
Delay: 1.49 nS
Speed: .671 GHz
Slew Rate: 10.77 V/nS

After Post Layout Simulation:
Dynamic Power Dissipation: 65 µW
Delay: 2.15 nS
Speed: .460 GHz
Slew Rate: 11.07 V/nS

PROPOSED COMPARATOR

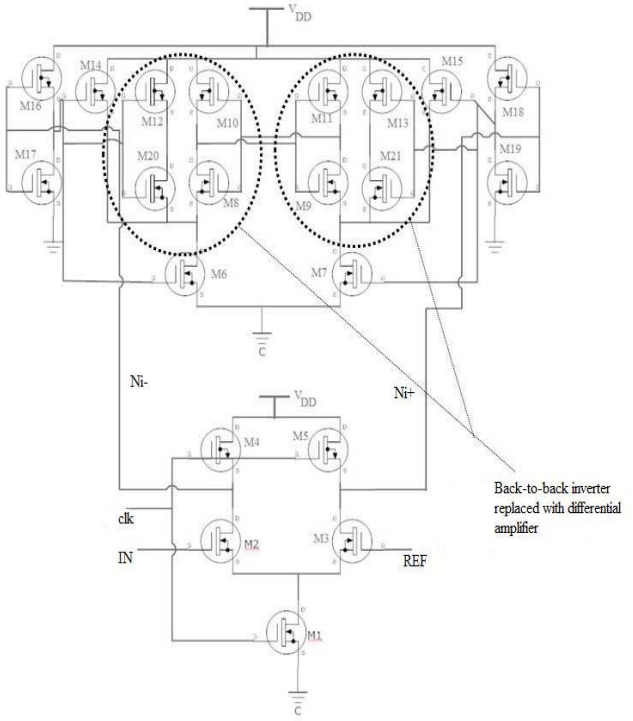

Figure 6. Proposed Comparator

Figure 6 shows the schematic of the proposed comparator. The back-to-back latch stage is replaced with back-to-back dual input single output differential amplifier. Differential amplifier has so many advantages over the conventional latch which nothing but an inverter. It has higher immunity to environmental noise and it rejects common mode noise or in other words it has better CMRR. Another property of differential signaling is the increase in maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Here our main purpose is to eliminating the noise that is present in the latch stage and for which output is getting fluctuated with clock transition.

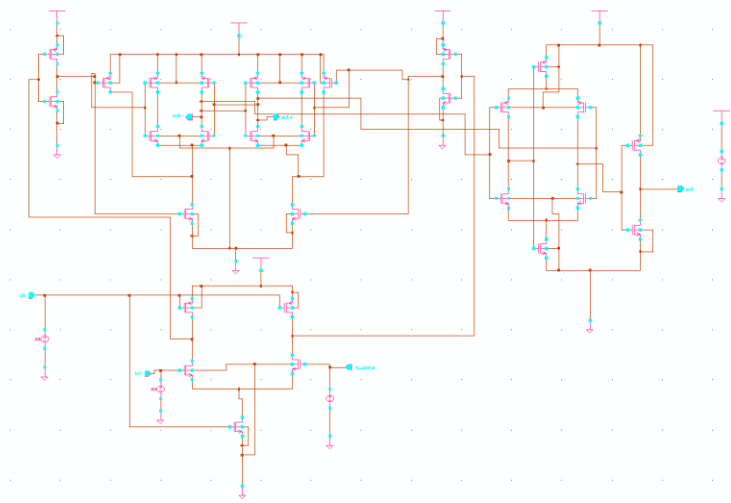

Figure 7 Schematic of the proposed comparator.

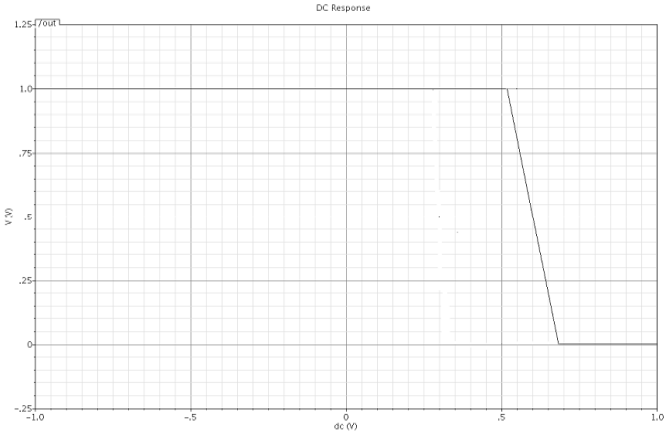

Figure 8 DC Response of the proposed comparator

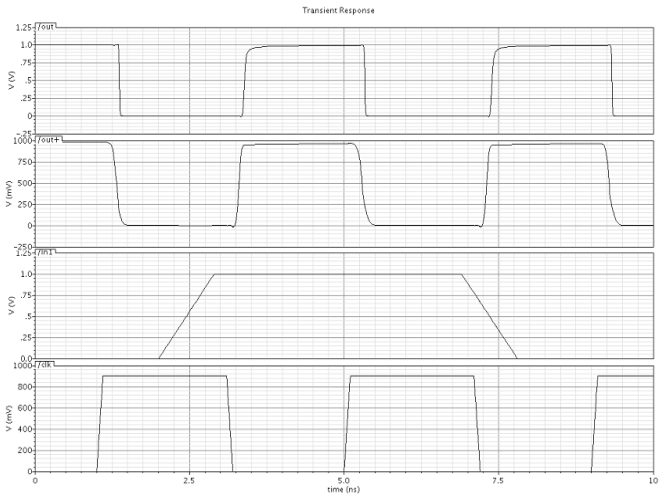

Figure 9 Transient Response of the proposed comparator

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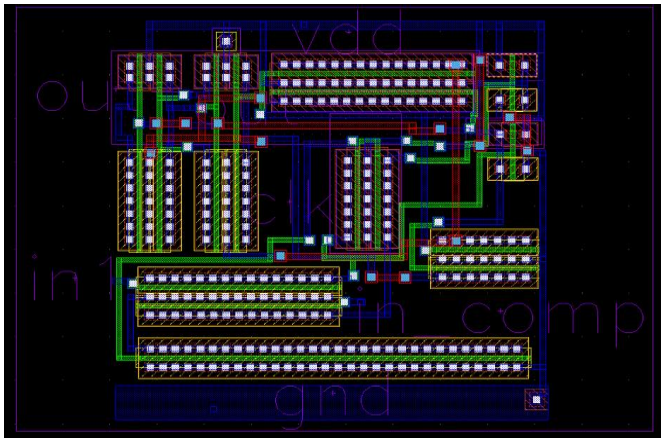

Figure 10 Layout of the proposed comparator

III. RESULTS DISCUSSIONS

TABLE I. Results before Layout Simulation

COMPARATORS	Transistor Count	Offset Voltage (mV)	Power Dissipation (µW)	Delay (nS)	Speed (GHz)	Slew Rate (V/nS)
Double Tail Dual Rail Dynamic Latched Comp.	27	300	57.37	1.49	0.671	10.77
Proposed Comparator	**29**	**300**	**44**	**1.1**	**0.910**	**10.26**

TABLE II. Result after Post Layout Simulation

COMPARATORS	Power Dissipation (µW)	Delay (nS)	Speed (GHz)	Slew Rate (V/nS)	Area (μm^2)
Double Tail Dual Rail Dynamic Latched Comp	65	2.15	0.460	11.07	110.24
Proposed Comparator	**58.25**	**2.06**	**0.485**	**8.95**	**130.42**

IV. CONCLUSION

A new dynamic comparator using positive feedback which shows better noise response, higher speed, lower power dissipation than the conventional dynamic latched comparators has been proposed & targeted for ADC application. The results are simulated in Cadence® Virtuoso Analog Design Environment with UMC 180nm technology. In the proposed design, the back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. Output of the latch stage in the proposed design is not affected by noise. The noise present in the input and the clock is completely suppressed by the differential amplifiers present in the output latch stage. The proposed structure shows significantly lower power dissipation, higher speed.

REFERENCES

[1] M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in Proc. A-SSCC, pp.269-272, Nov. 2008.

[2] H.J. Jeon, Y.B. Kim, "A Low-offset High-speed Double-tail Dual-rail Dynamic Latched Comparator," ACM GLSVLSI'10(Great Lakes Symposium on VLSI),May 16-18, 2010

[3] Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd ed.,Oxford Indian Edition, 2006.

[4] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.

[5] Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 53, no.12, pp. 1398-1402, Dec. 2006

[6] Pedro M.Figueiredo, Joao C.Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparator", IEEE Transactions on Circuits and Systems, vol.53,no.7, pp.541-545, July 2006.

[7] B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.

[8] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS- Circuit Design, Layout,And Simulation", IEEE Press Series on Microelectronic Systems, IEEE Press,Prentice Hall of India Private Limited, Eastern Economy Edition,2002

[9] Meena Panchore, R.S. Gamad, "Low Power High Speed CMOS Comparator Design Using .18µm Technology", International Journal of Electronic Engineering Research, Vol.2, No.1, pp.71-77, 2010.

[10] M. van Elzakker, A.J.M. van Tuijl, P.F.J. Geraedts, D. Schinkel, E.A.M.Klumperink and B. Nauta, "A 1.9W 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," ISSCC Dig. Tech. Papers, pp. 244–245, February 2008.

[11] S. Kale and R. S. Gamad, "Design of a CMOS Comparator for Low Power and High Speed" , Internationl Journal of Electronic Engineering Research, vol. 2, no.1, pp. 29-34, 2010.

[12] Heungjun Jeon and Yong-Bin Kim, "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator", IEEE, 2010.

[13] Razavi Behzad, "Design of Analog CMOS Integrated Circuits", New York, NY:McGraw-Hill, Inc., 2000

[14] Sansen Willy M.C., Analog Design Essentials", Neatherlands, Springer International Edition, 2006.

[15] Johns D., Martin K., Analog Integrated Circuit Design, Wiley India Pvt. Ltd., 2008.