A Low-Power and High-Speed Frequency Multiplier for DLL-Based Clock Generator

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***Abstract*—**A low-power and high-speed frequency multiplier for a delay-locked loop-based clock generator is proposed to generate a multiplied clock with different range of frequencies. The modified edge combiner consumes low power and achieves a high-speed operation. The proposed frequency multiplier overcomes a deterministic jitter problem by reducing the delay difference between positive- and negative-edge generation paths. The proposed frequency multiplier is implemented in a 0.13-µm CMOS process technology achieved power consumption to a frequency ratio of 2.9 µW/MHz, and has the multiplication ratios of 16, and an output range of 100 MHz–3.3 GHz.

I*ndex Terms*—*Clock generator, delay-locked loop (DLL), edge combiner, frequency multiplier*.

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I. INTRODUCTION

DYNAMIC voltage and frequency scaling (DVFS) is currently being used in nearly every system-on- chip (SoC), because DVFS can efficiently lower the dynamic power consumption of the SoCs while maintaining the performance [1]-[4]. The clock generator is generally implemented using a phase-locked loop (PLL) to easily change the output clock frequency. Since the DLL has advantages over the PLL due to its easiness of design, stable operation, and no jitter accumulation, the DLL based clock generator has been widely researched [10]-[14]. However, PLL have been several weaknesses such as

the difficulty of design, high-cost loop filter, and jitter accumulation Delay-locked loops (DLLs) are a good substitute for PLLs, because they resolve the PLL weaknesses. Therefore, a DLL alone cannot be used as a clock generator. The DLL-based clock generator is composed of a DLL core and a frequency multiplier, and the frequency multiplier is generally divided into two blocks: 1) a pulse generator and 2) an edge combiner. If variable frequency multiplication is required, a multiplication-ratio control logic is added. The pulse generator generates the appropriate number of pulses from the multiphase clocks, and the edge combiner generates a multiplied clock. In general, the maximum multiplication ratio of the frequency multiplier is half of the number of multiphase clocks. Because the frequency multiplier generates the multiplied clock by simply collecting the multiphase clocks, jitter accumulation does not occur. In addition, the frequency multiplier can easily change multiplication ratios. The proposed DLL based clock generator improves the lock speed without degrading the loop stability by utilizing a dual edge triggered phase detector (DET-PD) [12]-[14]. To solve the problems of the previous frequency multiplier, a novel frequency multiplier is proposed in this paper. A hierarchical structure and an overlap canceller are used for the proposed edge combiner. Owing to the proposed edge combiner, the proposed frequency multiplier can generate a wider frequency and higher frequency range multiplied clock with a lower power consumption per frequency ratio than previous frequency multipliers. The previous structures and problems of the previous frequency multipliers are presented in Section II. The structure and the operation of the proposed frequency multiplier are presented in Section III. Design and simulation results of proposed frequency multiplier are presented in Section IV. The measurement results are presented in Section V. Finally, the conclusion is drawn in Section VI.

II. ARCHITECTURE OF PREVIOUS FREQUENCY MULTIPLIERS

Fig. 1 shows the structures of the recently published frequency multipliers that perform better than most previous frequency multipliers [6]–[8]. The frequency multiplier in [6] is composed of a D-flip–flop-based pulse generator, a multiplication-ratio control logic, and a push–pull-stage based edge combiner, as shown in Fig. 1(a). Owing to its simple edge-combiner structure, this frequency multiplier is

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Suitable for high-frequency multiplied clock generation with low power and a small area. It can also guarantee a 50% duty cycle for its multiplied clock. However, because the output pulses of the pulse generator are generated consecutively [i.e., the *k*th pulse is generated directly following the $(k-1)^{th}$

pulse], the pulses might overlap owing to process variation or layout mismatch as they pass through the multiplication-ratio control logic; this could cause a short-circuit current to flow in the edge combiner, which in turn could lead to excessive power consumption or malfunction of the frequency multiplier. In addition, the output loading of the edge combiner rapidly increases with the multiplication ratio, because one pull-up pMOS (PU-P) and one pull-down nMOS (PD-N) are added to the output of the edge combiner whenever the maximum multiplication ratio increases by one.

Fig. 1(b) shows the structure of the frequency multiplier in [7]. This frequency multiplier is composed of multiplication-ratio control logic, an AND-gate-based pulse generator, and a differential cascade voltage switch (SW) logic (DCVSL)-stage-based edge combiner. The frequency multiplier can generate the multiplied differential clocks with a small area penalty. As only one PD-N is added to each differential output of the edge combiner when the maximum multiplication ratio is increased by one, the output loading of the edge combiner increases slower than that of the edge combiner in [6]. However, the PD-N should remain on till the positive and the negative edges of the multiplied differential clocks are generated by the edge combiner.

In addition, when the PD-N is turned ON, the edge combiner uses a small-sized PU-P to prevent conflict between the PU-P and the PD-N. Because of these restrictions, the frequency multiplier in [7] may not be suitable for high-speed operation and cannot guarantee 50% duty cycle for the multiplied clock. Finally, interphase timing distortion may occur when the multiphase clocks pass through the multiplication-ratio control logic, which in turn can generate pulse overlapping similar to that experienced in the frequency multiplier in [6]. The frequency multiplier in [8] has the same structure as in [7], with the exception that its edge combiner is composed of a modified DCVSL stage and a push–pull stage, as shown in Fig. 1(c). The modified DCVSL stage has SWs that turn the PU-P OFF when the PD-N is ON, preventing conflict between the PU-P and the PD-N.

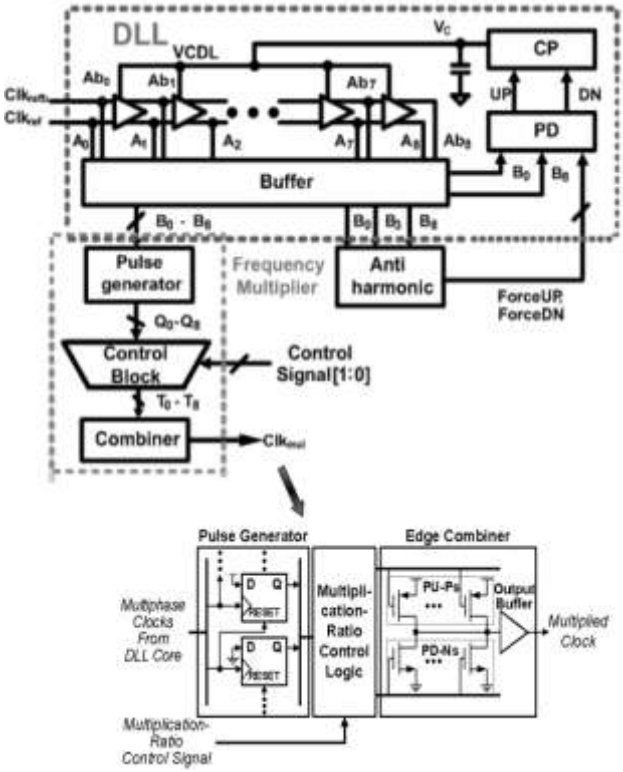

Fig. 1(a) Structure of the DLL-based frequency multiplier.[11].

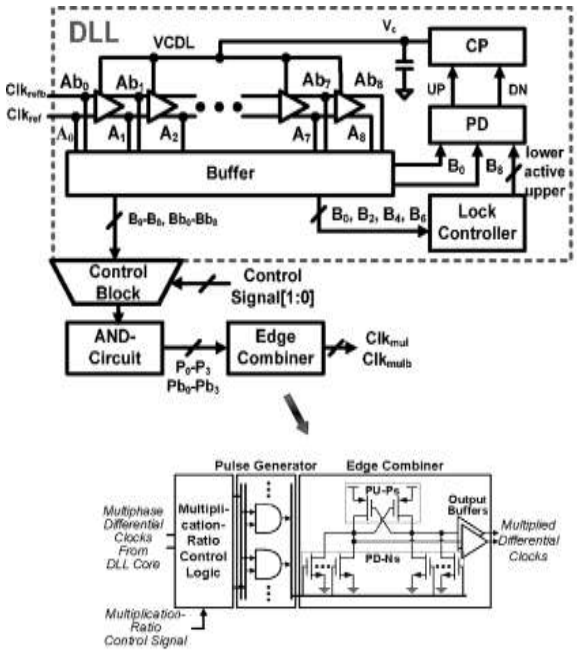

Fig. 1(b) Structure of the DLL-based frequency multiplier.[4]

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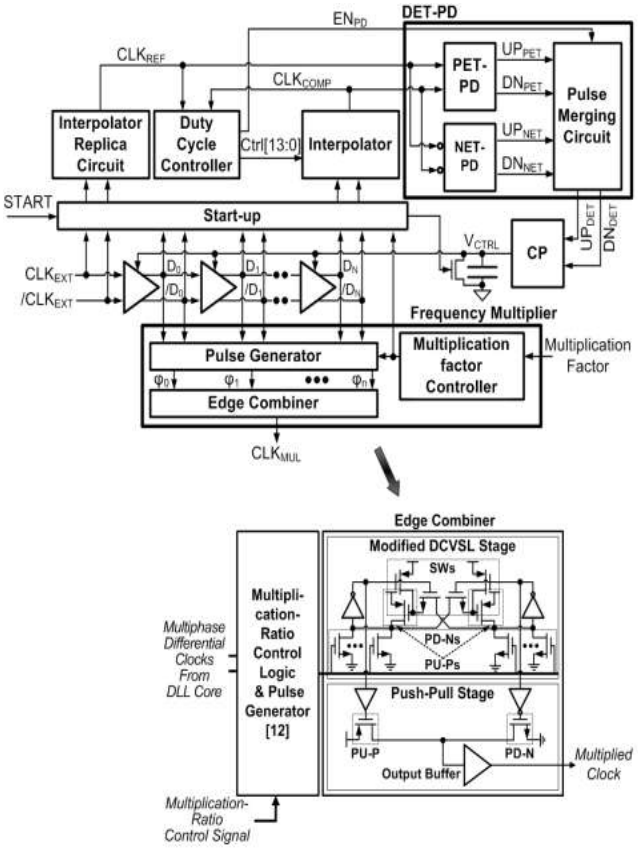

Fig. 1(c) Structure of the DLL-based frequency multiplier.[13]

Therefore, a small-sized PU-P is no longer required; this property efficiently solves the slow operation problem of the DCVSL-stage-based edge combiner in [7]. In addition, by adopting a push–pull stage, 50% duty cycle can be guaranteed for the multiplied clock. Finally, as the modified DCVSL stage maintains the characteristics of a DCVSL structure, only one PD-N is added to each differential output of the modified DCVSL stage when the maximum multiplication ratio is increased by one, as in the edge combiner in [7]. However, the frequency multiplier in [8] still has some problems in common with the frequency multiplier in [6] and [7], including reliability degradation owing to pulse overlapping.

III. PROPOSED FREQUENCY MULTIPLIER

The proposed DLL-based clock generator is composed of a DLL core and the proposed frequency multiplier, as shown in Fig. 2. To enhance the lock time, which is an important design parameter in the clock generator, a dual-edge-triggered phase- detector-based DLL core [9] is adopted. Similar to previous frequency multipliers, the proposed frequency multiplier is also composed of a pulse generator, a multiplication-ratio control logic, and an edge combiner.

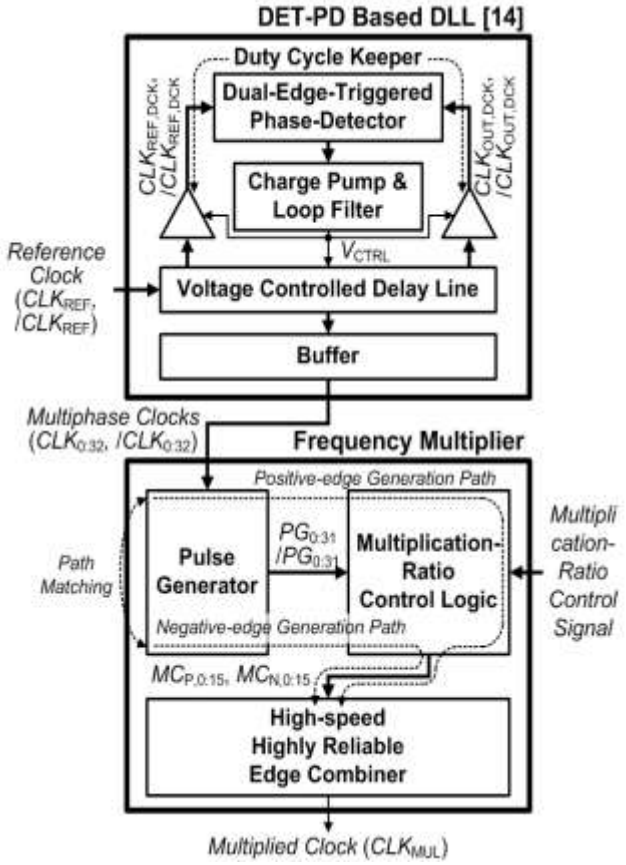

Fig.2 Structure of the proposed DLL-based frequency multiplier.

Fig. 3 shows the operations of the DLL in [9] and the proposed frequency multiplier. The dual-edge-triggered phase-detector compares both the positive and the negative edges of CLKREF,DCK and CLKOUT,DCK, which are the duty cycle recovered clocks of CLKREF and CLKOUT using the duty-cycle keeper. The DLL is locked within 300 cycles in all

process–voltage–temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks (CLK0:32 and /CLK0:32*)*. Using the 32-phase differential clocks, the pulse generator makes pulses (PG0:31 and /PG0:31*)* for positive- and negative-edge generation. The multiplication-ratio control logic selects appropriate pulses from PG0:31 and /PG0:31 and generates MC*P*,0:15 and MC*N*,0:15 according to the multiplication- ratio control signal. Finally, the high-speed and highly reliable edge combiner (HSHR-EC) generates one multiplied clock (CLKMUL*)* using all the outputs of the multiplication ratio control logic. Since the number of multiphase is 32, the maximum multiplication ratio is 16. To solve the speed and the reliability issues of previous edge combiners, an HSHR-EC, which consists of a precombining stage, overlap canceller, and push–pull stage, as shown in Fig. 4, is proposed. The two-step edge combiner, precombining, and push–pull stage are used to enhance the maximum

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multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier. Fig. 5 shows the operation of the HSHR-EC. As the number of signals merged in the precombining stage (*N*PRE*)* increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of *N*PRE. It might appear that, by increasing *N*PRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the precombing stage are equal to log2*N*PRE and 32(1–1/*N*PRE*)*, respectively, a large *N*PRE causes the precombining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter. Thus, *N*PRE is limited to two, which corresponds to a logic depth of one in the HSHR-EC, and thus, the precombining stage can be simply realized using NAND and NOR gates.

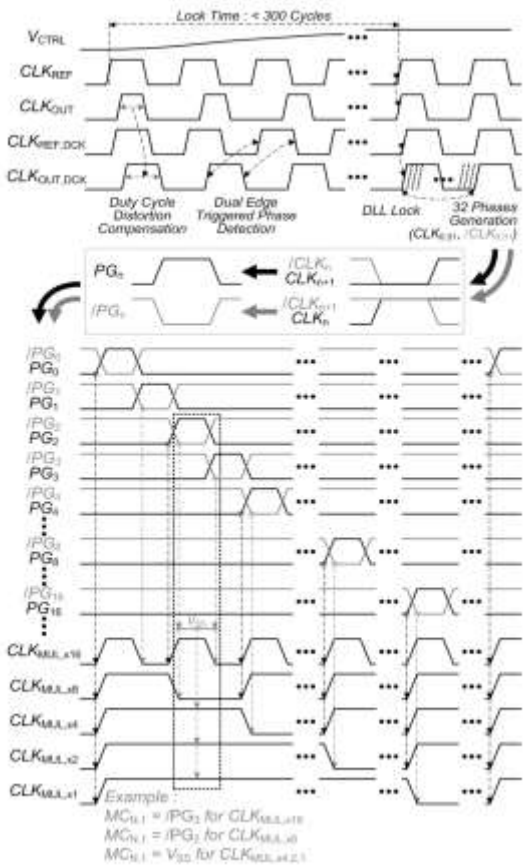

Fig. 3 Waveform of proposed clock generator

As is true for the frequency multipliers in [6]–[8], the proposed frequency multiplier may suffer from pulse overlapping owing to the multiplication -ratio control logic. To prevent this, an overlap canceller is inserted between the precombining and the push–pull stages. Its operation is also shown in Fig. 5. As shown in Fig. 4, the overlap canceller consists of simple NAND and NOR gates. If the delay of PC*P,*0 (PC*N,*0*)*generation path is less (more) than that of PC*N,*0 (PC*P,*0*)* generation path because of the process variations or layout mismatches, overlap between the high level of PC*P,*0 and the low level of PC*N,*0 can be generated. The NAND gate with PC*P,*0 and PC*N,*0inputs makes OC*P,*0 low only when both PC*P,*0 and PC*N,*0 are high. This eliminates pulse overlapping. Similarly, if the delay of the PC*N,*0 (PC*P,*1*)* generation path is less (more) than that of PC*P,*1 (PC*N,*0*)*generation path due to process variations or layout mismatches, overlap can exist between the low level of PC*N,*0 and the high level of PC*P,*1. Because a NOR gate makes OC*N,*0 high only when both PC*N,*0and PC*P,*1 are low, pulse overlapping is eliminated. Thus, highly reliable operation of the frequency multiplier can be guaranteed.

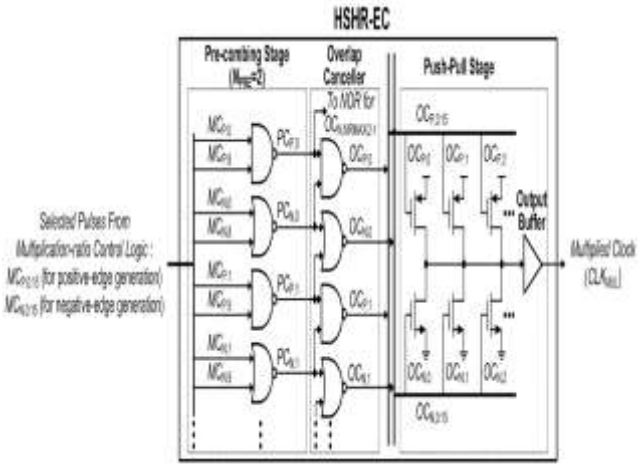

Fig. 4 Structure of the proposed HSHR-EC.

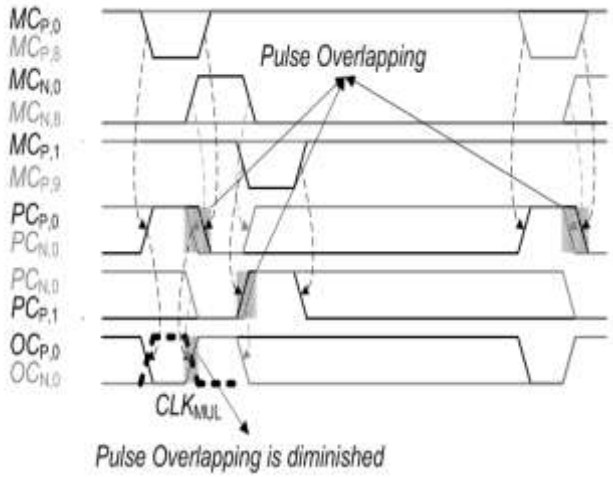

Fig. 5 Operation of the proposed HSHR-EC

IV. DESIGN AND SIMULATION RESULTS OF PROPOSED FREQUENCY MULTIPLIER

The proposed frequency multiplier was designed and simulated using Tanner EDA. The circuit design and simulation results are shown in Fig. 6(a), 6(b) and 6(c).

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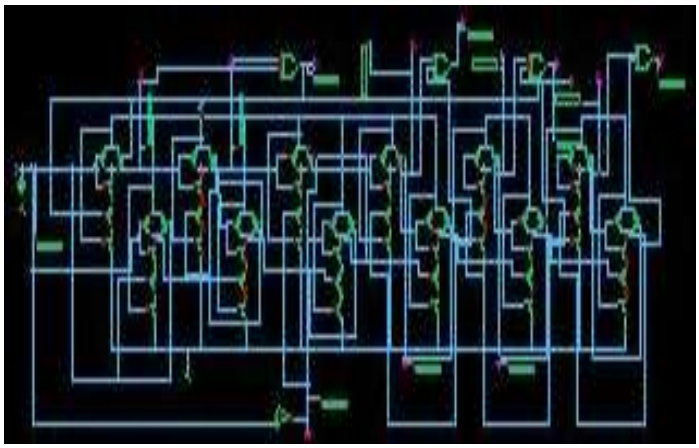
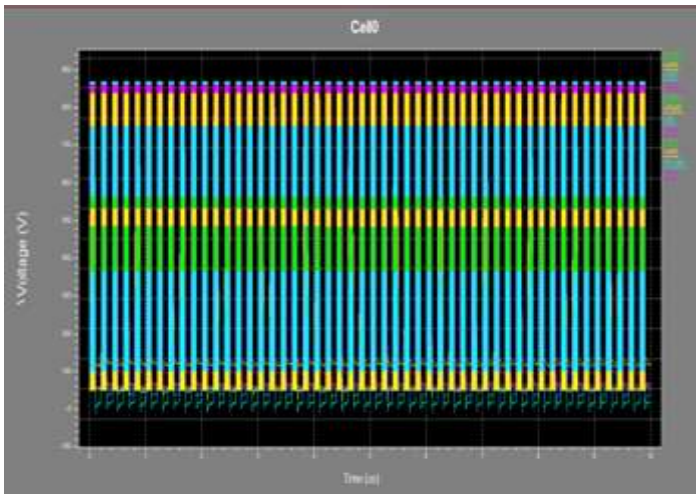
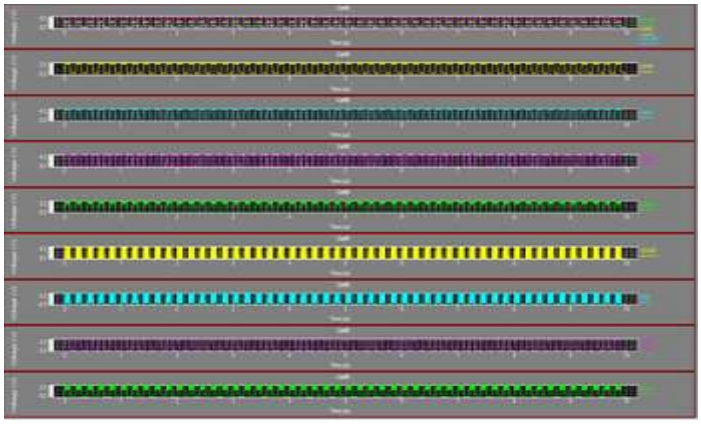


(a)



(b)

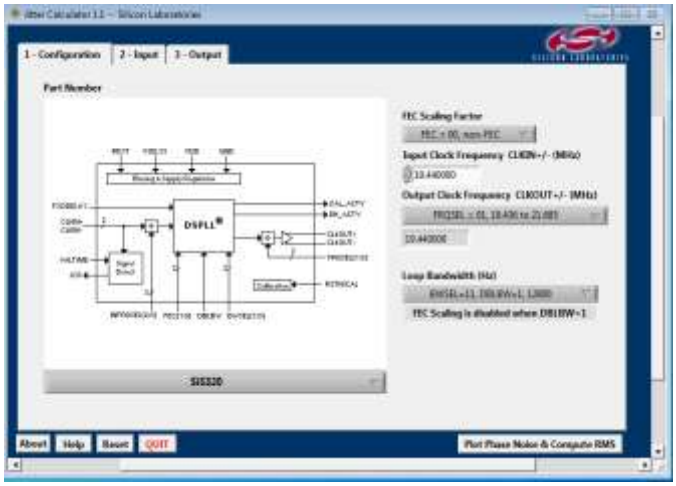


(c)

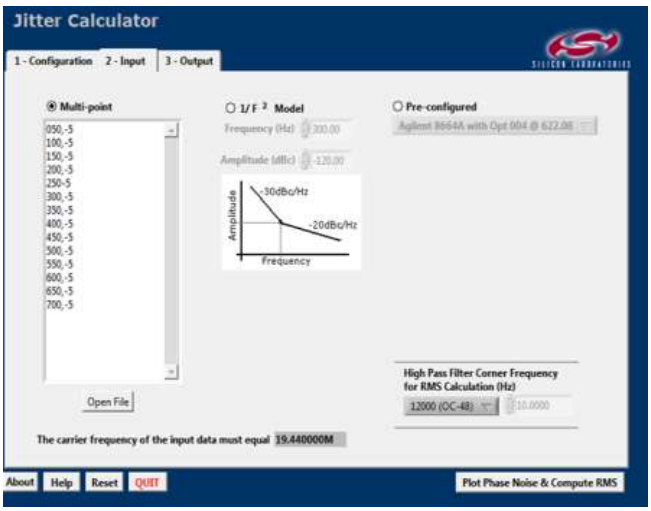
Fig. 6 Design and simulation results (a) Circuit designs of proposed frequency multiplier and (b and c) Transient analysis of proposed DLL based frequency multiplier.

V. MEASUREMENT RESULTS

The proposed frequency multiplier is implemented using a 2.5-μm CMOS process technology, and has a supply voltage of 1.2 V. the proposed frequency multiplier has the multiplication ratios of 1, 2, 4, 8, and 16, and a maximum multiplied clock frequency of 3.3 GHz.

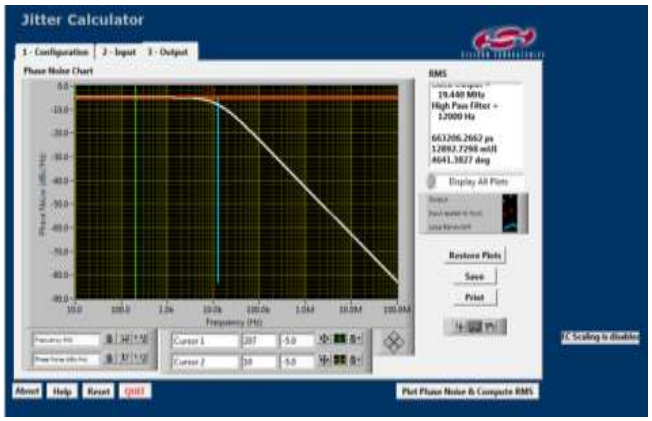


(a)



(b)

Fig. 7(c) shows the output waveform and the jitter of the DLL-based clock generator measured in the worst case condition; the operating frequency of the measured multiplied clock is 3.3 GHz with the 206.25 MHz input reference clock, giving a multiplication factor of 16.



(c)

Fig.7 Jitter calculation of proposed frequency multiplier (a) Configuration section, (b) Input section and (c) Output section.

The duty-cycle error of the multiplied clock is −0.9%–0.4%, and the rms and the peak-to-peak jitter are 1.85 and 13.6 ps, respectively. Table I shows lists the performance summary and provides a comparison with the previous clock generators. Among the DLL with frequency multiplier architectures, the proposed frequency multiplier achieves the highest maximum multiplication ratio and the highest maximum clock frequency. Thus, the proposed clock generator (frequency multiplier with DLL core) achieves the lowest power consumption to frequency ratio among the DLL with frequency multiplier architectures. Because the proposed clock generator has the highest maximum multiplication ratio and the areas of the DLL core and the frequency multiplier are proportional to the maximum multiplication ratio.

Table I PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

PARAMETERS	**EXISTING SYSTEM**				**PROPOSED SYSTEM**
	[1]	[2]	[3]	[4]	
V_{DD}	3.3 V	1.2 V	1.8 V	1.8 V	1.2 V
Multiplication ratio	4	4	4	8	16
Power Consumption of FM	Not shown	4.8mW @2GHz	17mW @1.7GHz	6.8mW @2GHz	9.6mW @3.3GHz
Normalized Area	$0.143*10^6$	$0.281*10^6$	$0.337*10^6$	N/A	$0.037*10^6$
Jitter (rms/peak-to-peak)	1.8/13.2ps @1.3GHz	3.2/19ps @1GHz	2.6/16.8ps @1.7GHz	N/A	1.9/13.6ps @3.3GHz

VI. CONCLUSION

In this paper, a frequency multiplier for a DLL-based clock generator is proposed. The modified HSHC-EC guarantees high-speed operation owing to its hierarchical edge-combiner structure and an overlap canceller.

The proposed frequency multiplier reduces the delay difference between positive- and negative-edge generation paths. Finally, a numerical analysis is performed to validate its performance. The frequency multiplier, which is implemented using 2.5-μm CMOS process technology, has the multiplication ratios of 16, an output range of 100 MHz–3.3 GHz, and a power consumption to frequency ratio of 2.9 μW/MHz.

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