International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 4 Issue: 5 549 - 553

A Novel Approach for Design of Carry Select Adder

Miss Nimisha A. Deshmukh
M tech (VLSI) student: Electronics Department
Priyadarshini College of Engineering
Nagpur, India
deshmukhnimisha03@gmail.com

Prof A. P.Khandait
Assistant Professor: Electronics Department
Priyadarshini College of Engineering
Nagpur, India
arachana.khandait@gmail.com

***Abstract*—**In VLSI technology smaller area, less power and faster units are the major concern of VLSI circuits. As addition is the basic operation of all computer arithmetic, adders are one of the widely used components in digital integrated circuit design .In many DSP processor digital adders are the fundamental block. The structure of carry propagation adder produces high propagation delay thus it reduces overall performance of DSP processor. Therefore to alleviate this problem carry select adder is used in many computational systems by independently generating multiple carries and then select a carry to generate the sum. The carry select adder uses multiple pair of ripple carry adder for generating carry, hence area and power of the circuit increase. To overcome this problem we proposed a new way to design carry select adder with transmission gates and binary to excess one converter. The area of modified carry select adder is reduced to great extent thus it consumes less power, therefore delay also get decreases.

Keywords- *carry select adder,ripple carry adder,BEC,transmission gates,modified carry select adder.*

*****

I. INTRODUCTION

The design of area and power efficient data path logic system are the main research areas of VLSI design systems. The high performance processors, or DSP processors always need a high speed adder and multiplier to increase operation speed. The speed of the digital adder is limited by time required for carry propagation through the adder. There are many types of adders having its own advantages and disadvantages like ripple carry adder, carry look ahead adder, carry skip adder etc. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Hence carry select adder is to developed to overcome the problem of carry propagation delay which drastically reduces area and power to great extent[1].The carry select adder is used in many computational and DSP processor units. The carry select adder structure possess multiple pair of ripple carry adder for generating the carry for cin=0, cin=1 and resultant sum.

However, the Regular CSLA is not area and speed efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers (MUX). Due to the use of two independent RCA the area will increase which leads an increase in delay.

The basic idea behind the proposed work is to design carry select adder with transmission gate and to use binary to excess one converter (BEC) to reduce the overall area of the circuit. Here the BEC is used in place of ripple carry adder for carry cin=1.The main advantage to use BEC logic is that it uses lesser number of logic gates than n bit full adder[2]-[4].

Therefore the modified carry select adder is designed with transmission gates and binary to excess one converter to reduce area, delay and power on comparison with regular carry select adder [5].

This work in brief is structure as follows. In section II, basic adder blocks are described corresponding to area and delay characteristics. Section III describes the structure of BEC logic and corresponding function table and logic equations. Section IV deals with architecture of modified carry select adder and its implementation methodologies and design tools and finally in section V the paper is concluded with results and simulations.

II. THE BASIC ADDER BLOCKS

The basic adder block of carry select adder is designed with ripple carry adder, BEC and mux. In this we calculate and explain the delay & area using the theoretical approach and show how the delay and area effect the total implementation. The implementation of XOR gate with AND, OR, and Inverter (AOI) gate is shown in Fig 1. Based on this approach, the blocks of 2:1 MUX, Half Adder (HA), and FA are evaluated and listed in Table I.

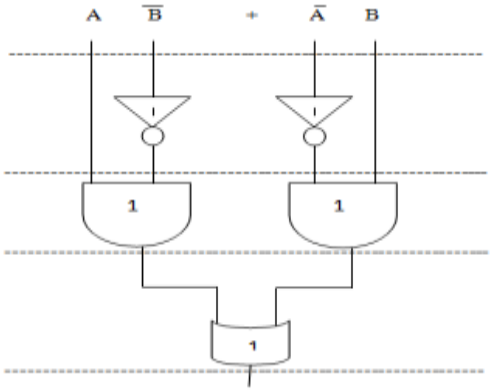

Fig.1. Delay and Area evaluation of XOR.

Table. I. Delay and Area Evaluation of basic blocks

Adder Blocks	Delay	Area
Xor	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	12

A. *Ripple Carry Adder*

A ripple carry adder is constructed with cascaded connection of n bit full adder as shown in figure 2.It is a digital circuit which produces arithmetic sum of two binary numbers. The output of ripple carry adder, can be generated from carry of previous stage. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

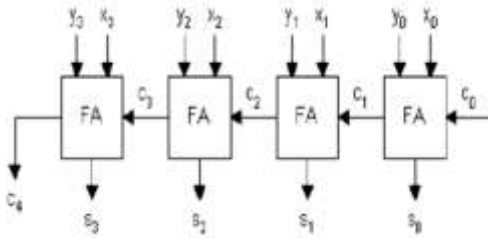

Figure 2: Conventional Ripple Carry Adder

The schematic designof riple carry Adder on Tanner EDA tool is shown in following figure 3.

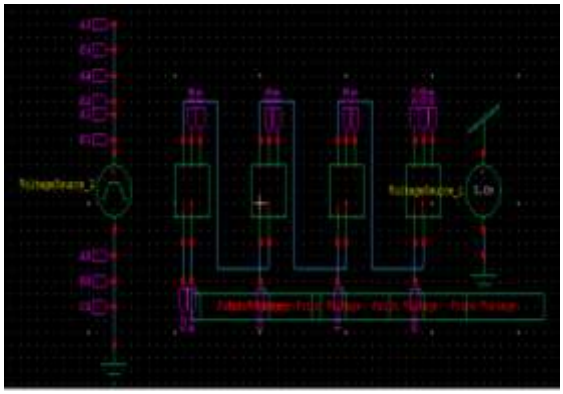

Figure3: schematic of Ripple carry adder

Here the full adders are connected in cascaded pattern .the input is given to the first block of full adder. The carry generated from least significant bit is rippled through the chain full adder to most significant bit, and we get final carry and sum for delay consideration.

B. *Conventional Carry Select Adder*

The carry select adder is one of the conditional sum adder. The output of this adder i.e. final sum and carry are calculated by considering input carry as Cin =1 and Cin =0. The final value of sum and carry are selected by multiplexer. It consists two adders for least significant bit and most significant bits that is k/2bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits two k/bit adders. As shown infigure4. In MSB adders one adder is considered for carry input as one for performing addition and another for carry input as zero. The calculated carry out from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum by multiplexer. Thus adder is divided into stages which increases the area utilization but addition operation become fast.

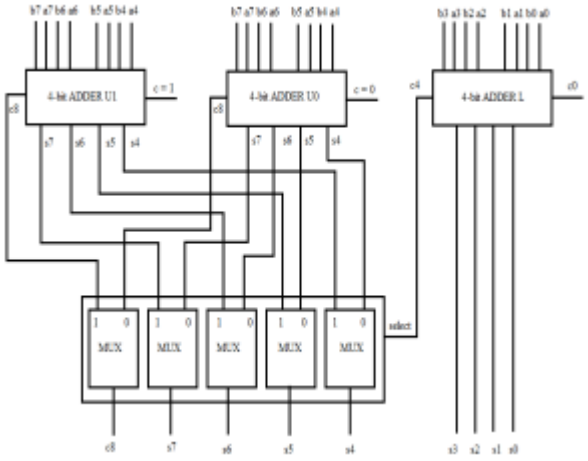

Figure 4: 8 Bit carry select adder

The schematic of conventional carry select adder is shown in following figure 5.

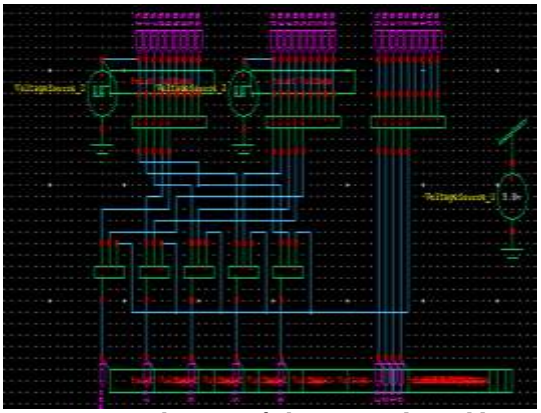

Figure 5: Schematicof8 bit carry select adder

The two ripple carry adders are used for least and most significant bits and final output i.e. sum and carry is selected by multiplexer.

III. BINARY TO EXCESS-1 CONVERETR (BEC) BLOCK

The main idea of this work is to use BEC instead of the ripple carry adder which is used in conventional carry select adder for cin =1 in order to reduce the area and power consumption of the regular CSLA.To replace n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a BEC are shown in Figure 6 and Table II, respectively.

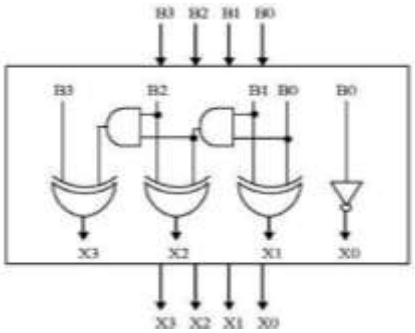

Figure 6: 4 Bit Binary to Excess-1 Converter

Table II: Function table of BEC

Input B[3:0]	Output X[3:0]
0000	0001
0001	0010
0010	0011
⋮	⋮
⋮	⋮
⋮	⋮
1110	1111
1111	0000

The inputs of BEC are B0 to B3 while outputs are X0 to X3 as shown in figure. One input of the mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The main advantage of using BEC is reduction in area of the circuit. The Boolean expressions of the BEC is listed as

X0= not (B0) ---------- (1)

X1=B0 xor B1 ---------- (2)

X2= B2 xor (B0 and B1---------- (3)

X3= B3 xor (B0 and B1 and B2) ---------- (4)

IV. MODIFIED CARRY SELECT ADDER

The area consumption of carry select adder is more as it uses the multiple pair of ripple carry adder for generating carry. To overcome this problem we have proposed a new design of carry select adder using transmission gates and BEC.

A. Transmission Gates

A transmission gate is an electronic analog switch which selectively passes or block the signal from input to output. It is comprises of pMOS and nMOS transistors shown in figure 7. The control gates are biased in a complementary manner so that both transistors are either on or off.

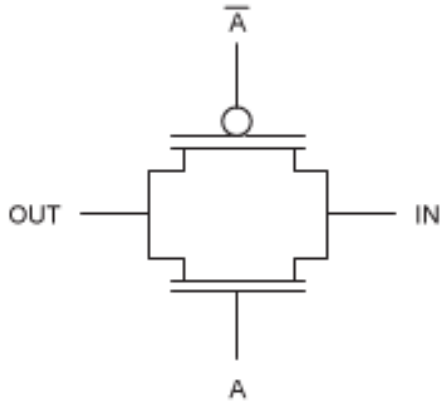

Figure 7. Schematic representation of a transmission gate.

B. Modified Carry Select Adder

The modified carry select adder structure comprises of BEC, Transmission gates and ripple carry adder. We replace ripple carry adder used for cin=1by BEC. The overall circuit is made up of transmission gates. Following figure 8 shows the diagram of modified carry select adder.

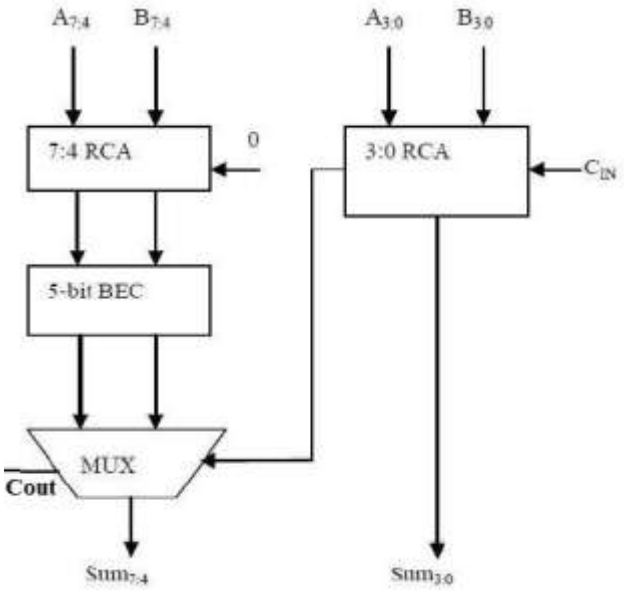

Figure 8: Modified carry select adder

The following figure 9 shows the schematic of modified carry select adder using Tanner EDA tool.

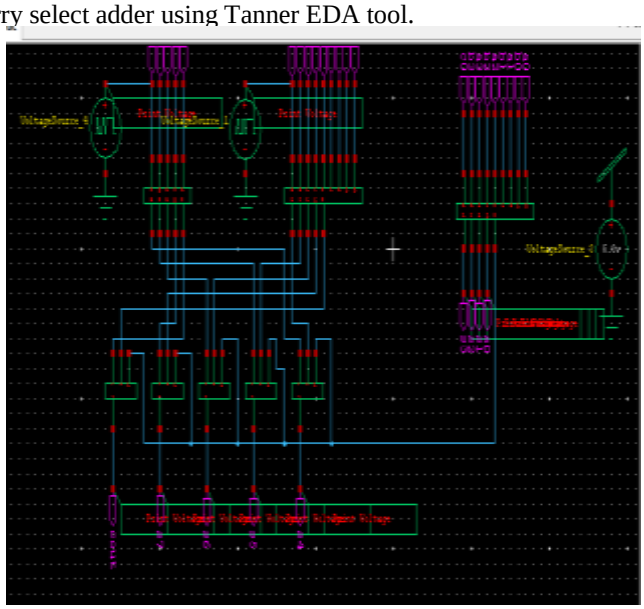

Figure 9: Schematic of modified carry select adder

V. SIMULATION AND RESULTS

The carry select adder and modified carry select adder are designed in s-edit of tanner tool and compared as shown in above figures. Here we have used TSPICE simulation with 180 nm CMOS technology file of frequency 50 MHz and supply voltage of 5V.Thus the proposed designed has less no of transistors compared to conventional carry select adder.

The following figure 10, 11 shows simulation result and timing analysis of conventional carry select adder respectively.

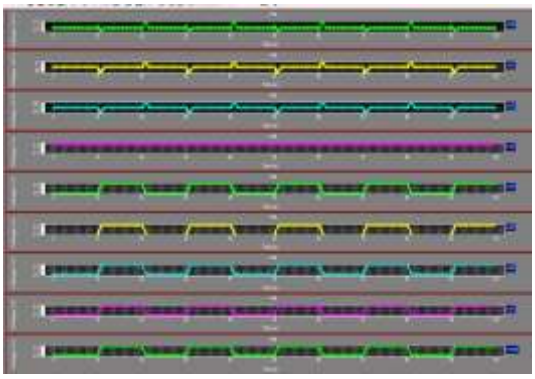

Figure 10: Simulation of CSA using transmission

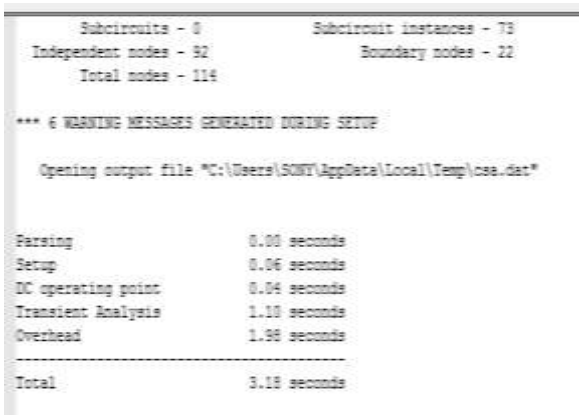

Figure 11: Timing analysis of Carry select adder

The simulation result and timing analysis of modified carry select adder using BEC is given in following figures 12, 13 respectively.

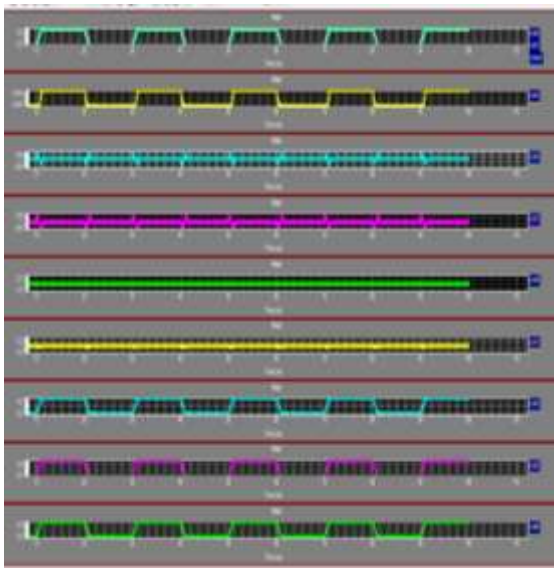

Figure 12: Simulation Modified CSA with BEC

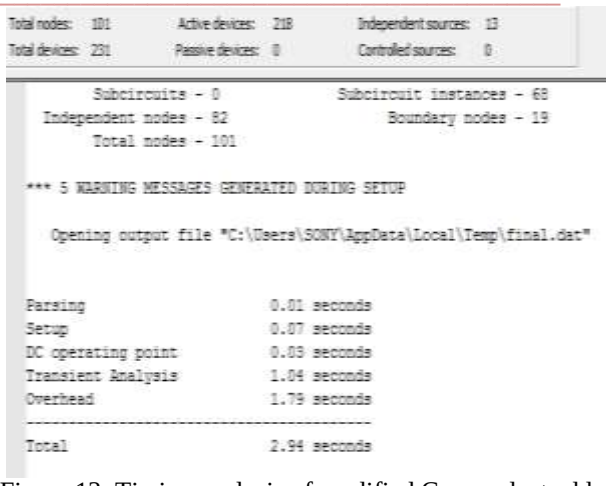

Figure 13: Timing analysis of modified Carry select adder

Following table III will show the comparison between conventional and modified carry select adder.

Table III. Comparison between conventional carry select adder Vs Modified carry select adder

Sr. No	Carry select Adder	Delay	Transistor count
1	Regular carry select adder	3.18sec	246
2	Modified carry select adder	2.94 sec	218

CONCLUSION

The conventional carry select adder and modified carry select adder are compared. The modified carry select adder is designed by transmission gate .In this adder one of the ripple carry adder is replaced by binary to excess one converter to reduce area and to optimize power and delay. From the above comparison table III, it is clear that proposed design has low area, delay and power in comparison with conventional carry select adder. The simulation results showed that the proposed system performs better with the binary to excess one converter than the regular one. We have used very small number of bit a - 8bit adder. We can increase the number of bits and analyze the performance.

REFERENCES

[1] Ceiang ,T. Y. and Hsiao,M. J. ,(Oct. 1998),"Carry-select adder using single ripple carry adder," Electron. Lett., vol. 34, no. 22, pp. 2101– 2103.

[2] O. J. Bedrij, "Carry Select Adder", IRE Transactions Electronic Computers, pp 340-344, 1962 .

[3] B. Ramkumar and H.M. Kittur, " Low power and area efficient Carry Select Adder", IEEE Trans. Very large scale integration system, vol. 20,pp. 37-375,Feb. 2012 .

[4] J. M. Rabaey, Digtal Integrated Circuits—A Design Perspective. Upper Saddle River, NJ: Prentice-Hall, 2001.

[5] B. Ramkumarnd Harish M Kittur, "Low Power and Area Efficient Carry Select Adder" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems-2011.

[6] Basant Kumar Mohanty, Senior Member IEEE and Sujit Kumar Patel, "Area-Delay-Power efficient Carry select adder", IEEE Trans. On circuits and system-II, vol.61, no.6, Jun. 2014.

[7] Nishan Singh, Amardeep Singh, Mandeep Kaur, Puneet Jain, "An Efficient Full Adder Design using Different Logic Styles", IJCA (0975-8887),vol.98, no.21, Jul. 2014 .

[8] Edison A.J., Mr. C.S. Manikandababu, " An efficient Carry Select Adder architecture for VLSI hardware implementation", IJMIE, vol.2, Issue 5, May2012.

[9] Chithra1, G.Omkareswari,"128-bit Carry Select Adder Having Less Area And Delay", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 7, July 2013.

[10] Bokam Krishnaveni1, P.Saroja,"An Efficient Implementation Of Carry Select Adder With Low Power And Area Efficient Characteristic",International journal of Advanced Research in Comptuer and communication Enginering,Vol. 3,Issue 11 Nov 2014.