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Modified DA based FIR Filter in Multirate DSP systems on FPGA

Mrs. Bhagyalakshmi. N
Research Scholar,
Department of ECE, JainUniversity,
Bangalore, India,
blndck@gmail.com

Dr. Rekha K. R
Professor,
Department of ECE, SJBIT,
Bangalore, India,
rekha.sjbit@gmail.com

Dr. Nataraj K. R
Professor and Head,
Department of ECE, SJBIT,
Bangalore, India,
krnataraj@sjbit.edu.in

Abstract — Multirate systems are popular in DSP.Systems which employ multiple sampling rates in the processing of digital signals are called Multirate DSP systems, which are used in audio, video processing and communication systems. Multirate DSP systems that employ different chips for different frequency signal results in more area and power utilization. The setback can be avoided by implementing Multirate system, based on Distributed Arithmetic FIR filter. Using such systems, we can achieve computation efficiency and improve the system performance. Modified DA based FIR Filter using Multirate systems includes decimation, interpolation process implemented on FPGA with 53% less LUT utilization compared to existing Multirate system.

Keywords— *Distributed Arithmetic (DA), DSP, FIR, Filter, FPGA, LUT, Multirate.*

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I. INTRODUCTION

The Digital Signal Processing is one the fastest growing technology in digital communication systems over more than three decades. The digital filters are the main basic building blocks of DSP systems. The digital filter is used to remove unwanted noise in the incoming signals [1].The FIR (Finite Impulse Response) is most preferable digital filters because of its simple structure and stable characteristics. For achieving high speed computation in DSP Systems, FIR filters are used and it is implemented on dedicated hardware than software systems. The FIR filters are used in many applications that include audio, video, InfraRed, Visual Object Tracking, ECG signal constructions etc.

There are many ways to design FIR filters, which can be realized in recursive and non-recursive techniques. In the Direct form, normal FIR filter gives the filter output by computing inner product which leads to long critical path. To avoid these problems, many solutions are designed which includes parallel and pipelined methods.The DA (Distributed Arithmetic) method is one best method to reduce hardware resources by replacing the convolution multipliers by LUT's to get high throughput.

The paper is organized as follows. A Brief review of DA algorithm based FIR Filter is given in section 2. Section 3 presents the implementation of DA based reconfigurable FIR Filter design. Section 4 presents the DA algorithm based FIR Filter in multirate systems.The results and analysis are presented in section 5 and conclusion is presented in section 6.

II. RELATED WORK

DA based FIR filter that is designed in [2], is a memory based generation of upsampling along with interpolation method which can be modified or extended for filter design. The upsampling is one of the methods that are used to insert zeros between the original input samples followed by FIR filters. They have used, in interpolation method to store the LUT values instead of Memory blocks.The interpolation values are output samples which are sequentially connected with the help of simple counter which eliminates the zeros in the design and improves the design area. They are using two dimensional shifts plus rotate registers which is used to shift the samples vertically and rotate horizontally to give better result. The raised-cosine filter is used in example design. It acts as a band –limited filter and impulse response for the roll-off factor of 0.3 and upsampling value of 5 is obtained.

The performance is analyzed based on the parameter constraints like area, memory and mainly speed is considered to design the FIR filter using DA based approach in [3]. In FIR filter design, number of taps, plays a vital role for performance constraints. If the number of taps increases, the memory usage also increases exponentially, then the design operates at low speed. To solve these issues, two approaches are designed. One approach is to use Individual Scaling Accumulator for each DA based block and the other is to use only one Scaling Accumulator for all DA based blocks. With these approaches, reduction in memory usage is achieved along with improvement in the area and operating speed.

In paper [4], FIR filter based on DA algorithm is designed and compared with traditional multiply-add method on FPGA.The computation of multiply-accumulate operation is realized using DA algorithm. They have designed 16-tap filter and it is analyzed in two tests with 5MHZ sampling frequency. They have used tree based shift-adder module to reduce the delay time. The architecture is based on FPGA with reliability of the system and design precision.

The pipelined architecture of adaptive FIR filter is designed using DA method in [5] [6]. Adaptive filter based on DA-technique is designed using LMS algorithm for higher orders. They are replacing MAC operators with bit serial nature of LUT shift-add unit. The architecture is same as [3], with some changes in the design. The architecture is improved in terms of slices and there is reduction in delay.

By using systolic DA, the partial reconfigurable FIR is designed in [7]. In DA-LUT Architecture, the reconfigurable partition contains only filters coefficients than LUT coefficients and it greatly reduces the area of reconfigurable partition. The LUT values are calculated and updated in LUT RAM. Hence reconfigurable area is exponentially reduced by partition. They have used two modules for reconfigurable partition on FPGA, one is high pass filter and the other is low pass filter. Once implementation is done, partial Bit file is

generated with great reduction in size. So time taken to reconfigure the FPGA is also reduced to great extent.

III. IMPLEMENTED RECONFIGURABLE DA-BASED FIR FILTER

The DA implementation of a FIR filter mainly consists of N-bit shift registers; Arithmetic table like LUT's, scalable accumulator includes adders/subtraction unit and registers. When DA algorithm is directly applied to realize FIR Filter, the complicated multiplication-accumulation operation is converted to the shifting and adding operation. To achieve best configuration in terms of coefficient of FIR filter, the storage resource and the calculating speed, the DA algorithm is optimized and improved in terms of algorithm structure, the memory size and the look-up table speed.

Here, we propose reconfigurable DA-based FIR filter for FPGA implementation. The number of registers required, for the implementation of LUTs for FIR filter of length N is designed. But, registers are scarce resource in FPGA since each LUT in many FPGA devices contains only two bits of registers. Therefore, the LUTs are required to be implemented by distributed RAM (DRAM) for FPGA implementation. The multiple number of partial inner products $S_{l,p}$ cannot be retrieved from the DRAM simultaneously since only one LUT value can be read from the DRAM per cycle. Moreover, if L is the bit width of input, the duration of sample period of the design is L times the operating clock period, which may not be suitable for the application requiring high throughput.

Fig. 1 shows the structure of the proposed time multiplexed DA-based FIR filter using DRAM, the proposed structure has Q sections, and each section consists of P DRAM-based Reconfigurable Partial Product Generators (DRPPG) and the Pipeline Adder Trees (PAT) to calculate the rightmost summation followed by shift accumulator that performs over R cycles according to the second summation. However, we can use dual-port DRAM to reduce the total size of LUTs to half since those two DRPPGs from two different sections can share the single DRAM.

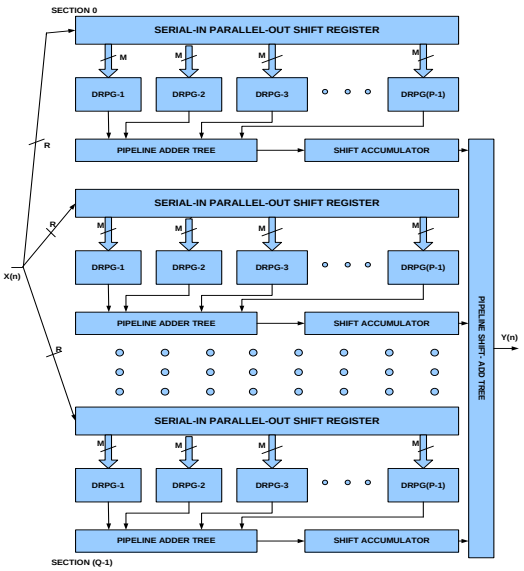

Figure 1. The Implemented Structure of the DA-based FIR Filter.

IV. DA-BASED FIR FILTER IN MULTIRATE SYSTEMS

The multirate systems majorly contain two processes. In that, one is decimator and other one is interpolator. These two processes are used in DSP system. Instead of Normal Low pass Filter we are using DA based FIR filter in Decimator and Interpolator process.

Decimation:

In sampling process, we usually use continuous time signal X(t) and convert to n number of samples X[n]. Where as in decimation process, the discrete time signal X[n] is converted to other discrete time signal Y[n] and it contains X[n] sub samples.

The mathematical definition of decimation process or down sampling or *M*-fold decimation is as given by equation (1) below. The decimation process is a down sampling method and its sampling rate is reduced from F_s to F_s/M by decreasing M-1 samples for every M samples in input sequence.

$$y[n] = v[nM] = \sum_{k=-\infty}^{\infty} h[k]x[nM-k] \qquad (1)$$

The decimation process is as shown in the Fig. 2.The FIR filter based on DA is used to position the down sampler to avoid the aliasing effect because of less sampling rate.v[n] is filtered output. Fs are sampling frequency of X[n] and Fs/M is output of Y[n].

Interpolation:

Interpolation is a reverse process of Decimation and the process is maintained in its original operation after filtering, means all the sampling data X[n] are available in Y[n] signal.

The mathematical definition of interpolation process or up sampling or *L*-fold interpolation is as given by equation (2) below.

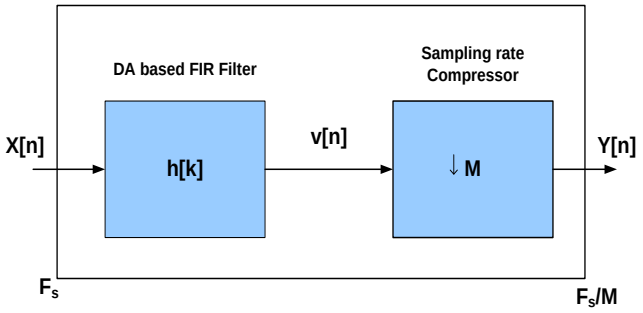

Figure 2. Internal Structure of Decimation process.

$$y[n] = L\sum_{k=-\infty}^{\infty} h[k]w[n-k] \qquad (2)$$

Where w[n] = X [n/L], if n/L is an integer and
w[n] = 0, if n/L is a non- integer.

The interpolation process is as shown in the Fig. 3. It contains sampling rate expander along with DA based FIR filter. By adding (L-1) zero valued samples for each input sample data, the sampling rate is increased from Fs to LFs.

The whole process is followed with DA based FIR filter called Anti –imaging filter.

Sampling rate conversion is commonly used in multirate Digital Signal Processing. To get the required integer ratio, we need to increase or decrease sampling rate**.** The rational integer ratio L/M (where L and M are integers) of sampling frequencies is achieved by the cascading of two above process, by first interpolating the process by L followed on decimating by M as shown in Fig. 4. Interpolation gives LFs and decimation produces Fs/M operating at the same sampling rate in cascade process.

For efficient implementation, we combine two DA based FIR filter into single FIR filter based on DA is as shown in Fig. 5 and it gives the output Fs (L/M). In general, decimation or interpolation process depends upon the value of L, where L should be greater or less than M. If L=1, then the modules acts as a decimator as shown in Fig. 2. and if M=1, then the modules acts as an interpolator as shown in Fig. 3.

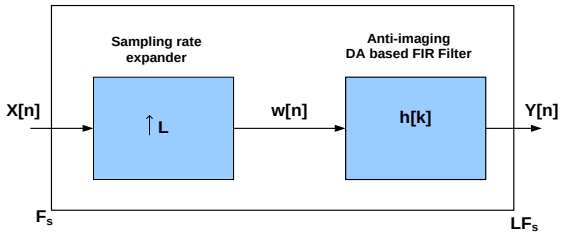

Figure 3. Internal Structure of Interpolation process.

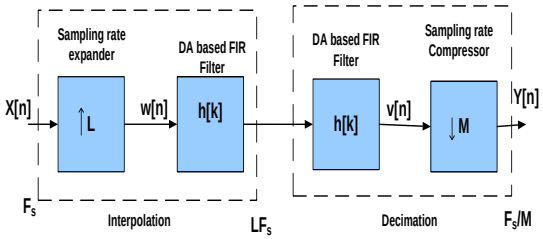

Figure 4. Cascade of Decimation and Interpolation process.

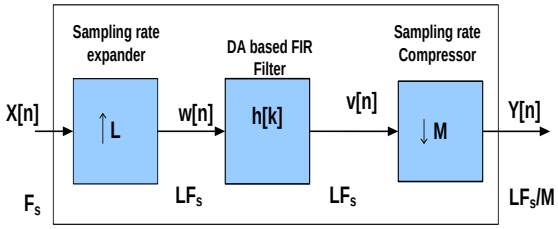

Figure 5. Block Diagram of Cascade process

We can reduce the sampling rate by using multistage method decimation process. In Fig. 6. we are considering 2-stage. It can be extended to k-stages where $M=M_1, M2\ldots..M_K$ or $L= L_1, L2 \ldots..L_k$.

By using multistage method, we can reduce the filtering complexity in terms of aliasing, anti-imaging and it leads to less computational effort.

V. RESULTS AND ANALYSIS

The DA based FIR filter in multirate systems are implemented on Spartan3PQ208 using Verilog language with the help of XilinxISE13.4 tool and simulated on Modelsim 6.3f. The Top Module, RTL architecture and simulation results of multirate systems with DA Based FIR filter is as shown in the Fig. 7(a), 7(b) and 7(c). respectively. The simulation results of interpolation and decimation process using FIR Filter based on Distributed Arithmetic is as shown in the Fig. 7(d) and 7(e) respectively.

The Table I and II shows the implemented design utilization results of Multirate system, decimation and Interpolation using DA Based FIR filter respectively.

The timing summary shown in Table III gives maximum operating frequency and minimum period. The decimation process shows high frequency and this improves the throughput of the design.

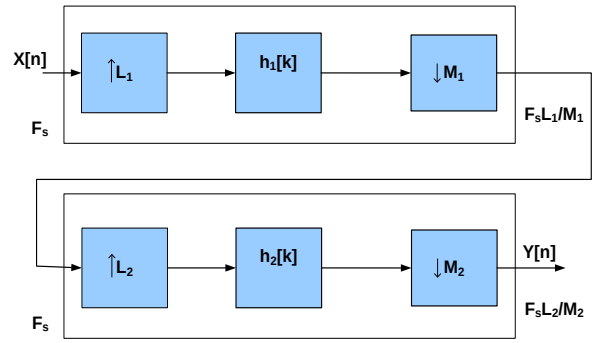

Figure 6. Block Diagram of Multistage method (2-stages)for the Decimation process.

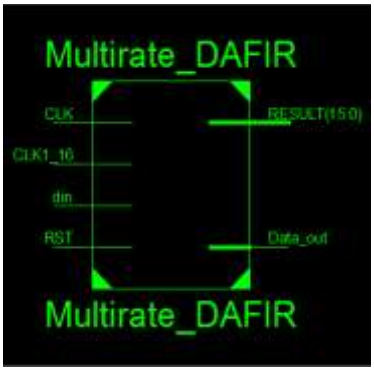

Figure 7(a). Top Module of Multirate systems with DA Based FIR Filter.

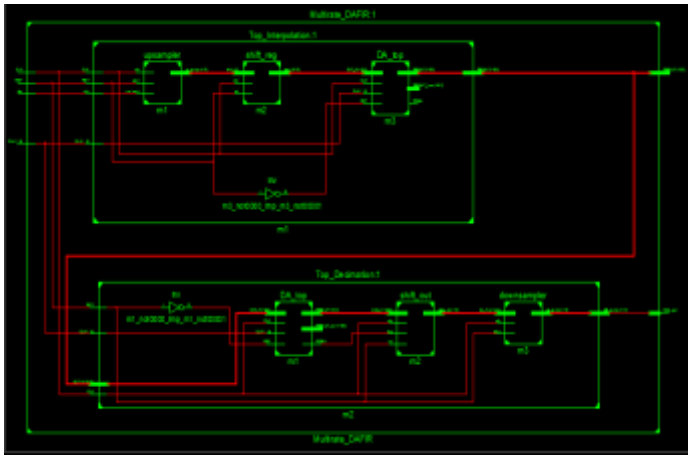

Figure 7(b). RTL Architecture of Multirate systems with DA based FIR Filter.

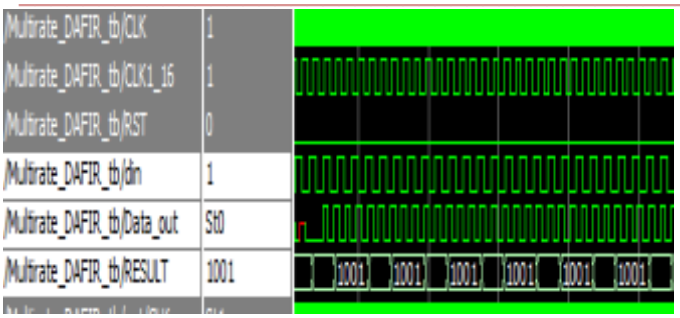

Figure 7(c). Simulation results of Top Module multirate Systems with DA based FIR filter.

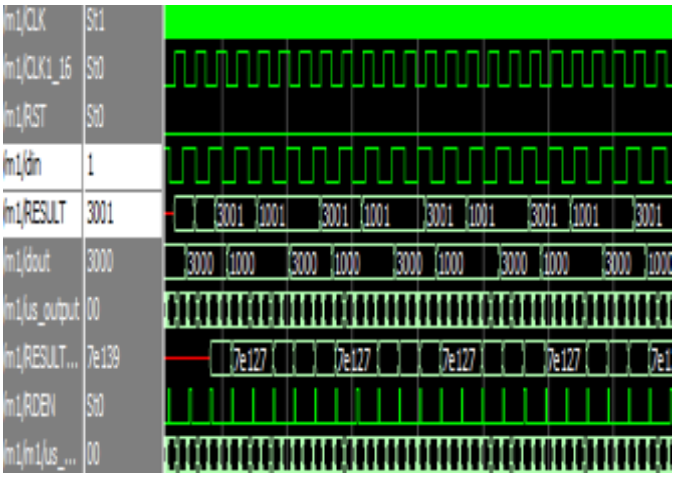

Figure 7(d). Simulation results of Interpolation process with DA based FIR filter.

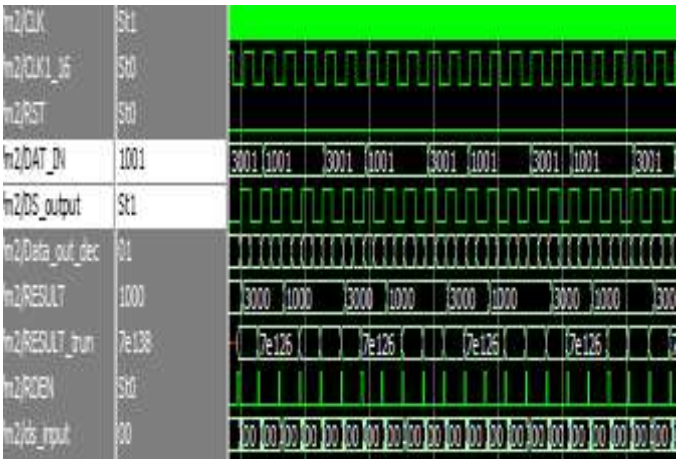

Figure 7(e). Simulation results of decimation process with DA based FIR filter.

TABLE I. IMPLEMENTATION RESULT OF TOP MODULE

	Device – Spartan 3PQ208	Multirate system with DA based FIR	
Logic Utilization	Available	Used	Utilization
Number of slices	3584	528	14%
No. of Slice Flip-Flops	7168	683	9%
No. of 4 input LUTs	7168	873	12%
No. of bonded IOB's	141	21	14%
No. of GCLKS	8	3	37%

TABLE II. IMPLEMENTATION RESULT OF DECIMATION AND INTERPOLATION MODULES

	Device – Spartan 3PQ208	Decimation with DA based FIR		Interpolation with DA based FIR	
Logic Utilization	Available	Used	Utilization	Used	Utilization
Number of slices	3584	261	7%	288	8%
No. of Slice Flip-Flops	7168	337	4%	366	5%
No. of 4 input LUTs	7168	414	5%	468	6%
No. of bonded IOB's	141	21	14%	20	14%
No. of GCLKS	8	3	37%	2	25%

TABLE III. TIMING SUMMARY

Time/Frequency	Decimation Design	Interpolation Design
Minimum Period	3.65ns	6.829ns
Maximum Frequency	273.695 MHz	146.438 MHz

VI. CONCLUSION

Here we have discussed about DA Based FIR filter with Multirate DSP systems which includes decimation and interpolation and its operations. The LPF is replaced with DA based FIR filter to improve the performance and computational time. By using multistage method we can reduce the small amount of filtering effects like aliasing, anti-imaging. We have implemented multirate system using DA based FIR filter on Spartan3 FPGA.Our design gives better results in terms of high speed by using both decimation and interpolation in a single design and less resource utilization for lower end devices.

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BIOGRAPHY

Mrs. Bhagyalakshmi.N obtained her M.Tech Degree from Visvesvaraya Technological University, Bangalore, India in 2007. She is pursuing her Ph.D degree in Jain University, Bangalore, India. Presently she is working as Associate Professor in the department of Electronics and Communication Engineering at Vivekananda Institute of Technology, Bangalore. Her research interests include FPGA Implementation, VLSI Design and Embedded Systems. Received Best Base paper award for the Conference paper titled "Analysis of High Performance FIR Filter Using Improved Distributed Arithmetic", Oct 2013. She is a life member of MIE and IETE.

Dr.K.R.Rekha obtained her PhD degree from Dr.MGR University, Chennai, India in 2011.Presently she is working as Professor in the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. Her research interests include Wireless communication, FPGA implementation, Microcontroller and Embedded Systems Design. She is a member of MIE, MISTE and IETE.

Dr.K.R.Nataraj obtained his PhD degree from Dr.MGR University, Chennai, India in 2010. He worked as Professor and Head of the Department during 2000-2008 and as Post Graduate Coordinator in the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. Presently, He is heading the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. His research interests include Wireless communication, FPGA implementation, and Microcontroller and Embedded systems design. He is a member of MIE, MISTE, IETE and IEEE.