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# Systematic Design Methodology for Successive – Approximation ADCs

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***Abstract* —** Successive – Approximation ADCs are widely used in ultra – low – power applications. This paper describes a systematic design procedure for designing Successive – Approximation ADCs for biomedical sensor nodes. The proposed scheme is adopted in the design of a 12 bit 1 kS/s ADC. Implemented in 65 nm CMOS, the ADC consumes 354 nW at a sampling rate of 1 kS/s operating with 1.2 supply voltage. The achieved ENOB is 11.6, corresponding to a FoM of 114 fJ/conversion – step.

***Keywords –*** *analog – to – digital conversion, low – power, capacitive DACs, sytematic design.*

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## I. INTRODUCTION

Biomedical implant devices and wearable biomedical nodes are rapidly growing, holding an increasing portion in the market share of consumer electronics. For such devices to be efficient and competitive, they must operate under low supply voltages and at very low levels of power consumption in order to prolong the battery lifetime. Successive – Approximation Register (SAR) ADCs are becoming widely used in many applications with ultra – low power requirements, and have become a dominant choice in designing ADCs for bio – potential signals' acquisition and monitoring sensor nodes [1 – 4].

While being a prioritized option in high – speed medium – resolution ADCs, Pipelined structures have OTAs at the core of their architecture, which are becoming harder to design as technology scales since supply voltages are reducing along with the intrinsic gain of the transistors. Sigma – Delta ADCs are preferred for high resolution applications, but they rely on oversampling; hence, inefficient.

SAR ADCs on the other hand rely on a mostly digital architecture, which lends itself to low power operation, and leverage many of the scaling advantages. Owing to their simple structure, SAR ADCs are well – known for their extreme power efficiency, achieving very – low figures – of merit (FoM) [5 – 7].

Driven by its importance and growing role in the low – power applications market, this paper describes a systematic design procedure for designing ultra – low power high – resolution SAR ADCs. At high resolutions, the design of SAR ADCs with low FoMs becomes more challenging due to the inaccuracies encountered in their sub – blocks, such as matching requirements and layout parasitics, making a systematic design methodology a remarkable shortcut for achieving high performance metrics, while optimizing many of the trade – offs against each other. This paper presents a 1 kS/s, 12 – bit SAR ADC based on the proposed design procedure.

The paper is organized as follows. Section II describes the basic SAR ADC architecture and its operation principles. Section III presents the detailed design procedure, while circuit design details are presented in Section IV. ADC simulation results and performance summary are shown in Section V. Finally, Section VI concludes the paper.

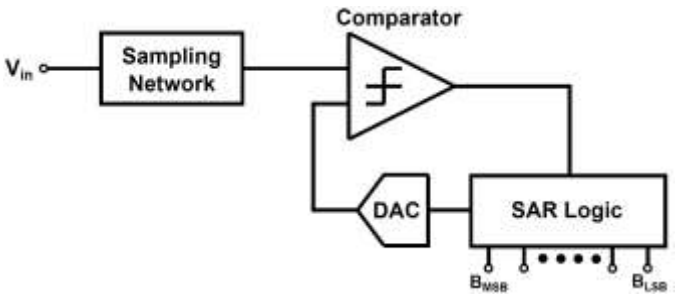


Fig. 1. SAR ADC Basic Architecture

## II. BASIC SAR ADC ARCHITECTURE

A typical SAR ADC consists of a sampling network, a digital – to – analog converter (DAC), a comparator, and SAR logic. The SAR architecture is shown in Fig. 1. In almost all modern SAR ADCs, the sampling network is merged with the DAC circuitry [8].

The SAR operation can be explained as follows: the conversion starts by sampling the input signal ($V_{IN}$) and then adopting the binary search algorithm. First, the SAR logic sets the output of the DAC to half of the full scale voltage ($V_{FS}$), defining whether the most significant bit (MSB) is logic "1" or logic "0" depending on the output of the comparator. If the comparator decides that $V_{IN}$ is larger than $V_{FS}/2$, the DAC is reconfigured to output an analog voltage equal to $3V_{FS}/4$, else, the output is set to $V_{FS}/4$. The algorithm continues reducing the error between the sampled input signal $V_{IN}$ and its digital approximation defined by the successive DAC outputs until $N$ bits have been resolved. From the previous operation description, it can be inferred that a complete conversion in a typical SAR ADC requires $N + 1$ clock cycles; one for sampling the input and the rest for resolving $N$ bits, starting from the MSB down to the least significant bit (LSB).

Fig. 2 shows another representation of the SAR ADC architecture, where the DAC is implemented using a capacitive DAC (CDAC), while the input sampling network is simply represented by the input sampling switches. Depending on the output of the comparator, the SAR logic turns ON and OFF the appropriate DAC switches. For proper operation, the top plates of the CDACs should be purged to the common mode voltage ($V_{CM}$) while the input is being sampled on the bottom side of the capacitor plates.

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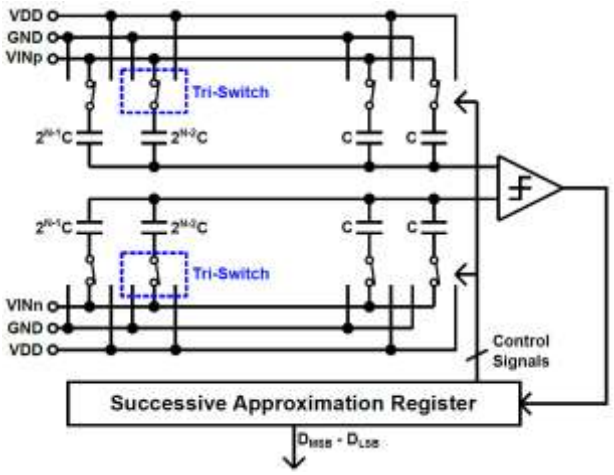


Fig. 2. SAR Architecture with Merged CDAC & Sampling Network

## III. Systematic Design Procedure

### A. Internal DAC

The proposed design procedure starts by designing the core of the SAR architecture, the CDAC. CDACs are used rather than resistive or current DACs due to their relative ease of matching, and more importantly, their zero static power consumption; allowing for ultra – low power operation.

The CDAC is responsible for providing accurate successive reference levels, and since no scaling takes place during the conversion, all the comparisons should be done at the overall accuracy. The choice of the CDAC unit capacitance ($C_U$) is defined as the maximum of two minimum limits: mismatch, and noise, while having an upper limit imposed by settling; that is:

$$\max\{C_{U\min,m}, C_{U\min,n}\} \le C_U \le C_{U\max,s} \quad (1)$$

where $C_{U\min,m}$ and $C_{U\min,n}$ are the minimum limits imposed by matching and noise requirements, respectively, and $C_{U\max,s}$ is the upper limit defined by settling requirements.

CDAC mismatches between the unit capacitors directly define the overall ADC static nonlinearities; namely, the differential – and integral – nonlinearities (DNL & INL). In LSB units, the standard deviation of the DNL and INL is usually chosen to satisfy:

$$\sigma_{DNL,INL} \le \frac{1}{2\alpha} \quad (2)$$

where α is an integer equal to 1, 2, or 3 depending on the required yield percentage; 68%, 95%, or 99.7%, respectively.

The function relating the DNL/INL standard deviation and the unit capacitance mismatch depends on the CDAC topology; whether a conventional binary weighted (CBW) CDAC as shown in Fig. 2, a split – array CDAC [8], CBW with attenuating capacitor (BWA) [9], or others is used. These topologies trade – off with each other in terms of area, total capacitance, number of switches, routing complexity, and their dynamic power consumption. Thus, the DNL/INL standard deviation is a function of the used topology, the value of the unit capacitance, and the ADC number of bits, and can be expressed by:

$$\sigma_{DNL,INL} = F(\text{Topology}, C_U, N) \quad (3)$$

By deriving the function $F$ for a given CDAC topology, the value of $C_{U\min,m}$ can be easily calculated.

The sampling network defines the other two limits. As depicted in Fig. 2, during the sampling phase, the input signal is connected through the tri – switches to the CDAC. In the context of low – power applications, the sampling network is simply a sampling switch; whereas the CDAC input capacitance ($C_{IN}$) resembles the load/hold capacitance.

The second limit is associated with the thermal noise of the sampling switch noise given by:

$$V_{Sw,N,tot}^2 = kT/C_{IN} \quad (4)$$

where $k$ is Boltzmann constant, and $T$ is the temperature in Kelvins.

The sampling switch noise is targeted to be less than the ADC quantization noise, imposing another theoretical minimum on the total CDAC input capacitance, hence, its unit capacitance value, $C_{U\min,n}$.

The third performance metric governing the choice of $C_U$ is the sampling switch settling behavior which defines $C_{U\max,s}$. Modeling the sampling switch with its ON – resistance ($R_{ON}$), and allocating only one clock cycle, $T_{CLK}$, for input sampling, an upper limit must be enforced on the switch time constant ($C_{IN}R_{ON}$) for the output to settle within half an LSB. Assuming an exponential settling, and a worst case input of $V_{FS}$, the time constant of the switch is given by:

$$\tau = R_{ON}C_{IN} \le \frac{1.4T_{CLK}}{N+1} \quad (5)$$

Based on the ADC design scenario, the proper value of $C_U$ differs based on the chosen topology. For example, in high speed applications where driving large capacitance may prove power hungry, the limit given by (5) may dominate the choice of $C_U$, sacrificing other performance metrics, such as static linearity for example. In applications where area and power consumption are vital, a CDAC topology should be chosen so that $C_{IN}$ is minimized. As a final example, in applications where DNL and INL figures are of major concern, the CDAC topology with minimum $F$ should be elected. Regardless of the starting point, the three aforementioned limits should be iteratively calculated for different set of specifications and/or CDAC topologies until a satisfactory compromise is reached.

### B. Sampling Switches

The main errors introduced by the sampling switches can be categorized into offset, gain, and linearity errors; whereas thermal noise has been dealt with in the CDAC design (4). In SAR ADCs, offset and gain errors are easily accounted for in the digital domain, leaving linearity as the main performance metric. For biomedical applications, the sampling rates are rather low, excluding $C_{U\min,s}$ from $C_U$ limit's list, but imposing an upper limit on $R_{ON}$ for adequate settling.

The major issue is, however, the input signal dependent nature of $R_{ON}$, resulting in a number of undesired harmonics at the output, degrading the overall ADC linearity performance; namely, total harmonic distortion (THD) and, hence, the signal

to noise plus distortion ratio (SNDR). The THD and SNDR are limited by the ON – resistance of the switch given by:

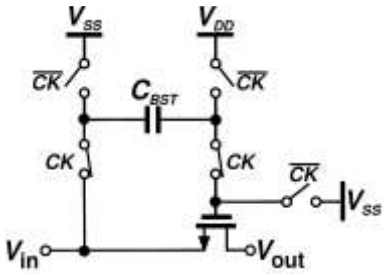


Fig. 3. Bootstrapping/Constant – $V_{GS}$ Sampling

$$R_{ON} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{th})} \quad (6)$$

where $W$ and $L$ are the channel length and width of the sampling switch, respectively, $\mu$ is the mobility of the device, $C_{ox}$ is the oxide capacitance, $V_{th}$ is the threshold voltage of the MOS transistor, and $V_{GS}$ is the gate – source voltage drop.

For low resolutions, a conventional transmission gate may suffice. In cases where higher resolutions are required, however, special techniques are incorporated for linearity enhancement. The main technique used for linearizing the switches is bootstrapping [10, 11], or more physically, constant – $V_{GS}$ sampling. As the name implies, devising a circuit that ensures a constant $V_{GS}$ value across the sampling MOS switch makes $R_{ON}$ input signal independent, enhancing the linearity performance. The main idea of bootstrapping, shown in Fig. 3, is to pre – charge a capacitor during the hold phase, and plugging this capacitor as a floating battery between the MOS gate and source terminals during the sampling phase; thereby, minimizing $R_{ON}$, while maintaining it, ideally, at a constant value. For further linearity enhancement, one may increase the main MOS switch sizing for further reduction in $R_{ON}$, while using low leakage devices for better control over the capacitor charging/discharging behavior.

In designing bootstrapping circuits, the main design considerations are minimizing the leakage currents, so that the constancy of $R_{ON}$ is preserved, and avoiding voltage stresses over any of the devices.

### C. Comparator

In SAR ADCs, comparators are responsible for comparing the sampled analog input voltage with the successive DAC outputs and feeding back the result to the SAR logic. For low – power consumption, dynamic/clocked comparators are usually used. The comparator nonidealities are its offset voltage, input referred noise, metastability, hysteresis, linearity, and kickback noise.

As with sampling offset error, the offset of the comparator can be easily corrected for in the digital domain, and does not result in harmonic distortion given the signal is not saturated. This observation, along with the inherent low operating speed in biomedical applications, relax the requirements on the sizing of the comparator input differential pair, reducing its input parasitic capacitances, which, indeed, reduces the nonlinear effects caused by the input capacitance of the comparator.

Metastability errors arise when the differential input to the comparator is sufficiently small such that the comparator is unable to push any of its outputs to one of the supply rails within the allowed time slot. Such errors can be minimized or even prevented by decreasing the length of the input differential pair transistors, enhancing its speed and regenerative performance.

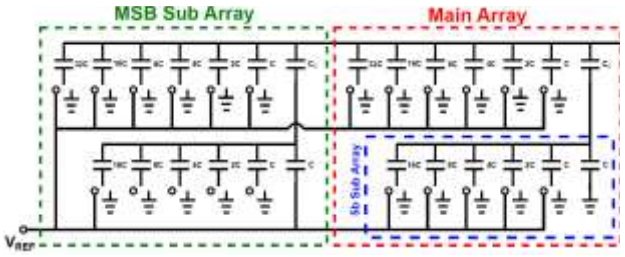


Fig. 4. 12 – bit BWA CDAC

Kickback noise is due to the signal – dependent capacitive coupling of the clock – switched nodes and output nodes with the non – zero resistance input node. This kickback can severely deteriorate the linearity performance of the ADC at resolutions greater than 10 bits. In [12], various techniques dealing with kickback noise have been outlined.

Finally, the standard deviation of the comparator input noise should be kept at a level below half LSB for proper operation. In [13], a simple method was outlined for estimating the noise standard deviation using transient noise simulations. In general, for noise reduction, one should increase the input differential pair sizing and increase the load capacitance at the expense of higher input parasitic capacitance and higher power consumption for the same speed [14].

### D. SAR Logic

Being fully digital, the SAR logic is optimized with regard to its power consumption and is simply implemented as a Johnson counter and a shift register. This conventional approach is superior, in power terms, over non – redundant combinational logic, and delay – line implementations [15].

## IV. Circuit Design Details

This Section applies the aforementioned systematic design procedure in Section III to design a 12 bit SAR ADC operating at 1 kS/s.

### A. Internal DAC

To reduce the total input capacitance, and hence the CDAC dynamic switching power, the BWA CDAC topology [9] had been chosen. Shown in Fig. 4, the CDAC is split into a 5 bit sub – CDAC and a 7 bit main – CDAC connected with the attenuating capacitor $C_C$. The MSB is split into its own array for further reduction in the area and capacitance spread. The total of 12 bits is divided into a 7 – bit main CDAC and a 5 – bit sub – CDAC array. For BWA CDACs, the DNL and INL requirements impose a limit on the unit capacitance given by [16]:

$$\sigma\left(\frac{\Delta C_U}{C_U}\right) = \frac{A_C}{\sqrt{C_U}} \le \frac{1}{2\alpha 2^{3N/4}} \quad (7)$$

where $A_C$ is a technology parameter defining the unit capacitance mismatch:

In the used 65 – nm CMOS technology, $A_C$ is equal to 0.005 while $C_U$ is in femto – Farad units. Based on (7), a unit

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capacitance of 26 fF is large enough for meeting the static linearity requirements with 68% yield. A minimum unit

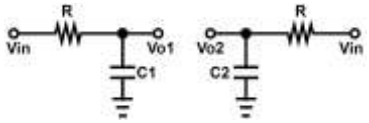
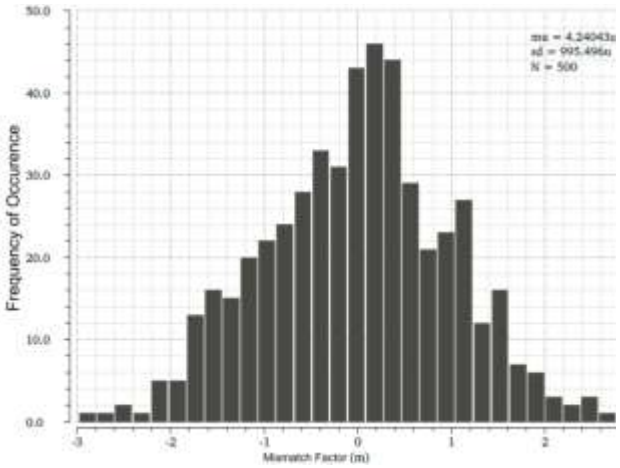



Fig. 5. Mismatch simulation setup




capacitance of 51.16 fF was used, however, as imposed by the technology kit. Fig. 5 shows the mismatch simulation setup. Under mismatched condition, $C_1$ and $C_2$ will differ in value, and the relative mismatch can be calculated using:

$$\sigma\left(\frac{\Delta C}{C_U}\right)=\frac{1}{\sqrt{2}}\sigma\left(\frac{C_2-C_1}{C_{1,2}}\right)=\frac{1}{\sqrt{2}}\sigma\left(\frac{BW_{Vo1}}{BW_{Vo2}}-1\right) \quad (8)$$

where the square root of 2 factor accounts for the differential operation and $\Delta C/C_U$ is the mismatch factor. Based on 500 Monte Carlo simulation runs, the histogram shown in Fig. 6 is obtained. The shown value of 0.1% neglects the differential nature; hence, the correct value for the standard deviation is 0.07%, which is less than the necessary standard deviation of 0.098% calculated from (7). The total input capacitance is 6.55 pF which satisfies the noise requirements, and imposes a loading capacitance on the sampling circuitry.

### B. *Sampling Switches*

To achieve the high resolution of 12 bits, the bootstrapped switch presented in [10], shown in Fig. 7, is used. *M5* and *M6* are responsible for charging *C3* during the hold phase. To avoid forwarding unnecessary junctions, *M5* is implemented using an NMOS device rather than a PMOS one, necessitating a gate voltage beyond the supply rails to turn ON. The Nakagome charge pump formed by *M3*, *M4*, *C1*, and *C2* is used for such purpose. *M2* is the main sampling transistor while *M1* is a dummy switch for charge injection error reduction. The remaining switches are responsible for connecting *C3* across the *G – S* terminals of *M2* during the sampling phase, and disconnecting it during the hold phase. *M11* is used as a shielding device to avoid stressing *M12*. Loaded by the CDAC total capacitance of 6.55 pF, the bootstrapped switch achieves an SNDR of 87 dB, equivalent to 14 bits of resolution. All switches were implemented using high – voltage low – leakage

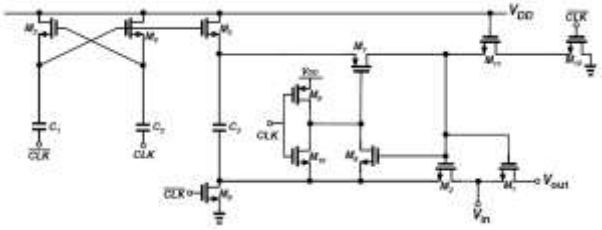


Fig. 7. Bootstrapped sampling switch.

devices.

### C. *Comparator*

For reduced power consumption, the conventional strong – Arm dynamic comparator [14] is chosen. For kickback noise suppression, a preamplifier was used to shield the CDAC output node from the aggressive switching action at the input of the comparator. PMOS topology was used for better supply rejection ratio. Fig. 8 shows the circuit implementation of the comparator and the pre – amplifier.

### D. *SAR Logic*

The SAR logic is simply a Johnson counter followed by a shift register. The logic circuitry is shown in Fig. 9.

## V. Simulation Results and Perfromance Summary

The implemented ADC is tested using a 498.046875 Hz single – tone input signal sampled at 1 kHz. The implemented SAR ADC, designed in a 0.65 – nm CMOS technology, shows an ENOB of 11.6 at a power consumption of 354 nW, corresponding to a Walden FoM of 114 fJ/conversion – step and a Schreier FoM of 161.3 dB which are excellent FoMs given the conventional circuitry used. The total occupied area is 0.24 $mm^2$. Table I shows the power consumption breakdown, Fig. 10 shows the output waveform power spectral density

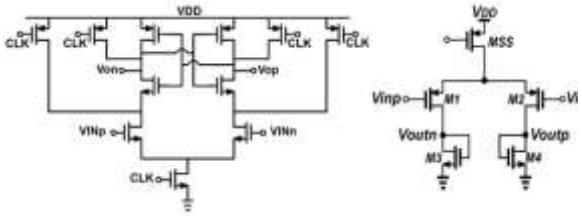



Fig. 8. Dynamic comparator (left) and pre – amplifier (right).

(PSD), and Fig. 11 shows the layout of the ADC.

## VI. Conclusion

The paper presented a systematic design procedure for designing SAR ADCs for bio – medical applications. The procedure identifies the main non – idealities of the ADC sub – circuits along with systematic design techniques for meeting the required specifications. The proposed procedure was adopted and a 12 bit SAR ADC was implemented in 65 – nm CMOS for bio – medical sensor nodes. Operating at 1 kS/s, the

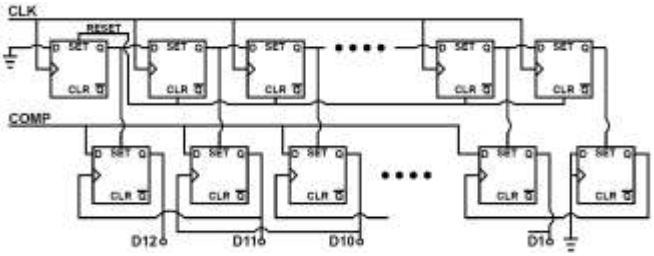


Fig. 9. SAR Logic

ADC consumed 354 nW from a 1.2 supply voltage, achieving an ENOB of 11.6 bits. The ADC has a Walden and Schreier FoMs of 114 fJ/conversion – step and 161.3 dB, respectively.

TABLE I. POWER BREAKDOWN

| *Block* | *Power (nW)* | *Power Percentage %* |
|---|---|---|
| Clocking | 22.5 | 6.36 |
| SAR Logic | 30.84 | 8.72 |
| Sampling Switches | 28.26 | 8 |
| CDAC Switching | 19.31 | 5.26 |
| Pre – amplifier | 251.16 | 71 |
| Comparator | 1.61 | 0.46 |
| Total | 353.7 | 100 |

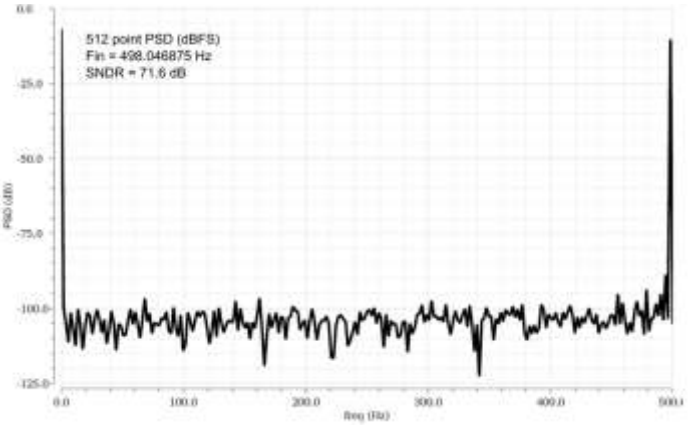


Fig. 10. 12 – bit ADC output PSD (dBFS)

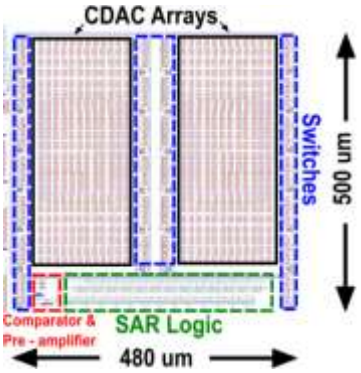


Figure 11. 12 – bit SAR ADC Layout

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