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Implementation of Stacked-CMOS Inverter based TIQ Comparator for FADC.

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***Abstract*—**A Threshold Inverter Quantizer (TIQ) is suggested in this paper for implementing a 3-bit, 1.2V Flash Analog to Digital Converter (FADC). A Stacked-CMOS Inverter based Threshold Inverter Quantizer (TIQ) is used for implementation of Comparator section in the Flash ADC; the comparator operates on different reference voltages, which is achieved by systematic variation of W/L ratio of each stacked CMOS TIQ comparator. Proposed design is simulated on Empyrean EDA tool with SMIC 65nm Technology. The power dissipation of ADC simulated at 1.2V Vdd for 1fF capacitive load over input frequency range of 1 Hz to 1 MHz is observed as 5.98µW; which is about 70 % lesser than that of conventional CMOS TIQ based Flash ADC.

Keywords*-*FADC, CMOS, ADC, TIQ, MUX, TM2B.

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I. INTRODUCTION

In modern high speed, digitized, battery operated handheld devices like mobile phones, cameras, and bio-medical devices etc. Analog to Digital Converters (ADCs) are mostly used as a part of system, instead of a separate circuit used for data conversion [1].This use of ADC emerges a need to minimize the power dissipation. Conventionally the power is reduced by reducing supply voltage and reducing switching activityetc but it is not sufficient for the recently developed power hungry devices[2-8].

Prime use of Analog to Digital Converter (ADC) is for signal conversion, which is carried out in two phases; Quantization and Coding of the analog input signal.Depending upon the different architectures ADCs are broadly categorized as Flash type, Pipelined, Sigma-Delta, Dual Slope, and Successive Approximation ADC; among these categories Flash type ADC is utilized for the high speed application; but its main drawback is its power hungry nature, which is a prime concern to the designers [2-8].

The proposed work discusses about implement a Flash type ADC using stacked-CMOS Inverter Threshold Inverter Quantizer (TIQ) comparator as an alternative of conventional CMOS logic which has increase in power dissipation as the switching is increasing and the technology is shrinking further. The TIQ comparator is intentionally used here to achieve faster conversion rate and low power consumption.

II. THE FLASH ADC ARCHITECTURE

Two-stage Flash Type ADC architecture prototype is shown in Fig 1. First section of ADC comprises of the comparator which is implemented using stacked CMOS TIQ. Output of the first section that is comparator is available in thermometric code format and is needed to be converted in binary code for that purpose Second section is used. The Second Section is Thermometric to Binary Code Converter (TM2B) implemented using 2:1 multiplexer, used to convert the output of the comparator stage to the corresponding binary code, which will be used as the output of the ADC. [9]

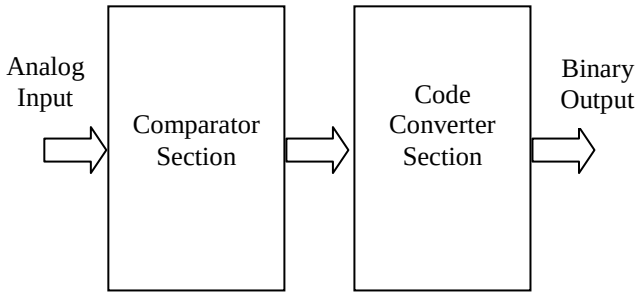

Fig1. Two Stage Flash ADC Architecture Prototype.

III. THE TIQ COMPARATOR

This Most critical section in the Flash ADC architecture is a comparator. Its role is to convert analog input voltage into logic 1 or logic 0 by comparing it with the reference voltage. Architecture of the flash type converter is developed by different comparators such as differential amplifier latch; auto zeroed sequentially sampled type, dynamic type, Threshold Inverter Quantizer (TIQ) and Quantum Voltage (QV) comparator [2-8].

Faster analog to digital conversion is achieved by TIQ comparator, which is designed using stacked-CMOS inverter logic as shown in Fig 2, comprises of cascaded stages of inverter, includes the gain booster stage to maintain the same DC threshold level and linearity of TIQ comparator inbalance.

The analog input is quantized at comparatorsection by selecting desired threshold voltage (Vth) of the inverter as and is approximately given by the following equations [6].

$$Vth = \frac{|Vtp| + Vtn\sqrt{(Kn/Kp)}}{1+\sqrt{Kn+Kp}} \quad (1)$$

$$Kn = \left(\frac{W}{L}\right) n\ \mu n\ Cox \quad (2)$$

$$Kp = \left(\frac{W}{L}\right) p\ \mu p\ C \quad (3)$$

Where $V_{tp}$and V_{tn} are the threshold voltages of PMOS and MOS transistors respectively and μ_p and μ_n are the mobility of PMOS and NMOS transistors respectively.

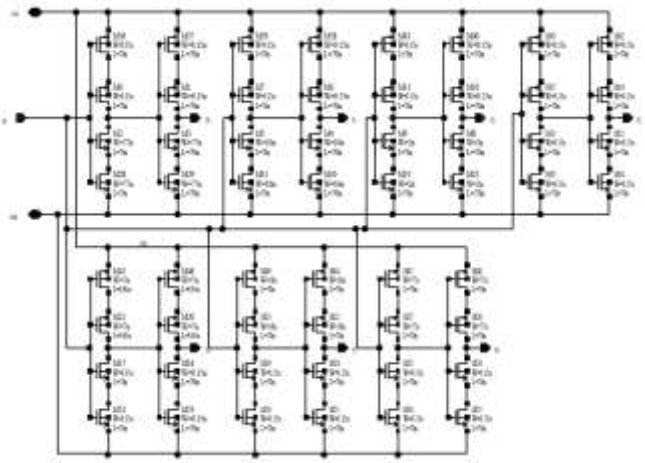

Fig2.Schematic of Stacked-CMOS TIQ Comparator stage.

To obtain desired switching voltage(V_{th}) of a specific comparator the transistor size of the inverter is varied systematically. The length and the width of PMOS and NMOS are varied in order to manage the preferred switching voltage [11]. The number of stages of inverter required to implement TIQ depends on bit size of the ADC to be implemented and calculated by following equation,

$$\text{No. of Inverter Stages} = 2^n - 1 \quad (4)$$

Where n = no. of bits for which ADC to be implemented.

Here a 3-bit ADC is to be implemented for that seven (2^3-1 = 7) stages of such inverters are required.

Simulated waveforms of such TIQ comparator with varied length and width of transistors to obtain desired switching voltage (V_{th})is shown in Fig3 and Fig 4.

Fig. 3 depicts the transient analysis of proposed TIQ comparator with analog input of 1 KHz frequency and 1.2 V, from the Fig. it is observed that the threshold level of each inverter is different and as per the requirement of the ADC comparator.

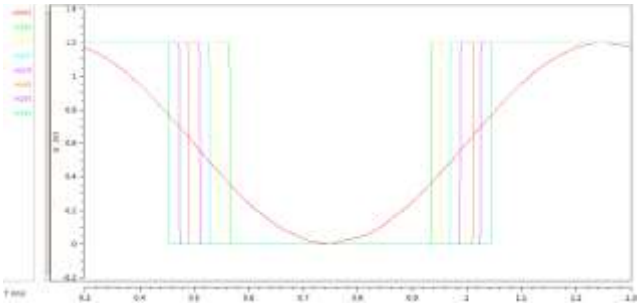

Fig.3.Transient analysis of TIQ Comparator stage.

Effect of variation of transistor sizes of an inverter can also be observed in the Fig. 4, where DC input voltage Vin is varied from 0V to 1.2V with linear step of 0.1V and the desired reference voltage is obtained for the functioning of TIQ comparator.

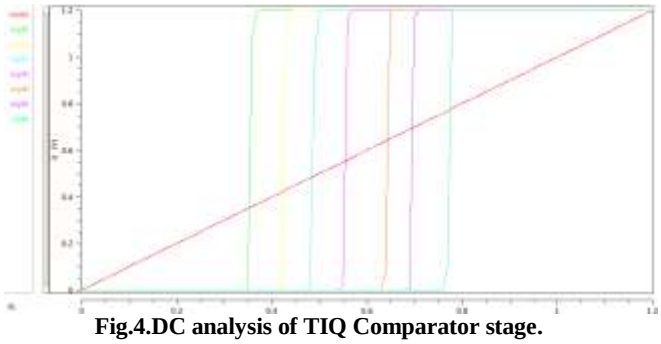

Fig.4.DC analysis of TIQ Comparator stage.

IV. CODE CONVERSION SECTION

Second section of FLASH ADC architecture is a code converter section. Thermometric to Binary Code Converter (TM2B) is implemented to convert the output of the comparator section to its corresponding binary equivalent code, which will be used to mark the output of the ADC. The easiest method for implementing Thermometric to Binary code converter is by using a binary encoded ROM [13]. Another method for implementing TM2B converter is by Wallace tree [9]. In afterward stages of development fat tree converter was utilized [15].

This work implements TM2B converter using 2:1 multiplexer, as it has several advantages such as low circuit complexity and low power consumption [16-18]. Schematic for implemented TM2B converter (7 to 3 line) is as shown in Fig. 5.

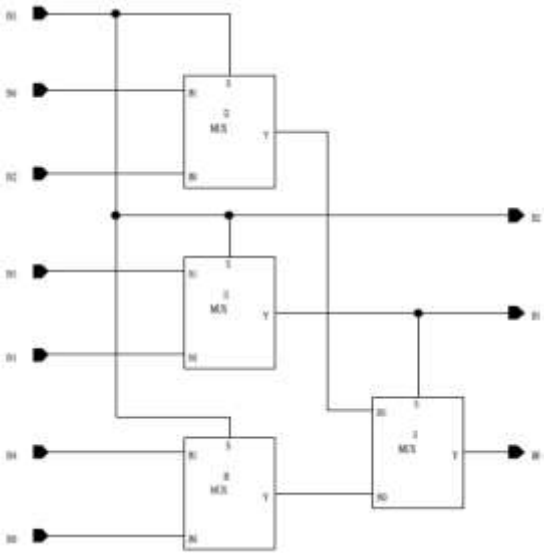

Fig. 5. Schematic of Thermometric to Binary code Converter.

TABLE 1 defines the operation of the code converter section. Each row publicized in the table is a valid input code obtained from comparator section and its equivalent 3-bit binary output, considering these values and equations based on these values TM2B converter is implemented as Shown in Fig. 5. There are total 8 valid inputs and 8 corresponding

binary output codes are illustrated in the table to represent the 3-bit Flash ADC [8].

TABLE 1 Thermometric to Binary Code Conversion Truth-Table

Thermometric Code							Binary Code		
Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

V. SIMULATION RESULTS

The proposed Flash type ADC is simulated for stacked-CMOS TIQ comparator on Empyrean EDA tool using SMIC 65nm technology. Transient analysis and DC sweep analysis is carried out at load capacitance of 1 fF, obtained simulation results are as shown in Fig. 6 and Fig. 7.

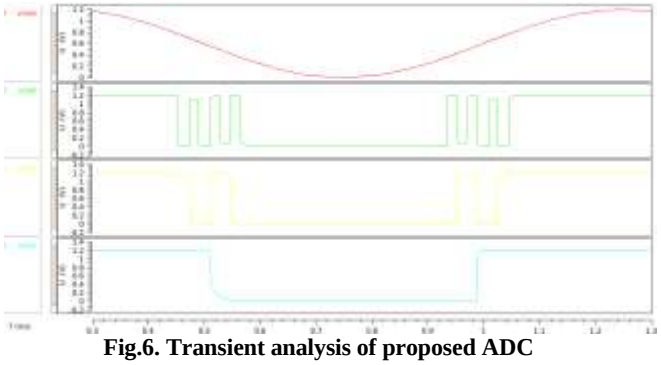

Fig.6. Transient analysis of proposed ADC

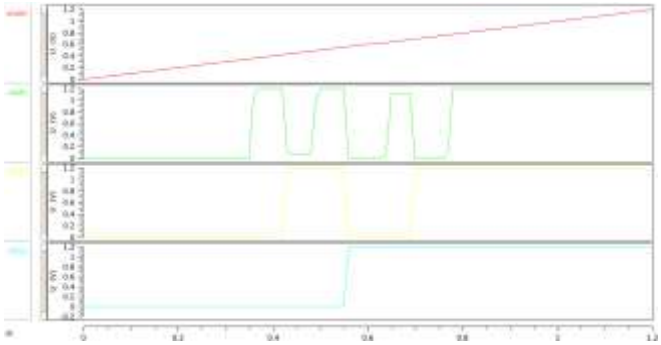

Fig.7. DC sweep analysis of proposed ADC

From Fig. 6 and Fig. 7 it is noticeable that input Vin is varied from 0 to 1.2V in linear steps, and output bits b0, b1 and b2 are observed; which are the equivalent binary output of the input voltage Vin depending upon the threshold voltage calculated through systematic variation of transistor sizing and observed as 000,001,010,011,100,101,110,111 at a specific time interval.

To perform the comparative analysis on power consumption the ADC is simulated with conventional CMOS inverter TIQ Comparator and stacked-CMOS inverter TIQ comparator and the results obtained are as shown in Fig. 8.

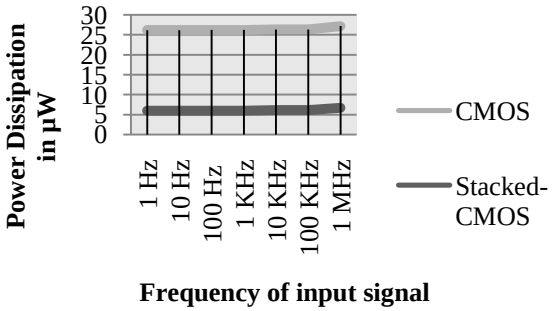

Fig.8. Power dissipation comparison

Fig. 8 depicts that the frequency of input signal is varied from 1Hz to 1MHz, the power dissipation for both the methods does not show any significant change over the range of input frequency while doing this analysis the voltage of input signal is kept at1.2 V and the transient analysis is performed at capacitive load of 1fF.

VI. CONCLUSION

In this work, flash type ADC is designed and simulated using stacked-CMOS inverter based Threshold Inverter Quantizer. The key intent of this work is to reduce the power dissipation in an ADC. This proposed design illustrates the total power dissipation of ADC simulated at 1.2V Vdd for 1fF capacitive load over input frequency rangeof 1 Hz to 1 MHz is observed as 5.98µW; which is about 70 % lesser than that of conventional CMOS TIQ based Flash ADC

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