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Adaptation in Optical Transport Networks with FPGA-Based GLDPC Decoding

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ABSTRACT

Since LDPC codes are well-known for their strong error correcting capabilities, this design intends to use them to make OTNs more adaptable and reliable. Because of the high-speed processing and adaptability offered by the FPGA implementation, it is possible to make real-time modifications to transmission conditions and data rates. In this research, we look examine how well the Generalized Low-Density Parity-Check (GLDPC) codes that have been suggested work on an FPGA platform. Three essential parts make up the FPGA system: a circuit for error counting, a GLDPC decoder, and a noise generator with a Gaussian distribution. To create white Gaussian noise samples, the Gaussian noise generator uses the Box-Muller algorithm in conjunction with two uniform generators based on Linear Feedback Shift Register (LFSR). Based on our findings, the proposed unified GLDPC decoder architecture is a practical option for next-gen high-speed fiber optical communications as it allows for variable net coding gains (NCGs) without an error floor at BER levels as low as 10-15.

Keywords: Gaussian, Transport Networks, Fiber, Signal, Parallel

I.INTRODUCTION

More bandwidth, more dependable transmission methods, and faster data rates are in increasing demand due to the development of communication networks. With their enormous bandwidth capacity, optical transport networks (OTNs) enable the worldwide interchange of information and have therefore become the foundation of contemporary telecommunications. The capacity of these networks to adjust to different transmission circumstances and data rates is crucial to their efficiency and dependability. For the network to keep performing at its best regardless of external influences like noise and signal deterioration, its capacity to adapt is crucial. An essential technique that enables such flexibility is Low-Density Parity-Check (LDPC) codes, which are a kind of error correcting coding. Their near-capacity performance and efficiency in error correction make LDPC codes excellent for use in OTNs, and they have attracted substantial attention as a result. Robert Gallager first proposed LDPC codes in the 1960s, but their computational complexity caused them to be originally disregarded. But with the rise of current computer power, and especially with the creation of Field-Programmable Gate Arrays (FPGAs), LDPC codes are all the rage again. Due to their reconfigurable nature, field-programmable gate arrays (FPGAs) offer a strong foundation for LDPC code implementation, allowing for real-time scheme modifications to adapt to optical network circumstances.

There is no easy way to include LDPC codes into OTNs. Due to the ever-changing nature of modern communication, coding schemes need to be able to dynamically adjust to varying data speeds. To meet this demand, generic LDPC codes were developed, which allow the parameters to be tuned to the specific requirements of the network. By building upon the standard LDPC structure, generalized LDPC codes make it possible to dynamically alter the code length and rate. Since the transmission rate can have to be adjusted depending on traffic load, channel conditions, and other network dynamics, this flexibility is vital for rate-adaptive OTNs. These generalized LDPC codes have several benefits when implemented on FPGAs. For LDPC codes' high-speed decoding procedures, FPGAs' well-known parallel processing capabilities are required. Furthermore, field-programmable gate arrays (FPGAs) are perfect for implementing adaptive coding schemes because they can be reprogrammed to accept alternative code patterns without requiring hardware redesign. By adapting the error correction settings in real-time to real-world situations, network operators may maximize the performance of OTNs, ensuring data integrity and network efficiency.

Notwithstanding these benefits, there are a number of obstacles to overcome in the design and implementation of generalized LDPC codes for OTNs based on FPGAs. The decoding algorithms are quite complicated and resource-intensive, which is one of the main obstacles. Efficient

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hardware designs that can handle the computational burden without adding unnecessary delay are required for real-time processing and the iterative nature of LDPC decoding. The design also has to take into account the fact that generalized LDPC codes have different data rates and code length requirements, which increases the system's complexity. This project aims to produce an optimal FPGA architecture for rate-adaptive OTNs that can handle generalized LDPC codes in order to overcome these problems. Considerations of computational complexity, decoding speed, and design flexibility are all taken into account. In order to accomplish fast decoding while keeping the flexibility needed for current OTNs, the suggested architecture makes use of FPGAs' parallel processing capabilities. In order to make sure the system can handle the load of high-throughput optical networks, the research also investigates several optimization strategies like pipelining and parallelism to make the FPGA implementation more efficient.

Field-Programmable Gate Array (FPGA)

An FPGA, or Field-Programmable Gate Array, is a type of integrated circuit that can be configured by the user after manufacturing, making it highly versatile for a range of applications. Unlike fixed-function chips, FPGAs can be reprogrammed to perform different tasks, allowing designers to create custom digital circuits without the need for expensive and time-consuming manufacturing processes. FPGAs consist of programmable logic blocks and interconnects that can be configured to implement complex functions, from simple logic operations to intricate digital signal processing tasks. This re-configurability makes FPGAs ideal for prototyping, custom hardware implementations, and applications requiring flexibility, such as communications, signal processing, and AI. Their ability to be reprogrammed multiple times also allows for iterative design, making them a crucial tool in modern electronic design and development.

II.REVIEW OF LITRATURE

Sun, Xiaole & Djordjevic, Ivan. (2019) The findings show that SC codes outperform other codes of the same complexity when emulation is based on FPGAs. A coding-rate adaptation approach based on spatial coupling may be provided by the built unified structure for any template QC-LDPC code.

Zou, Ding & Djordjevic, Ivan. (2015) Our proposed FEC scheme combines a hard-decision FEC code with a non-binary LDPC code based on soft-decisions. The suggested NB-LDPC + RS provides an increased NCG of 11.9 dB at a post-FEC BER of 10^{-5}, with an overhead of 27.06%. With throughputs surpassing 100Gb/s, the suggested NB-LDPC codes are therefore excellent choices for soft-decision FEC in optical transmission systems.

Djordjevic, Ivan & Wang, Ting. (2014). Our findings suggest that it is possible to enhance GLDPC codes—codes that are created from many components—to get record coding improvements. Afterwards, we show that GLDPC coding may be used to describe a number of recently proposed LDPC code types, such as convolutional and spatially-coupled codes. This points to the possibility that GLDPC coding may be used as a basis for enhanced FEC, which will allow for optical transmission at very high speeds. If the optical channel changes, the error correction intensity may be adjusted via code-rate adaptation, which is especially well-suited to the proposed GLDPC code class.

Gho, Gwang-Hyun et al., (2011) A transmission approach that uses variable-rate forward error correction (FEC) codes to modify its rate is part of our proposal. The method keeps the symbol rate and signal constellation constant. The objective is to put a number on the distance-dependent change in viable bit rates for long-haul fiber networks. Using serially concatenated Reed-Solomon (RS) codes, the Forward Error Correction (FEC) system corrects errors. The inadequacy of the repetitive coding used beyond a distance of 3280 kilometers is likely the main cause of the gap's expansion. When regeneration stations are inconveniently located, rate-adaptive transmission may be a lifesaver for network coverage expansion. Networks are able to adapt to changes in traffic needs in this way. As optically switched mesh networks develop further, their significance is likely to grow, which in turn will cause signal quality to vary more.

III.ARCHITECTURE OF GLDPC DECODER

We verify suggested GLDPC codes on a field programmable gate array (FPGA) device. It’s an integrated circuit that can be programmed or configured after manufacturing to perform specific tasks or functions. FPGAs are highly versatile and can be used for a variety of applications, including digital signal processing, telecommunications, automotive systems, and more.

This platform consists of three components: A Gaussian noise generator, a GLDPC decoder, and an error counter circuit. It is analogous to many other platforms. The white Gaussian noise is generated by the Box-Muller method in conjunction with two Linear Feedback Shift Register (LFSR)-based uniform generators. A Linear Feedback Shift Register (LFSR) is a type of shift register used to generate sequences of binary numbers, which can appear random but are actually deterministic. It operates by shifting the bits in the register to the right, with the leftmost bit being fed by a linear function of the previous bits, typically implemented using XOR gates. The initial value in the register is known as the "seed," and

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the sequence generated by the LFSR will eventually repeat after a certain number of shifts, known as the "period."

The quantized log-likelihood ratios (LLRs), obtained by multiplying the resulting sample sequence by the AWGN standard deviation, are then supplied to the LDPC decoder. The GLDPC decoder employs a layered strategy with scaled min-sum updating rules with a constant Q Factor in this FPGA-based platform is a key performance metric that represents how well the system can handle noise and accurately decode the transmitted signal, with a direct influence on the bit error rate. Additionally, a maximum a posteriori (MAP) computation approach based on the BCJR algorithm is used for the local codes.

The BCJR algorithm, named after its inventors Bahl, Cocke, Jelinek, and Raviv, is a critical component in the field of error correction coding. This algorithm is designed to perform maximum a posteriori (MAP) probability decoding of convolutional codes, making it an essential tool for improving the reliability of digital communication systems. The algorithm operates in both forward and backward directions over the received signal, calculating the probabilities of various states at each step. This approach allows it to achieve optimal performance, particularly in scenarios where the transmission channel introduces significant noise and errors. The BCJR algorithm's ability to deliver highly accurate decoding makes it indispensable in applications requiring robust error correction, such as deep space communications and mobile networks.

It is important to note that the local codes are evenly distributed throughout the check nodes, which greatly simplifies the addressing issue of the local codes. The current variable used to verify the node message is directed to either a traditional check-node processor or a BCJR-based MAP processor, depending on the local code valid signal.

BCJR-based MAP decoder architecture

The MAP decoder implementation that makes advantage of BCJR may consist of three components. Figure 1 shows the three components of the system. The first section determines the likelihood of recursion in both directions, and here is where it all begins. The memory, namely $\boldsymbol{\nu}$ and β, is the second component. It contains the intermediate data. The final part, a combiner, computes the result. Given the time-varying properties of the trellis constructed from a block code, pre-storing selection signals in ROM is imperative. An acceptable feedback output to feed into the forward and backward recursion blocks may be selected by this approach. To maintain an acceptable level of latency and complexity, we have opted to replace the max-star operation with a max operation.

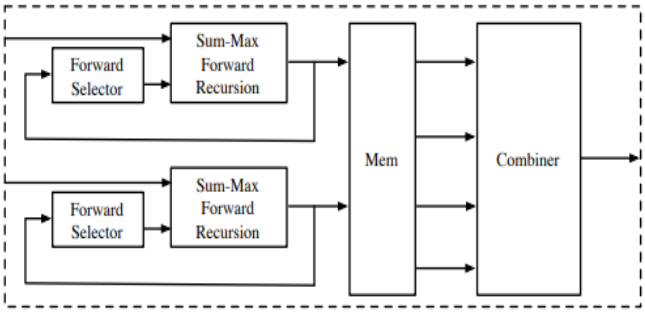

Figure 1: BCJR-Enhanced MAP Decoder Framework

Figure 2 provides more detailed information in addition to displaying the decoding of the (15, 11) Hamming code. The output $O7$ is produced by combining the updated and memory-stored first half of the forward and backward recursion with the current values of $\beta 7$ and $\beta 8$. From then on, every cycle will provide two outputs: one will be the result of combining the current $\boldsymbol{\nu}$ with β from memory blocks, and the other will be the result of combining β from the memory itself. Should this strategy prove effective, the overall latency will be lower than the total of the local code length plus the delay resulting from input and output serial/parallel conversions. Lastly, the suggested GLDPC approach shows great promise due to the relatively low complexity of the MAP decoder.

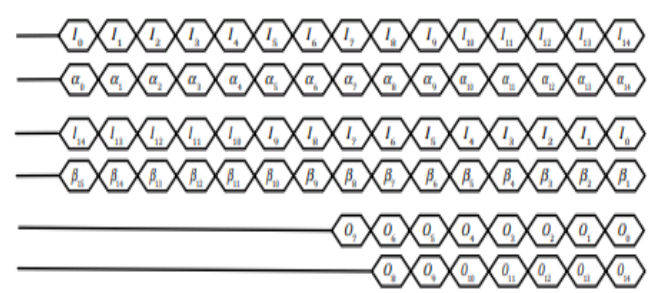

Figure 2: BCJR Processor Timing Diagram

IV.EXPERIMENTAL RESULTS AND DISCUSSION

Starting with an efficient LDPC code, a quasi-cyclic (3, 15)-regular, girth-10 (34635, 27710, 0.8) binary LDPC code, and using a basic (15, 11) Hamming code as the component code, it will be demonstrated that the suggested rate adaptive GLDPC codes are advantageous. We decided to set the parameter d which represents different levels of redundancy in the range {∞, 127, 63, 31, 15} to make implementation easier. This range corresponds to code rates of {0.8, 0.7953, 0.7906, 0.7807, 0.7601}. The maximum number of iterations may be set to either 10 or 15, and the precision of LLRs, the variable-to-check message, and the check-to-variable message are all set to 5-bit and 6-bit, respectively. Figure 4 shows the results after 15 iterations, while Figure 3 shows the

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results after 10 iterations, both in relation to the Q factor and the bit error rate (BER). With a net coding increase of 11.71 dB after 15 iterations and 11.61 dB after 10 iterations, the planned mother clearly converges quickly. Figure makes it easy to see that BER performance improves with decreasing d, allowing for coding rate fine-tuning.

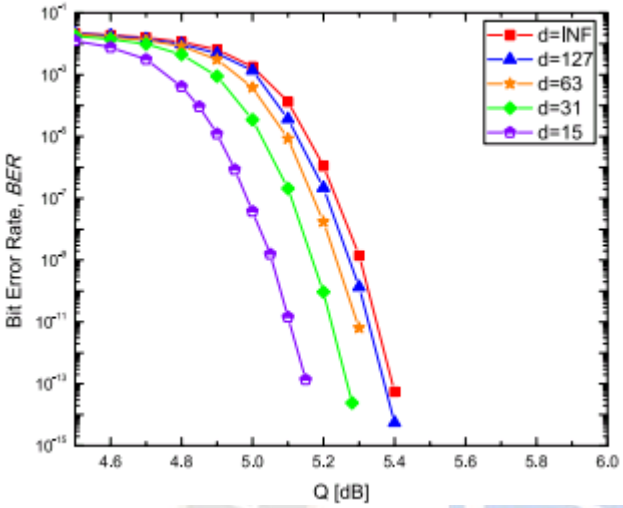

Figure 3: BER Performance vs. Q Factor for 10 Maximum Iterations

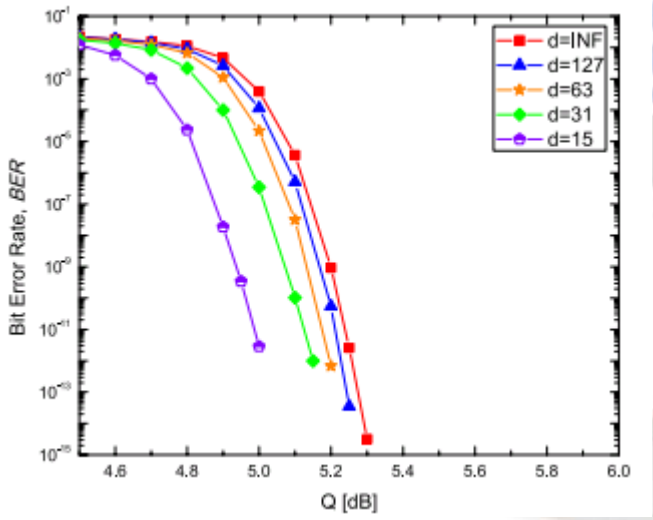

Figure 4: BER Performance vs. Q Factor for 15 Maximum Iterations

V.CONCLUSION

Ultimately, rate-adaptive optical transport networks (OTNs) on FPGA platforms have advanced significantly with the application of generalized Low-Density Parity-Check (LDPC) codes. Real-time, high-speed decoding must be accomplished if contemporary communication systems are to continue operating effectively and dependably. This method makes use of the parallel processing power and inherent flexibility of FPGAs. The study's conclusions demonstrate the significant potential of FPGA-based solutions for enhancing network performance through fast adaptation to variations in data rates and transmission conditions. The proposed FPGA design handles the complexities of LDPC code decoding algorithms, offering a scalable and adaptable solution to the evolving demands of OTNs. Because optical networks have the ability to instantly alter the coding scheme, data can remain intact even in the event of external circumstances changing. This design has the potential to significantly enhance OTN capabilities, which might lead to new advancements in flexible, high-speed communication networks, if it performs as planned.

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