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Design and Implementation of High Speed Bi-directional Transceiver for Low Power Applications

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***Abstract*—**In this paper, a new bi-directional transceiver has been proposed for high speed signaling. The new proposed transceiver architecture has two modes of operation namely, the transmitter and the receiver. Transceiver on either side supports two way communications via same link. Since high transimpedance gain over a large bandwidth in the receiving mode, the signaling current can be reduced to a very low value. The proposed circuit is designed in 90nm technology with the supply voltage of 1.8V.

Keywords*—transciever; bidirectional*.

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I. INTRODUCTION

This electronic document propose a high speed signaling architecture using bi-directional transceiver in 90nm technology with the supply voltage of 1.8V. To enhance high system performance, global interconnects to data transmission from on digital end to another end in system on chip or network on chip have to be very fast and power efficient [1]. Modulated signaling systems, loss compensation by negative impedance converters, pre-emphasis, pulse width modulation techniques are used to increase the bandwidth of the links. But these mentioned techniques are less energy efficient. This paper proposes a new technique of high speed bi-directional transceiver [2]. The proposed transceiver can either act as a transmitter of a receiver since it uses a same interconnects for a bi-directional communication. This in turn has very low small-signal impedance in both directions and enhances link bandwidth to the large extent. It has a very high transimpedance gain over a large bandwidth, which reduces the required signaling current to a very low level in comparison to the existing resistive termination [3]. The main scope focuses on the design and verification of bidirectional transceiver using 90nm CMOS technology. Transceiver design is done by choosing proper aspect ratio for each transistor such that all transistor remains in saturation region and proper selection of reference current helps in determining correct aspect ratio.

II. RELATED WORK

The multicore system network on chip uses an efficient high speed data sharing among its cores. The typical method is used for data communication from one core to another to divide the interconnect into various segments [5]. Repeaters are inserted between them to boost the performance of the interconnect. Many techniques exist in the past to optimize the area and proper placements of repeaters. Increase in the complexity leads to supply noise, jitter, skew, cross-talks and various other issues leading to failure. In another technique, several signaling schemes is used to transmit the high speed data through the lossy global interconnect [6]. In some cases preemphasis circuits are used to reduce the noise effect. These techniques mentioned realize high speed transfer of data over a long on chip interconnect.

A. Gain

Gain term is used to measure the ability of two port circuit to increase the power or amplitude of the signal. Logarithmic decibel is used for analysis. The current gain and voltage gain is given by equations 1 and 2 respectively.

$$\text{gain} = 10\log\frac{\frac{V_{\text{out}}^2}{R_{\text{out}}}}{\frac{V_{\text{in}}^2}{R_{\text{in}}}}\ \text{dB} \quad (1)$$

$$\text{gain} = 10\log\left(\frac{I_{\text{out}}^2 R_{\text{out}}}{I_{\text{in}}^2 R_{\text{in}}}\right)\ \text{dB} \quad (2)$$

B. Bandwidth

Bandwidth signifies the measure of the width of a range of frequencies, measured in hertz.

C. Slew Rate

The rate of change of voltage per unit time is given by the slew rate of the electronic system expressed as given in the equation 3.

$$\text{SR} = \max\left(\left|\frac{dv_{\text{out}}(t)}{dt}\right|\right) \quad (3)$$

III. TRANSIEVER DESIGN

The design of the bi-directional transceiver system is done using cadence tool gpdk90nm technology.

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709 – 712

A. *Transmitter Design*

The high efficient low-voltage differential signaling (LDVS) transmitter is used for the design of the transmitter. The transmitter architecture in CMOS design is shown in figure 1.

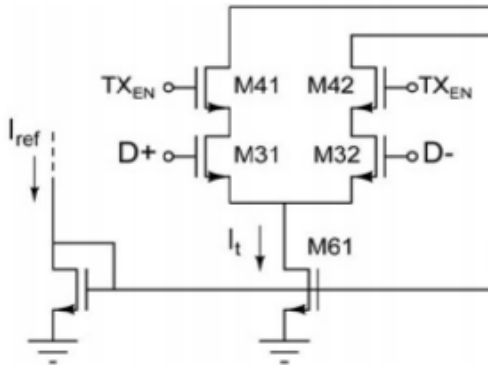

Figure 1. Transmitter Design.

Transmitter has four transistors function as the current mirror for stabilization of current. Depending on the data need to be send either M31 and M32 or M41 and M42 is switched ON. This configuration provides very low impedance since the signaling techniques has less cross-talk.

B. *Receiver Design*

Figure 2 gives the design of receiver in the bi-directional system. The main feature of the receiver is the very low small-signal input impedance and high transimpedance gain. Transistors M1 and M2 are cross coupled and drive resistors R1 and R2 respectively.

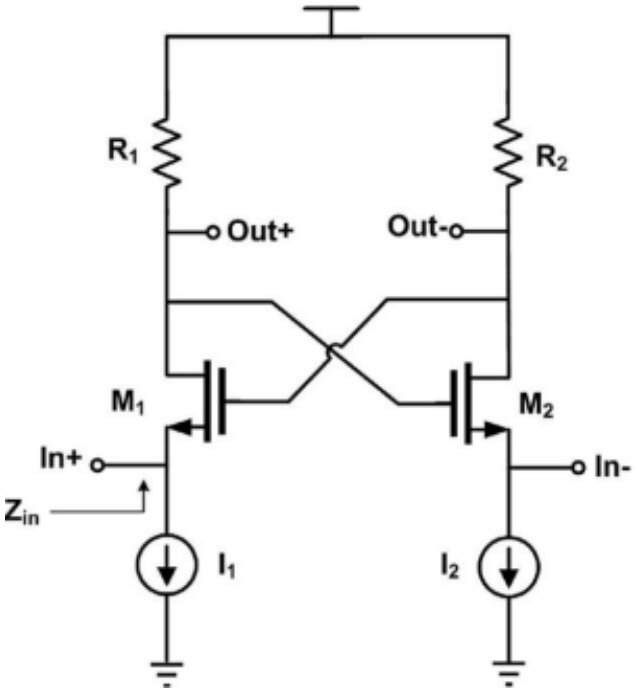

Figure 2. Receiver Design.

C. *Implementation*

Figure 3 show the schematic design of bi-directional transceiver. Transistors M7 and M8, M4 and NM2 forms differential amplifier circuit. Transistors M7 and M8 acts as switch. Current variation and in turn rise in output voltage is seen by controlling the gate voltage of the transistor M4 and NM2. Transistors M1 and M0 acts as a latch which strengthen the output and transistors M10, NM5, M2, M3 act as a current mirror.

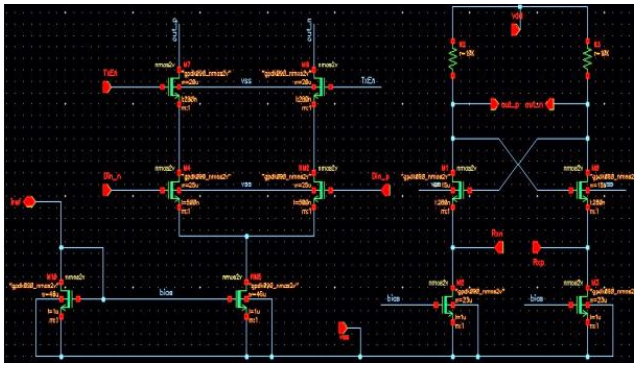

Figure 3. Bi-direction Transceiver.

D. *Design Specifications*

The current flowing through the transistors M7 and M4 and M8 and NM2 is 100µA since the tail current is 200µA. The aspect ratio for these transistors is determined to operate in saturation region. For latch transistor minimum aspect ratio is selected for low power analysis. The aspect ratio of current mirror M10 and NM5 is chosen to be 46. Since Transistors M2 and M3 acts as current mirror and current flowing through them is 100µA, the aspect ratio is half of the first current mirror part i.e., 23.

1. Slew rate = 20V/microsecond
2. Capacitor = 5pf
3. Vds= 200mV
4. µnCox = 217µV
5. Gain > 1

E. *Results and Waveforms*

In Simulation DC, Transient and AC analysis are performed and the results are tabulated. Figure 4, 5 shows differential voltage of the transiever, peak to peal voltage of the transceiver respectively. The differential input with amplitude of 170mV and offset voltage of 900mV is applied to transimitter introducing the delay of 400ps. Input signal is processed and strengthened at the transmitter block. The receiver in the transceiver block enhances the information form peak to peal voltage of 338.5mV to 900mV.

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709 – 712

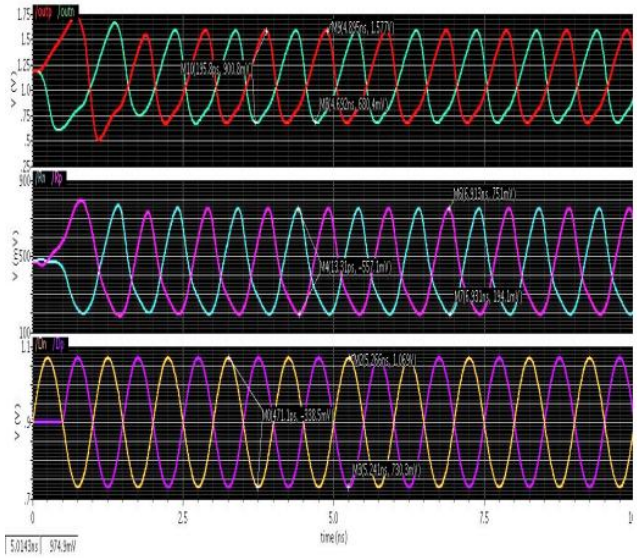

Figure 4. Differential voltage of the transceiver

The peak to peak voltage at input end of the transmitter is named by Data_pp, and input of receiver by Txout_pp and output of receiver by Rxout_pp. Table 1 gives the transmitted and received voltage. Transmitted and Received signal is almost similar with some loss of information due to atmospheric and electronic noise introduced.

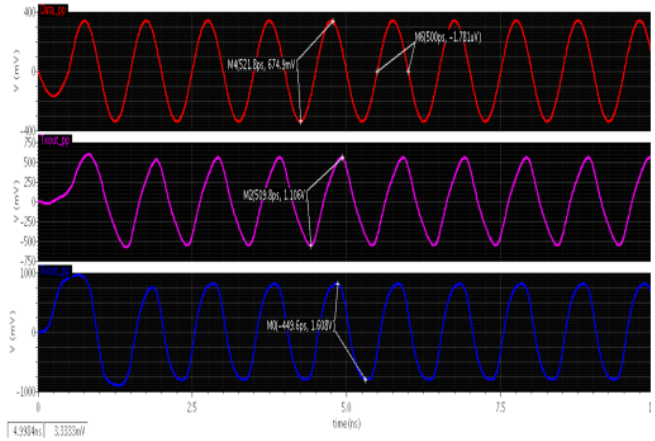

Figure 5. Peak to peak voltage of the transceiver.

Table 2 gives the comparison of the technology and the signaling scheme. It clearly shows that as technology is advanced the energy dissipation is reduced under different techniques.

Tabe1: Voltage at transmission and reception

Signal Type	Voltage
Data_pp	974.9mV
Txout_pp	1.106V
Rxout_pp	1.608V

Table2: Comparison of Technology

Technology(nm), Supply Voltage(V)		Signaling scheme	Data rate(Gbps)	Energy(pJ/b
350	2.5	Hybrid current mode	1	5.80
180	1.8	Capacitive driven pre-emphasis	1	1.05
180	1.8	Loss compensation	3	2.00
130	1.2	Pulse width pre-emphasis	3	2.00
90	1.8	Pre-emphasis and equalization	6	0.63

IV. Conclusion and Future Scope

The proposed transceiver can be used as a transmitter or receiver and hence supports bi-directional communication for high speed communication for low power applications. It shows very low impedance in both directions. The signaling current is reduced to a very low level and gain at receiving end is high. In future, design can be implemented for bit rate more than 14Gbps.

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