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603 – 608

Multi-Level Inverter For Domestic Application

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***Abstract*-**In this paper both DC-DC Converter and multilevel inverter have been proposed. The proposed multilevel inverter with appropriate gate signals generates seven level AC output voltage. Also, with the implementation of Low Pass Filter, the output voltage's Total Harmonic Distortion is reduced. Not only switching losses but also voltage stress of switches can be reduced. With the help of Sinusoidal Pulse-Width Modulation (SPWM) switches of the inverters are controlled. Finally, a laboratory prototype has been implemented and from experimental results, the seven level output of implemented inverter can be inferred.

***Keywords*-** *THD, SPWM, FFT, MLI, MATLAB*

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I. INTRODUCTION

Due to recent advancements in technology, the power quality demand is increasing daily. Inverter is nothing but a power device that converts DC to AC with the help of power electronic switches. Whenever the loads vary, the output frequency and voltage should change accordingly in order to satisfy different nature and demand of loads. In recent years power equipment has increased rapidly. In order to limit the harmonic quality and equipment's power factor, several standards and regulations have been formulated. In industrial sectors the demand for power applications and the power device's specification are higher. IGBT features not only high power rating but also high voltage stress. But the problem with them is that they cannot operate at high frequency. Further complexity is more while designing gate driver circuits for IGBT's. But even at higher frequency MOSFET can be able to operate, but power rating is not as good when compared.

Both DC-DC Boost Converter and multilevel inverter has been presented. To achieve the required stepped level of output at the end of the load, multicarrier SPWM technique is used. Fig. 1 represents the block diagram of this project.

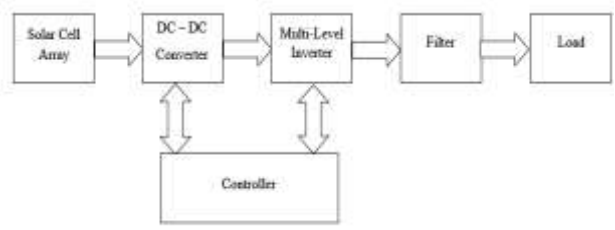

Figure 1. Block diagram of proposed system

II. PROPOSED SYSTEM

In this project, a general cascaded multilevel inverter using developed H-bridges has been proposed. This topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches. This gives the advantage of decreased complexity and overall inverter cost. The proposed topology generates the required 7-level voltage can be inferred both by simulation results and hardware prototype.

II. INDUCTOR DESIGN FOR PROPOSED BOOST CONVERTER

The design calculation are as follows:

Duty Cycle:

$$D = 1 - \frac{V_{in}}{V_0} = 1 - \frac{25}{48} = 0.4791$$

So fixing Duty Cycle to 0.5

Efficiency:

$$\eta = \frac{Pout}{Pin} = \frac{70}{60} = 0.85 \text{ or } 85\%$$

Input Current Ripple:

$$\Delta I_L = 20\% \text{ of } I_{in} = 2.8 * [\frac{20}{100}] = 0.56A$$

Output Voltage Ripple:

$$\Delta V_0 = 5\% \text{ of } V_0 = 48 * [\frac{5}{100}] = 2.4V$$

Capacitor:

$$C = \frac{I_0.D}{2.fs.\Delta V_0} = \frac{1.25 * 0.5}{2 * 20000 * 2.4} = 6.5\mu F$$

Inductor:

ISSN: 2321-8169
603 – 608

$$L = \frac{V_{in}.D}{fs.\Delta I_L} = \frac{25*0.5}{20000*0.56} = 1.11mH$$

III. SIMULATION

In this section of paper, both boost converter and inverter are simulated in MATLAB environment. The switches of the inverter are triggered using Multi carrier SPWM. The simulated results are as follows:

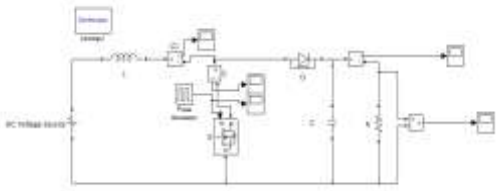

Figure 2. Boost converter

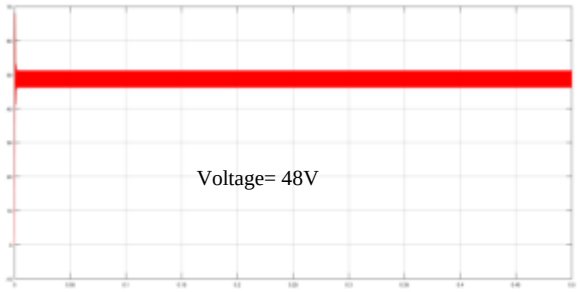

Figure 3. Output Voltage of Boost Converter

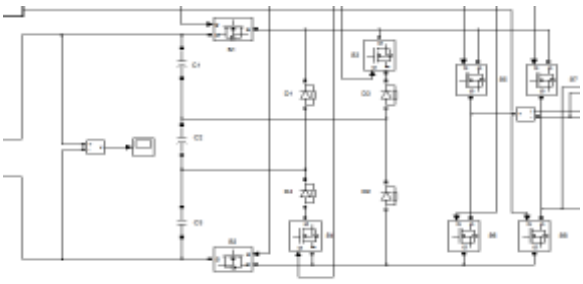

Figure 4. Seven Level Inverter

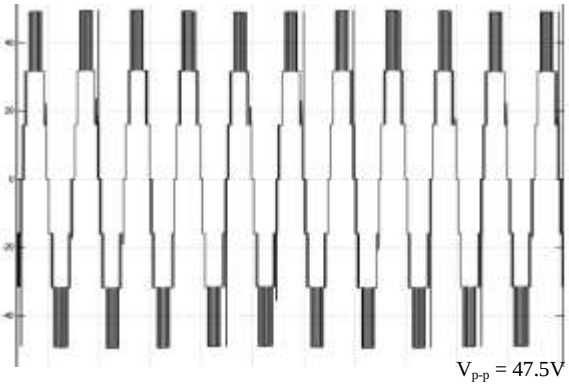

Figure 5. Output Voltage of Inverter

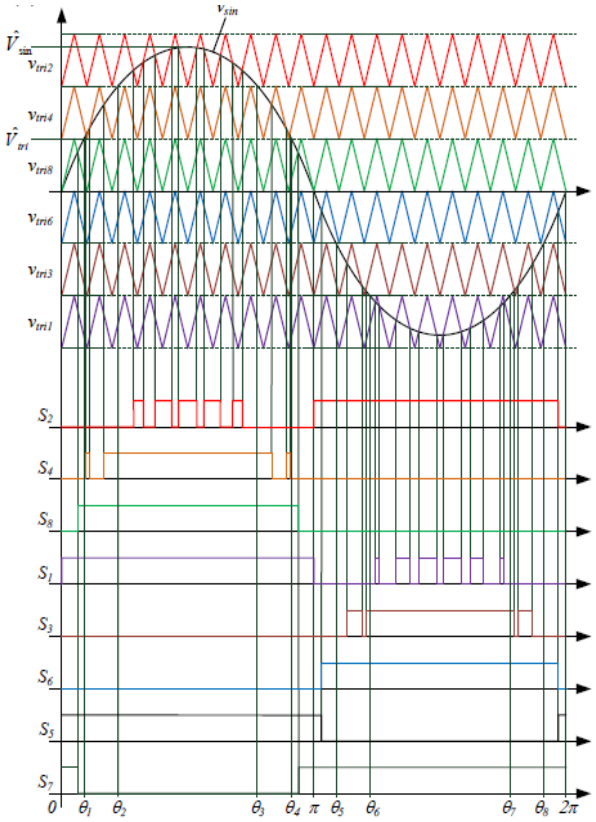

Figure 6. Reference sine wave, carriers, and control signals of switches.

Operating Principles:

The required seven voltage output levels (±1/3Vdc, ±2/3Vdc, ±Vdc, 0) are generated as follows:

1) C1 provides the required energy while switches S1, S5 and S8 are turned on. As a result, (1/3) Vdc is obtained across the output terminals. Fig. 7 explains about this mode.

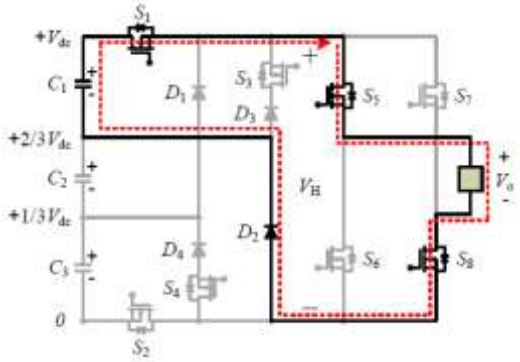

Figure 7. Mode1

2) C1 and C2 provides the required energy while switches S1, S4, S5 and S8 are turned on. As a result, (2/3) Vdc is obtained across the output terminals. Fig. 8 gives the pictorial representation of this mode.

 ISSN: 2321-8169
603 – 608

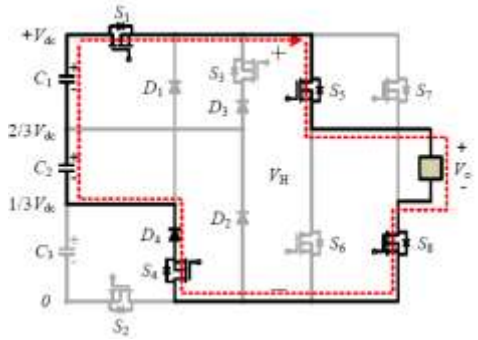

Figure 8. Mode II

3) All the capacitors C1, C2 and C3 provides the required energy while switches S1, S2, S5 and S8 are turned on. As a result, +Vdc is obtained across the output terminals. Fig. 9 shows operation of this mode.

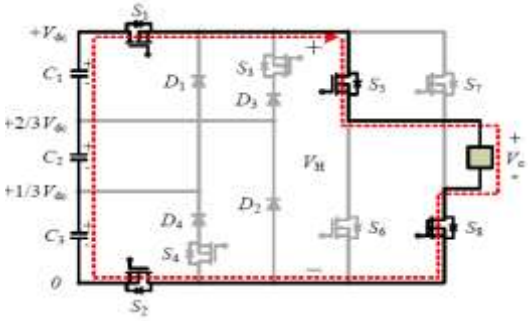

Figure 9. Mode III

4) C3 provides the required energy while switches S2 (turned at negative cycle), S6 and S7 are turned on. As a result, –(1/3) Vdc is obtained across the output terminals. Fig. 10 explains working of this mode.

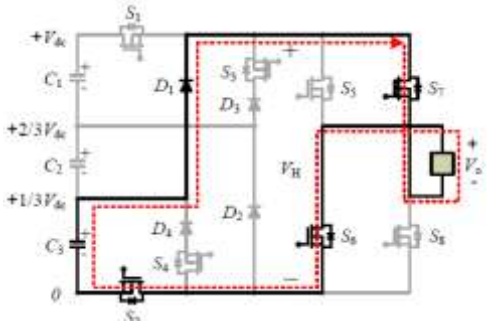

Figure 10. Mode IV

5) C2 and C3 provides the required energy while switches S2, S3, S6 and S7 are turned on. As a result, – (2/3) Vdc is obtained across the output terminals. Fig. 11 explains operation of this mode.

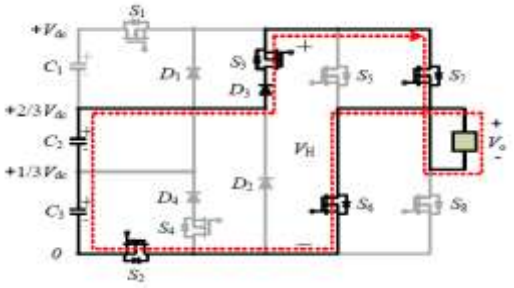

Figure 11. Mode V

6) C1, C2 and C3 provides the required energy while switches S1, S2, S6 and S7 are turned on. As a result maximum negative peak (– Vdc) is obtained across the output terminals. Fig. 12 explains about this mode.

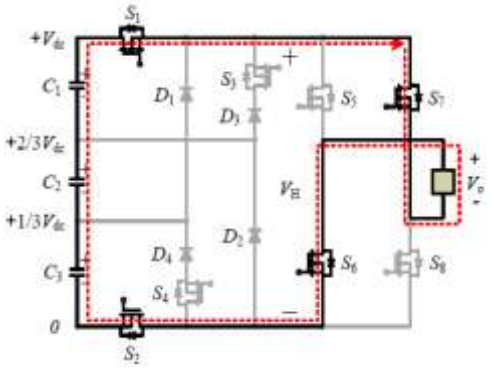

Figure 12. Mode VI

7) Here switches S5 and S7 are turned on. As a result V0= 0 is obtained across the output terminals. Fig. 13 gives pictorial explanation for this mode.

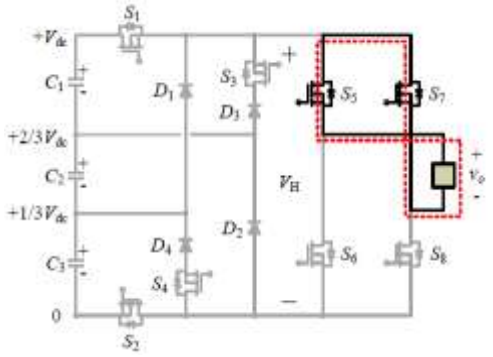

Figure 13. Mode VII

IV. HARDWARE RESULTS

Boost Converter:

 ISSN: 2321-8169
603 – 608

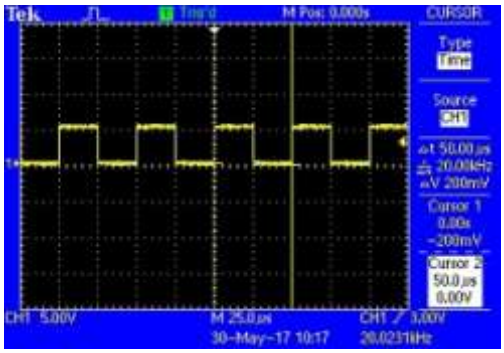

Figure 14. Gate Pulse of Boost Converter

Fig. 14 represents the gating pulses for MOSFET before driver circuit. It's Switching Frequency (Fs) is 20 KHz and Duty cycle (D) is 50%.

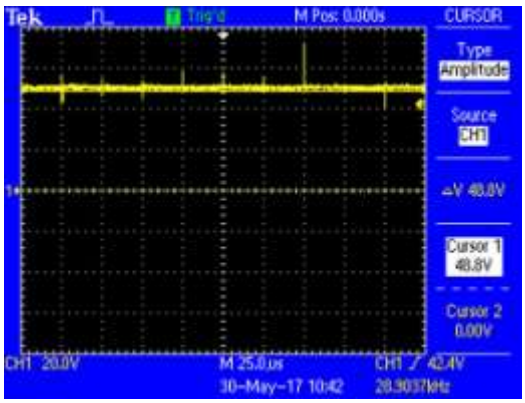

Figure 15. Output Voltage

Fig. 15 represents the output of the designed Boost Converter. Since the Solar supplies an input voltage of about 26V, the output voltage should be 52V. Due to drop in diode we are obtaining 48.8V.

ProposedInverter:

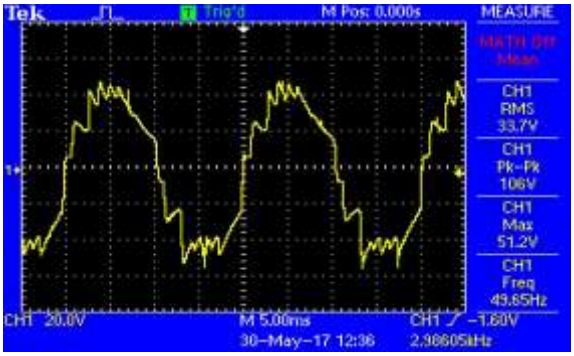

Figure 16. Inverter Output

Fig. 16 represents the output of the designed inverter. As explained in simulation results, in hardware prototype also we are able to achieve the seven level output. The table 1 represents the time period of the obtained output.

Table 1 Time Period of Output waveform

VOLTAGE LEVLS	TIME PERIOD
V_{DC}	6ms
$(2/3)V_{DC}$	2ms
$(1/3)V_{DC}$	1ms
0	1ms
$-(1/3)V_{DC}$	1ms
$-(2/3)V_{DC}$	2ms
$-V_{DC}$	6ms

And this matches the simulation results.

Figure 17. PWM Pulses

Fig. 17 represents the PWM pulses that is used for triggering the Switches S1, S2, S3, and S4 from the microcontroller.
Here,
Yellow colored signal is the PWM pulse that is fed to Switch S1.

Green colored signal is the PWM pulse that is fed to Switch S2.
Blue colored signal is the PWM pulse that is fed to Switch S3.
Pink colored signal is the PWM pulse that is fed to Switch S4.

When S1 is switched on PWM pulses are fed to S2 switch. And when S2 is turned on PWM pulses are fed to S1 switch respectively. Similarly, when S3 is turned off PWM pulses are fed to S4 and When S4 is turned off PWM pulses are fed to S3.

Figure 18. Pulses for H-Bridge

Fig. 5.16 represents the pulses for triggering the Switches S5, S6, S7, and S8, generated using Arduino Due.
Here,
Yellow colored signal is the pulse that is fed to Switch S5.
Green colored signal is the pulse that is fed to Switch S6.
Blue colored signal is the pulse that is fed to Switch S7.
Pink colored signal is the pulse that is fed to Switch S8.

To obtain 50 Hz output of the inverter, we operate these four switches at 180° phase shift with 10 ms each. Since S5 and S6 are in the same leg, we give inverted pulse to them to avoid the shorting of the switches. For same reason we give inverted pulse to S8 when compared to S7.

Harmonic Analysis:

Figure 19. Harmonic analysis of Inverter

$$\mathrm{THD_F} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots}}{V_1}$$

THD

$$= \frac{\sqrt{((1.565)^2+(2.504)^2+(2.191)^2+(0.6)^2+(0.94)^2)}}{28.4}$$

= 0.135 or 13.5%

V. CONCLUSION

Hence using Boost Converter we are able to boost from the input Solar Voltage of 25V to 48V under open loop conditions. The boosted output is then fed to the inverter. We are able to achieve the seven level output both in simulation and hard ware prototype. The THD obtained from simulation and hardware prototype were 6.24% and 13.5% (without filter in hardware implementation) respectively.

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