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High Speed and Low Power Consumption Carry Skip Adder using Binary to Excess-One Converter

Sanyukta Vijaykumar Chahande
Research Scholar (M. Tech), Dept of ECE
Anjuman College of Engineering and Technology
Nagpur, India
sanyuktavchahande@gmail.com

Prof. Mohammad Nasiruddin
Associate. Professor & Head of ECE Dept
Anjuman College of Engineering and Technology
Nagpur, India
mn151819@gmail.com

***Abstract*—**Arithmetic and Logic Unit (ALU) is a vital component of any CPU. In ALU, adders play a major role not only in addition but also in performing many other basic arithmetic operations like subtraction, multiplication, etc. Thus realizing an efficient adder is required for better performance of an ALU and therefore the processor. For the optimization of speed in adders, the most important factor is carry generation. For the implementation of a fast adder, the generated carry should be driven to the output as fast as possible, thereby reducing the worst path delay which determines the ultimate speed of the digital structure. In conventional carry skip adder the multiplexer is used as a skip logic that provides a better performance and performs an efficient operation with the minimum circuitry. Even though, it affords a significant advantages there may be a large critical path delay revealed by the multiplexer that leads to increase of area usage and power consumption. The basic idea of this paper is to use Binary to Excess-1 Converters (BEC) to achieve lower area and power consumption.

Keywords- *Arithmetic and Logic Unit(ALU), Carry Skip Adder, Binary to Excess-1 Converters(BEC)*

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I. INTRODUCTION

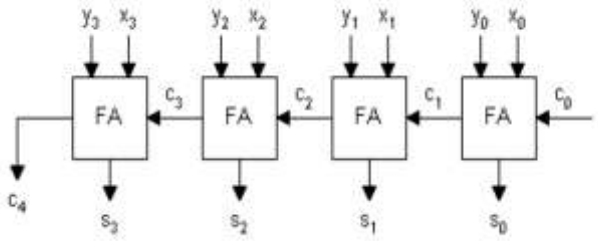
Well expressed in words that if you can count, you can control. Addition is a basic operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.Addition is an indispensable operation for any high speed digital system, digital signal processing or control system.Therefore pertinent choice of adder topologies is an essentialimportance in the design of VLSI integrated circuits for high speed and high performance circuits.

II. TYPE OF ADDERS

The design of various adders such as Ripple Carry Adder (RCA),Carry Increment Adder (CIA), CarryLook Ahead Adder (CLA), Carry Save Adder (CSA), Carry SelectAdder (CSLA) and Carry Skip Adder (CSkA) are discussed below.

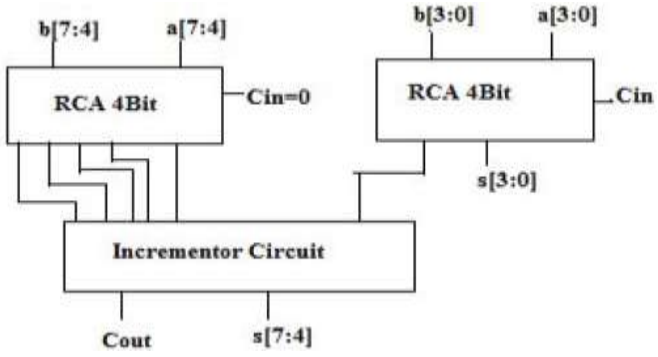
A. Ripple carry Adder(RCA)

Ripple Carry Adder (RCA) is a basic adder which works on basic addition principle [1]. The architecture of RCA is shown in figure below. RCA contains series structure of Full Adders (FA); each FA is used to add two bits along with carry bit.
The carry generated from each full adder is given to next full adder and so on. Hence, the carry is propagated in a serial computation[1]. Hence, delay is more as the number of bits is increased in RCA.



B. Carry Increment Adder(CIA)

The design of Carry Increment Adder (CIA) consists of RCA's andincremental circuitry [1]. The incremental circuit can be designedusing HA's in ripple carry chain with a sequential order. Theaddition operation is done by dividing total number of bits in togroup of 4bits and addition operation is done using several 4bit RCA's. The architecture of CIA is



C. Carry Look Aheah Adder(CLA)

As seen in the ripple-carry adder, its limiting factor is the time it takes to propagate the carry. The carry look-ahead adder

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solves this problem by calculating the carry signals in advance, based on the input signals. The result is a reduced carry propagation time.To be able to understand how the carry look-ahead adder works, we have to manipulate the Boolean expression dealing with the full adder. The Propagate P and generate G in a full-adder, is given as:

Pi = Ai XOR Bi Carry propagate

Gi = AiBi Carry generate

Notice that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay.

The new expressions for the output sum and the carryout are given by:

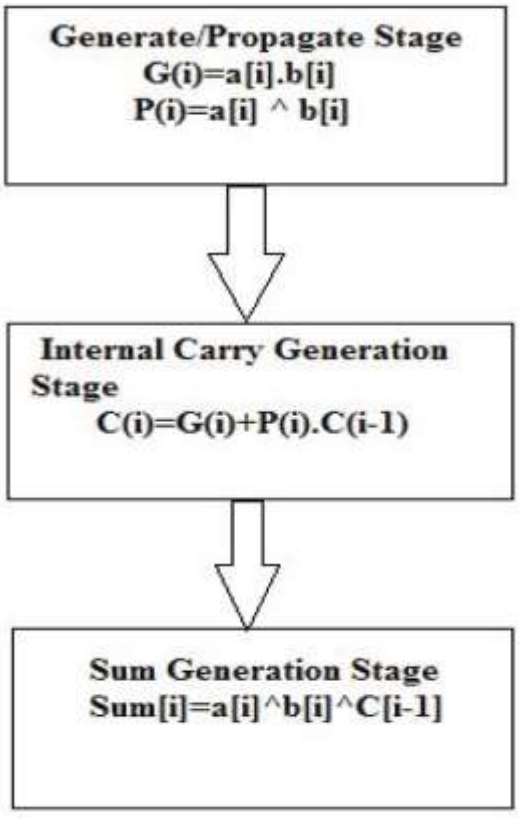
Si = Pi □ Ci-1

Ci+1= Gi + PiCi

These equations show that a carry signal will be generated in two cases:

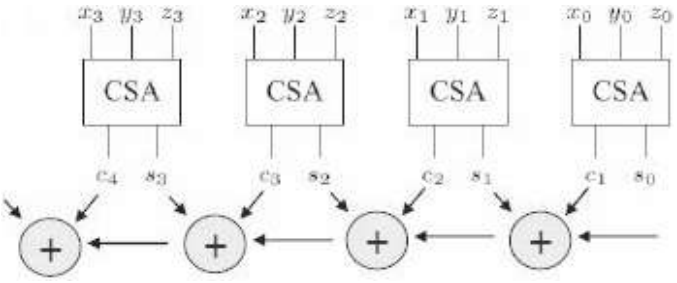
1) if both bits Ai and Bi are 1

2) if either Ai or Bi is 1 and the carry-in Ci is 1.



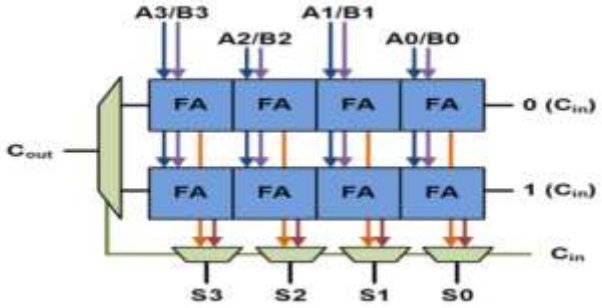
D. Carry Save Adder(CSA)

In Carry Save Adder (CSA), three bits are added parallelly at a time. In this scheme, the carry is not propagated through the stages. Instead, carry is stored in present stage, and updated as addend value in the next stage. Hence, the delay due to the carry is reduced in this scheme. The architecture of CSA is shown in figure



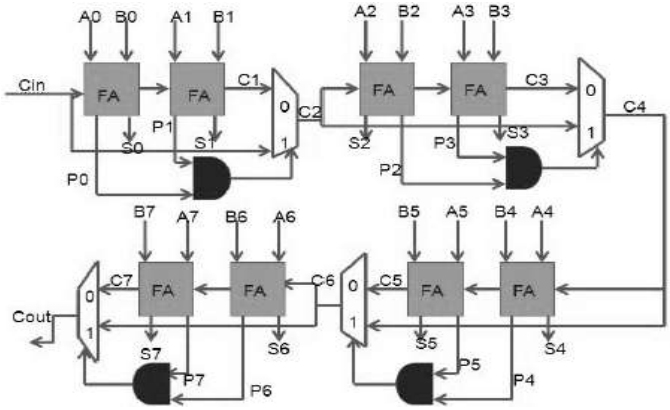
E. Carry Select Adder(CSLA)

Carry Select Adder (CSLA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 executed parallelly. Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected.



F. Carry Skip Adder(CSkA)

As the name indicates, Carry Skip Adder (CSkA) uses skip logic in the propagation of carry. It is designed to speed up theaddition operation by adding a propagation of carry bit around aportion of entire adder. Figure shows the architecture of CSkA.



III. PRIOR WORK

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures [19]. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder [23]. Many

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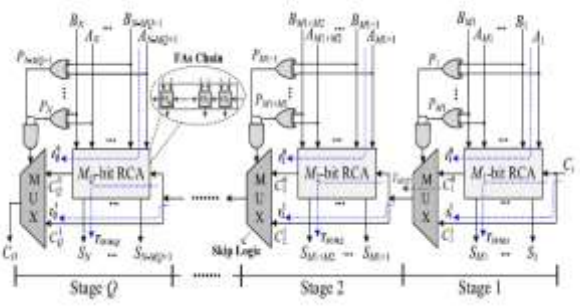
methods have been suggested for finding the optimum number of the FAs [18]–[26]. The techniques presented in [19]–[24] make use of VSSs to minimize the delay of adders based on a single level carry skip logic. In [25], some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power increase considerably and less regular layout.



The CSka with AOI/OAI logic structure is based on combining the concatenation and the incrementation schemes [13] with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces2:1 multiplexers by AOI/OAI compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay ,area, and smaller power consumption compared with those of the 2:1 multiplexer [37]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with as lightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI(or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates.

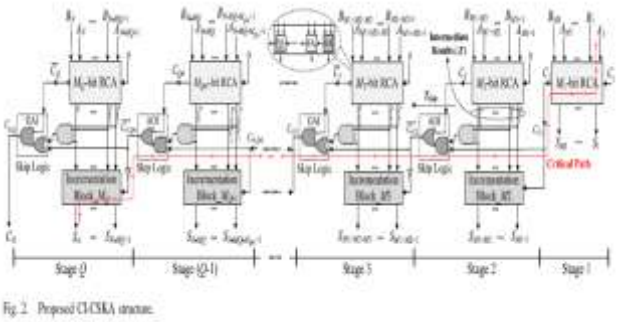


Fig. 2. Proposed CI-CSKA structure.

IV. PROPOSED WORK

Based on the discussion presented in Section III, it is concluded that by reducing the delay of the skip logic, one may lower the propagation delay of the CSKA significantly. Hence, in this paper, we present a modified CSKA structure that reduces this delay.

The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power.BEC uses less number of logic gates than N-bit full adder structure. To replace N bit RCA, an N+1 bit BEC is required. Therefore, Modified CSkA has low power and less area than conventional CSkA.

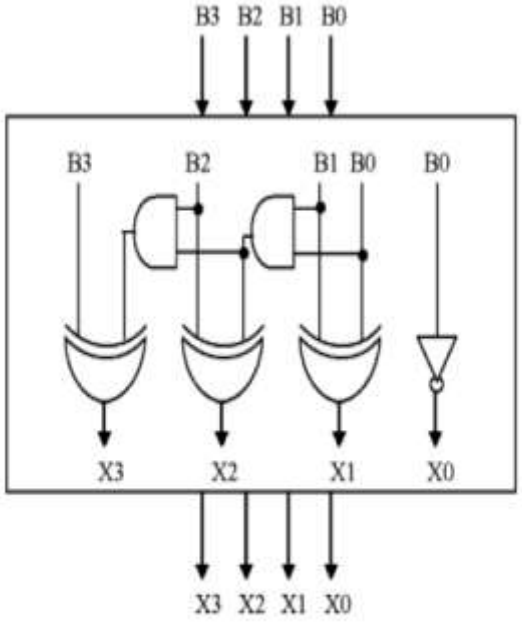


Fig. 2. 4-b BEC

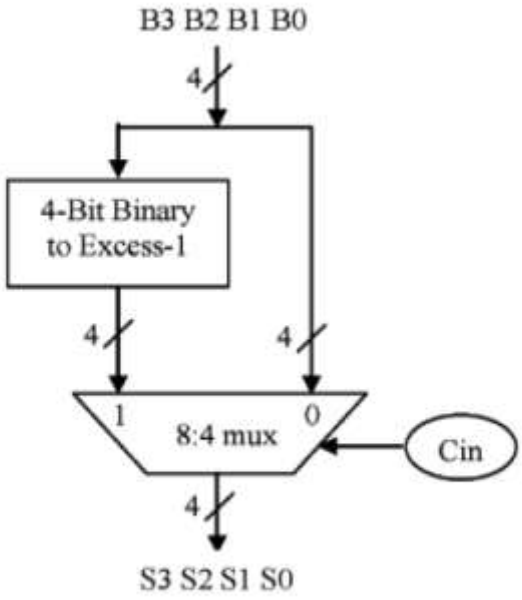


Fig. 3. 4-b BEC with 8:4 mux.

V. CONCLUSION

In this paper, Carry Skip Adder (CSKA) structure was proposed, which exhibits a higher speed and lower energy consumption compared with the conventional structure. The speed is through the use of Binary to Excess One converter for the carry skip logics. The results also suggested that the CSKA structure is a very good adder for the applications where both the speed and energy consumption are critical. In addition, a modified structure was proposed which reduces power consumption without affecting the delay of the structures.

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