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Optimized Design Space Exploration Framework Utilizing Predictive Fitness Evaluation Techniques

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Abstract**:** Design space exploration (DSE) is a critical process in system design, allowing for the identification of optimal configurations and parameter settings. This research proposes an advanced framework for DSE that integrates predictive fitness evaluation techniques to enhance the efficiency and accuracy of the exploration process. By leveraging machine learning models to predict the fitness of design points, our approach significantly reduces the computational overhead typically associated with traditional DSE methods. This framework facilitates faster convergence to optimal solutions by guiding the search process more effectively. Empirical results demonstrate that our predictive approach not only accelerates the exploration process but also maintains high accuracy in identifying optimal design configurations. This method has broad applicability across various engineering disciplines, including electronics, aerospace, and mechanical design, where rapid and precise DSE is essential.

Keywords: *Design Space Exploration, Predictive Fitness Evaluation, Machine Learning, Optimization, System Design, Parameter Optimization, Computational Efficiency, Engineering Design, Fitness Prediction, Machine Learning in DSE.*

I. INTRODUCTION

Design space exploration (DSE) is a pivotal aspect of the system design process, allowing engineers to evaluate a multitude of potential configurations and parameter settings to identify the optimal design. The increasing complexity of modern systems, particularly those involving embedded systems and multi-processor environments, necessitates advanced methodologies to efficiently navigate this vast design space. This research introduces an optimized framework for DSE that leverages predictive fitness evaluation techniques, significantly enhancing both the efficiency and accuracy of the exploration process.

Traditional DSE methods often suffer from high computational overhead due to the exhaustive evaluation of numerous design points. Recent advancements have shown the potential of integrating machine learning models to predict the fitness of design points, thereby reducing the computational burden. For instance, Alessio Colucci et al. [4] proposed a fast DSE framework for deep learning accelerators, demonstrating the benefits of predictive modeling in accelerating the exploration process. Similarly, Jan Spieck et al. [7] employed machine learning models for run-time scenario-based MPSoC mapping reconfiguration, highlighting the potential of these models in dynamic and complex environments.

The proposed framework builds upon these advancements by incorporating predictive fitness evaluation techniques into the DSE process. By utilizing machine learning models to estimate the fitness of various design points, the framework effectively narrows down the search space, focusing computational resources on the most promising configurations. This approach not only accelerates the convergence to optimal solutions but also maintains high accuracy in identifying the best design configurations.

In addition to the integration of predictive models, the proposed framework addresses the security concerns associated with embedded systems and multi-processor environments. Cybersecurity for embedded systems has become a critical issue, as highlighted by Abdulmohsan Aloseel et al. [2], necessitating robust design methodologies that ensure both performance and security. Our framework incorporates security-driven design principles to ensure that the optimized configurations are not only efficient but also secure.

Moreover, the proposed methodology is versatile, with broad applicability across various engineering disciplines. It can be employed in the optimization of embedded systems, multi-processor environments, and other complex systems requiring efficient DSE. The integration of predictive fitness evaluation techniques with traditional DSE methods marks a significant advancement, as evidenced by the work of Yong Xie et al. [9] in automotive cyber-physical systems and Sabeen Masood et al. [1] in multiprocessor embedded systems.

The following sections of this paper will delve into the detailed architecture of the proposed framework, the implementation of predictive fitness evaluation techniques, and the empirical results demonstrating the efficacy of our approach. By presenting a comprehensive analysis and validation of the optimized DSE framework, this research

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aims to contribute significantly to the field of system design and optimization.

II. LITERATURE SURVEY

Yong Xie, Gang Zeng, Ryo Kurachi, Hiroaki Takada, and Guoqi Xie, et al. [9] optimize the data throughput of a Controller Area Network bus taking possible attacks on the communication into consideration. They secure the com by adding message authentication codes (MACs) to messages vulnerable to manipulation. The additional overhead induced by these MACs influences the communication delay and system performance. The authors consider the influence of MACs on the performance constraint and describe a method to simultaneously optimize the system's timing behavior and secure the communication. Pimentel, Andy et. al. [10] As inserted systems develop increasingly perplexing and as new applications, for example, IoT require many design limitations, modern design space exploration techniques are fundamental so as to locate the best tradeoff between various design objectives and their tradeoff. This instructional exercise gives an organized knowledge into the field of design space exploration for inserted systems.

F. Tu, S. Yin, P. Ouyang, S. Tang, L. Liu, and S. Wei, et al. [11] presented a deep neural architecture (DNA), which can reconfigure its data paths to support dataflow techniques for different layer sizes. To find the optimal dataflow pattern, they simulate the analysis of buffer access and DRAM access. This paper performs a simulation by applying the roofline model to analyze the tendencies and provide an intuitive solution for optimal parameters in terms of the number of giga-operations per second (GOPS) and the computation-to-communication ratio (CCR).

S. N. Mahalank, K. B. Malagund and R. M. Banakar et. al. [12] presents a mind boggling Internet of Things framework needs systematic methodology in the underlying phases of the design to freeze between numerous accessible design options. The choices are situated at the framework level, method of information transmission and software module advancement level. The decisions influence the few design 2 objectives demonstrating the choices to speak to a multi-criteria issue to pass judgment on the nature of the new IoT design. A few parts of the design space condition are researched to address the inquiry that emerge at the system level joining stage, specifically the correspondence mode devices, software modules, design reconciliation issue and client administrations are interestingly distinguished from this structure. The necessary interface units, information move mode and software apparatus suite is given utilizing the IoT design space exploration approach. Clients inclinations dependent on the administration prerequisite depicts an end target design reaction that can be utilized in the arrangement model. Nan Feng, Harry Jiannan Wang, and Minqiang Li. et al. [13] propose a technique, which is also based on Bayesian networks for calculating cyber security risk. In their work, the authors describe a security risk management tool which takes into account historical security incidents as well as security expert judgment. Based on these inputs they formulate a risk analysis method. The authors do not consider techniques to mitigate security vulnerabilities, or decrease the security risk.

Kazmierski, Tom & Wang, Leran & Merrett, Geoff & Al-Hashimi, Bashir & Aloufi, Mansour, et. al. [14] presents Fast Design Space Exploration of Vibration-Based Energy Harvesting Wireless Sensors. To research the different exchange offs among these parameters, it is alluring to investigate the multi-dimensional design space rapidly. This paper presents a response surface model (RSM) based technique for quick design space exploration of a total remote sensor hub fueled by a tunable vitality collector A few test situations are considered, which represent how the proposed approach allows the designer to alter a wide scope of system parameters and assess the impact immediately yet with high exactness. In the created toolbox, the assessed CPU time of one RSM estimation is 25 μs and the normal RSM estimation mistake is not exactly 16.5%.

Buchli, Bernhard & Yücel, Mustafa & Lim, Roman & Gsell, Tonio & Beutel, Jan, et. al. [15] remote Sensor Network applications require trustworthy stages that convey right and solid activity over extensive stretches. In any case, application portrayal and accurate system prerequisites speciation can be muddled because of obscure natural elements and system restrictions. Right now we present another way to deal with design space exploration utilizing a component rich system for encouraged experimentation. We contend that outcomes acquired from experimentation with this stage permit fast speciation of advanced sensor systems at decreased expense.

Table -1 Summary Table

Reference	Authors	Title	Year	Conference/Journal
[1]	Masood et al.	Simulating Synchronization Issues on a Multiprocessor Embedded System for Testing	2021	IEEE ICICSE
[2]	Aloseel et al.	Analytical Review of Cybersecurity for Embedded Systems	2021	IEEE Access
[3]	Park et al.	Performance-efficient CPU Resource Management Algorithm on Heterogeneous Multi-processor	2020	IEEE ICCE
[4]	Colucci et al.	A Fast Design Space Exploration Framework for Deep Learning Accelerators: Work-in-Progress	2020	IEEE CODES+ISSS
[5]	Gressl et al.	Security Driven Design Space Exploration for Embedded Systems	2019	IEEE FDL
[6]	Kedia et al.	Work-in-Progress: A Case for Design Space Exploration of Context-aware Adaptive Embedded Systems	2019	IEEE CODES+ISSS
[7]	Spieck et al.	Run-Time Scenario-Based MPSoC Mapping Reconfiguration Using Machine Learning Models	2019	ACM/IEEE MLCAD
[8]	Sam, Agyeman	An Overview of Design Space Exploration of Cache Memory	2018	ACM
[9]	Xie et al.	Security/Timing-aware Design Space Exploration of CAN FD for Automotive Cyber-Physical Systems	2018	IEEE Transactions on Industrial Informatics
[10]	Pimentel	Exploring Exploration: A Tutorial Introduction to Embedded Systems Design Space Exploration	2017	IEEE Design & Test
[11]	Tu et al.	Deep Convolutional Neural Network Architecture with Reconfigurable Computation Patterns	2017	IEEE TVLSI
[12]	Mahalank et al.	Design Space Exploration for IoT-based Traffic Density Indication System	2016	ICRTIT
[13]	Feng et al.	A Security Risk Analysis Model for Information Systems: Causal Relationships of Risk Factors and Vulnerability Propagation Analysis	2014	Information Sciences
[14]	Kazmierski et al.	Fast Design Space Exploration of Vibration-Based Energy Harvesting Wireless Sensors	2013	IEEE Sensors Journal
[15]	Buchli et al.	Demo Abstract: Feature-Rich Platform for WSN Design Space Exploration	2011	IPSN

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This review underscores the diversity and depth of research in DSE methodologies, highlighting the integration of cybersecurity, machine learning, and performance optimization strategies across various application domains.

III. DESIGN SPACE EXPLORATION USING FITNESS PREDICTION TECHNIQUES

A methodology Framework for design space exploration using Fitness Prediction Techniques is represented in below Fig. 1.

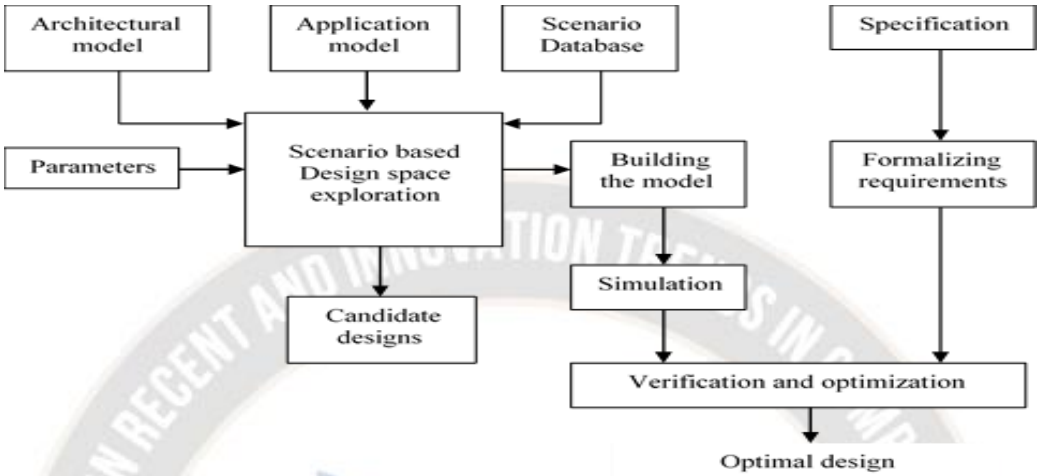

Fig. 1: WORKFLOW OF THE DESIGN SPACE EXPLORATION

The objective of the exploration framework is to establish a static mapping of multi-application workloads onto an MPSoC platform, which remains consistent throughout the system's operational lifespan. This necessitates optimizing the system's average performance across diverse application scenarios. The framework addresses several critical tasks in design space exploration (DSE). Initially, it involves constructing an accurate system model using suitable tools. Concurrently, formal requirements specification is essential, aligning with model development. Subsequently, simulations are conducted, and trace analyses verify compliance with specified requirements.

Scenario-based DSE focuses on mapping multi-application workloads onto an MPSoC platform. This requires explicit input of both the architectural model and the multi-application workload. The architectural model encompasses all available components and interconnections, which are then optimized by the DSE to utilize a subset of these resources suitable for the final MPSoC configuration.

The multi-application workload input comprises two key components. Firstly, application models define each application's structure, facilitating task mapping exploration. Secondly, a scenario database explicitly describes potential workload behaviors, including intra- and inter-application scenarios. This database enables the exploration of diverse workload behaviors, such as concurrent application modes and active applications.

During MPSoC DSE, a representative subset of application scenarios from the database is selected for efficient mapping evaluation. The subset selector dynamically identifies optimal scenarios using various techniques, ensuring accurate fitness prediction during the design exploration. This selection process is continuously refined using a training set of application mappings, adapting dynamically throughout the DSE process.

The fitness evaluation distinguishes between real fitness (F), which considers all scenarios, and estimated fitness ($\tilde{F}$), specific to the current scenario subset. The design explorer evaluates mappings based on the representative scenario subset ($\tilde{S}$), iterating through generations to refine mapping selections. Similarly, genetic algorithms (GA) evolve subsets using crossover and mutation to optimize scenario representation.

Model checking, involving automated verification against formal requirements, ensures model correctness and simulation validity. Techniques such as temporal Boolean logic and Satisfiability Modulo Theories (SMT) solvers verify compliance and provide debugging insights, crucial for ensuring design robustness.

Ultimately, the DSE framework yields a final set of candidate mappings validated by the trainer within the subset selector. This process guarantees that nondominated solutions, meeting stringent performance criteria, are retained throughout the design space exploration.

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IV. RESULT ANALYSIS

To validate the scenario-based Design Space Exploration (DSE), a series of experiments were conducted under controlled conditions. These experiments maintained a fixed multi-application workload and a predetermined set of architectural components. The multi-application workload was generated stochastically using a Python tool, simulating the behaviors of ten embedded applications. These applications collectively involved 58 processes and communicated through 75 channels, resulting in a diverse set of 4,607 distinct application scenarios.

Stochastic applications were chosen for their ability to offer broader variability than real-world applications, allowing for detailed parameter adjustments such as communication fractions. This flexibility facilitated a comprehensive study of DSE properties. The experiments focused on evaluating the impact of scenario subset size on mapping quality, particularly through an 8-hour DSE using a hybrid approach for scenario subset selection. During this process, two threads were dedicated to the subset selector, while six threads were allocated to the design explorer.

Key observations from the experiments include:

Accuracy: Larger scenario subsets enhance the accuracy of fitness predictions within the design explorer. This improvement enables more informed decisions regarding the selection of individuals for subsequent generations. In general, larger subsets increase the likelihood of identifying optimal mappings efficiently.

Overhead: Larger scenario subsets necessitate longer evaluation times per mapping. This extended evaluation period not only reduces the throughput of evaluated individuals but also limits the number of generations achievable within a set timeframe. Consequently, the effectiveness of the evolutionary search process diminishes, posing challenges in identifying optimal mappings within predefined time constraints.

In the experiment, four different subset sizes are used: 0.1%, 1%, 4%, and 16% of the total number of application scenarios. For each individual subset size, the result is averaged over nine DSE runs to take into account the stochastic nature of the GA in the design explorer. Fig. 2 and Fig. 3 shows the results of the experiments.

After a short period (5 min), the evaluation overhead is the most significant effect when looking at the different subset sizes. For the 1%, 4%, and 16% subsets, the minimal execution time is larger as the size of the used scenario subset increases. In case of the 0.1% subset, this deviation barely decreases over time. This shows that the DSE is far from accurate. For the other subsets, the prediction is accurate enough to result in a very small deviation at the end of 8 h of DSE.

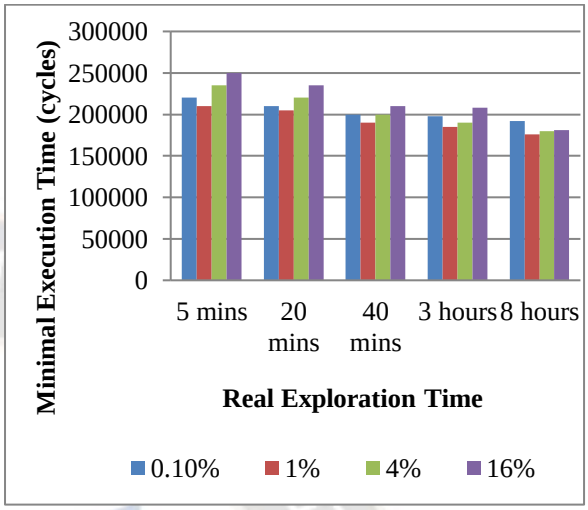

Fig. 2: EFFECT OF THE SUBSET SIZE ON QUALITY PERCEIVED RESULT OF DSE

The overhead effect is not visible any more once the GA is converged. Fig. 3 shows the convergence time (within 1% of final result). In general, a larger subset means a larger convergence time. An exception is the 0.1% subset. The 0.1% subset is not able to provide good mappings as the fitness prediction is not accurate enough. The increased convergence time of the design explorer is also seen in the minimal execution time in Fig. 2. In the first hour, the minimal execution time of the 4% subset larger than the 1% subset. The same holds for the 16% subset. Provided that the subset is accurate enough, the smaller the subset is, the earlier it gets close to the optimal execution time.

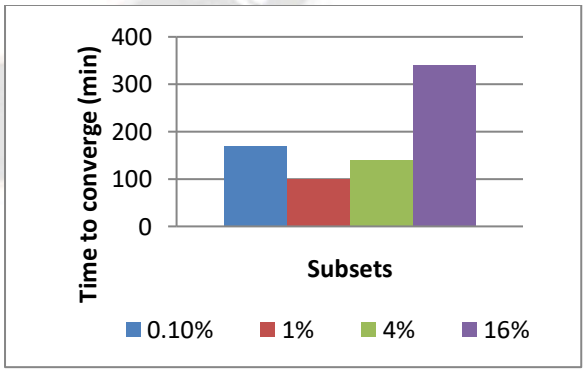

Fig. 3: EFFECT OF THE SUBSET SIZE ON OVERHEAD EFFECT

Therefore, we can speak of an accuracy threshold. Once the accuracy of the subset is above the accuracy threshold, the final GA results are not significantly affected by the subset

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size. However, due to the overhead effect, the convergence time will increase with a larger subset.

Our final experiment shows a comparison between the different subset selection methods and its effect on the efficiency of the DSE. Therefore, the required exploration time for the scenario-based DSE to identify a satisfying mapping is measured. After all, the faster the DSE can provide results that match the requirement of the user, the better it is. For this purpose, a DSE of 100 min is performed with all the subset selector approaches. Each experiment is performed for three different subset sizes (1%, 4%, and 8%). The results are averaged over nine runs.

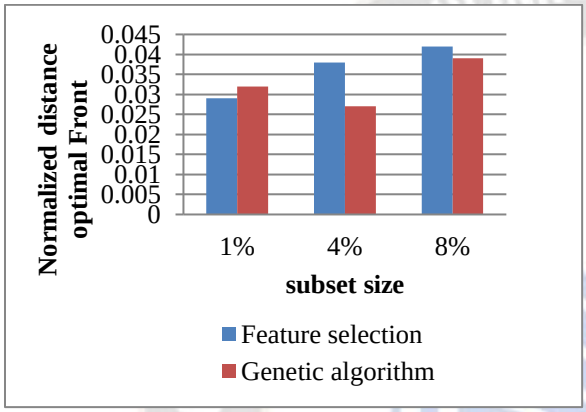

Fig. 4: QUALITY OF DSE FOR DIFFERENT SUBSET SELECTION APPROACHES

We observed that when increasing the subset two effects will occur: 1) higher accuracy, and 2) slower convergence. The FS subset selection has worse results when the subset becomes larger (the smaller the distance, the better). The GA however, shows a somewhat different effect. With 4% it is able to benefit from a subset with a higher accuracy. The slower convergence starts to affect the efficiency from the 8% subset. Comparing the different methods, the GA method has the best results. The only exception is for the 1% subset. In this case the feature selection is still able to search the smaller design space of possible subsets.

V. CONCLUSION

This paper presents a methodology framework for design space exploration (DSE) utilizing Fitness Prediction Techniques. The Scenario-based DSE facilitates efficient early exploration of dynamic multi-application workloads by concurrently exploring the design space of multi-application mappings on an MPSoC and representative scenario subsets. Fitness prediction plays a crucial role in assessing mapping quality, achieved through a representative subset of application scenarios derived from scenario subset co-exploration.

Experimental findings highlight two primary effects observed during DSE:

Overhead Effect: Increasing the size of the scenario subset results in more computationally expensive mapping evaluations. Consequently, DSE efforts required greater computational resources to identify the Pareto front.

Accuracy Effect: Larger scenario subsets improve prediction accuracy, enhancing the efficiency of genetic algorithms (GA) in reaching the Pareto front. Notably, GA performance benefits up to a 4% subset size increase, after which diminishing returns affect convergence efficiency.

Comparative analysis across different methods demonstrates that GA-based approaches yield superior results under these conditions.

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