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Review based on Semiconductor Manufacturing Process and Operations Optimization by Integrating AI Ready Hardware

[1*]Monish Katari
[1*]Master of Science, Electrical Engineering, Marvell Semiconductors.
[1*]Corresponding Author Email: monishkatari3@gmail.com

Abstract: The management of production bottlenecks, manufacturing equipment efficiency, and product quality management is growing more challenging for the semiconductor manufacturing business. Manufacturing businesses are recognizing that there are significant opportunities to apply Artificial Intelligence (AI) as a competitive advantage in order to maintain competitiveness in both productivity and sustainable growth. This review study elucidates AI readiness by enhancing productivity and streamlining the semiconductor manufacturing industry's process, and it is contrasted with prior research. The concepts put forward demonstrate how artificial intelligence might be applied to address issues in the processes involved in producing semiconductors. Nearly 25 to 70 research papers that are gathered from different standard publications. In the existing papers, automatic detection and AI methods are given with less results and it is overcome by our new AI ready hardware.

1. INTRODUCTION

Due to the competitive benefits [1] that artificial intelligence (AI) may offer industrial businesses in generating a more efficient and sustainable operation, AI has recently attracted a lot of attention from both academia and industry [2]. Developments in the underlying computing hardware commonly referred to as semiconductors, integrated circuits, microelectronics, or just chips, have made significant strides in the field of AI [4]. These advancements have facilitated the development of AI systems by providing more processing capacity. AI refers, in general, to computing systems that are able to learn from data and produce conclusions, suggestions, or classifications [5]. Production and AI technology advancements are driving the rate of the manufacturing sector's current transformation, known as Industry 4.0 or Smart Manufacturing [6]. Simultaneously, an increasing number of novel and developing AI technologies, including big data analytics, sophisticated robotics, computer vision, expert systems for diagnostics, and pattern matching for departing product quality [7], are having a significant impact on the manufacturing sector. By [8] automating and optimizing many productions and manufacturing process phases, artificial intelligence is transforming the semiconductor manufacturing industry. AI-powered systems watch over industrial processes all the time, looking for irregularities, flaws, and possible problems [9]. Better yield rates, better-quality products, and lower costs are the results of this [10]. Moreover, AI's capacity for large-scale data analysis makes root cause analysis easier, which helps find and fix production inefficiencies [11]. The need for hardware powered by AI is changing the semiconductor market and highlighting both opportunities and problems [12].

Gartner estimates that sales of semiconductors used in artificial intelligence (AI) could rise quickly from $44 billion in 2022 to $120 billion in 2027 [14]. Hardware designated for artificial intelligence (AI) comprises specific parts that are designed and tuned to run AI programs [15]. For AI and machine learning activities, these components often possess fast processing speeds, low latency, and high parallel processing capabilities [16]. AI-ready hardware can help semiconductor manufacturing processes operate more efficiently, with better quality control, and at a lower cost [17]. Semiconductor makers can anticipate equipment breakdowns, identify flaws instantly, and improve production processes by employing AI algorithms [19]. Increased yield rates, a shorter time to market, and generally better product quality are possible outcomes of this [21]. Furthermore, semiconductor makers may gain greater business insights and make more educated decisions by utilizing AI-ready technology to gather and analyze massive volumes of data [22]. All things considered, incorporating AI-ready hardware into semiconductor manufacturing procedures can have a big impact and support producers in remaining [24] competitive in the quick-paced semiconductor market.

2. OVERVIEW

There are many uses for semiconductors in our daily lives. For instance, cellphones, artificial intelligence, and 5G use

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would all be impossible without semiconductors. As a result, an upgraded procedure will give electronics company an advantage over its competitors. [25] Research on the worldwide semiconductor market from 2006 to 2021 indicates that rising processing costs and new materials are driving up semiconductor costs. A second round of price increases for chips was experienced globally in 2021 as a result of COVID-19. One explanation is that the epidemic disrupts the raw material supply. The other reason is that the cost of innovative manufacturing techniques is increasing due to their complexity. People witnessed the advancement of the semiconductor manufacturing process from 32 nm to 5 nm between 2011 and 2021. Every business employed its own cutting-edge transistors during the development. Using Intel as an example, businesses employed the first generation of Tri-gate FinFET transistors in 2012, the year that the 22 nm lithography technology was introduced. The business invested a large sum of money on researching and creating more sophisticated methods [26]. This does, however, also indicate [69] certain shortages there. The more the company advanced, the more difficult it became to build the semiconductor production process; the more sophisticated the process, the harder it is to develop. This widens the disparities between various companies as well. Samsung and TSMC developed two manufacturing processes: 5 nm LPE and N5. The chips that use these, however, have completely different power consumptions. Therefore, as firms improve the performance of their chips, they must figure out how to overcome the issue of power consumption. The most recent processor, the Snapdragon 888, has higher power consumption and employs 5 nm LPE. When they played with the chip, some researchers claimed to have felt 50°C on their backs [70].

2.1 Working

A semiconductor is a material with certain electrical characteristics that allow it to be used as the basis for electronic devices such as computers. Usually, it is a solid chemical element or compound that, under some circumstances, conducts electricity and, in others, does not. Because of this, it's the perfect medium for managing electrical current in household equipment. One that is not an insulator is referred to as an insulator, while one that is a conductor [27] is one that is not able to conduct electricity. The characteristics of semiconductors lie between those of an insulator and a conductor.

Fig: Semiconductor

Within a single atom, electrons arrange themselves into layers known as shells. A valence shell is the outermost shell found in an atom. The electrons that create bonds with nearby atoms are those in this valence shell. Covalent bonds are what we refer to as such. One electron makes up the valence shell of the majority of conductors. In contrast, the valence shell of semiconductor typically comprises four electrons [28]. Nonetheless, electrons may bind with the valence electrons of other atoms if they are adjacent atoms of the same valence. Atoms arrange themselves into crystal formations whenever that occurs. These crystals, primarily silicon crystals, are used to create the majority of semiconductors.

2.1.1 Types of Semiconductors*:* There are totally two types of semiconductors on the element based, that are placed near silicon a process is called as doping. Finished semiconductor alters the properties because of these doping impurities introduced to the crystalline silicon.

N-type - Phosphorus or arsenic are incorporated into silicon in trace amounts during N-type doping. With five outside electrons apiece, phosphorus and arsenic are out of position as they enter the silicon lattice. Since the fifth electron has nothing to attach itself on, it can travel around freely. A very little amount of the impurity is required to provide enough free electrons for an electric current to pass through silicon. Silicon of the N-type is a good conductor. N-type refers to the negative charge of electrons. [29].

P-type - Gallium or boron is the dopant used in P-type doping. Gallium and boron have only three outer electrons apiece. They create "holes" in the silicon lattice when combined with the silicon, which provide an electron in the silicon with nothing to connect to. The term "P-type" refers to the phenomenon of a positive charge resulting from the absence of an electron. Current can flow through holes. A hole will gladly take in an electron from its neighbor, which causes the hole to move across space. Silicon of the P-type is a good conductor.

2.1.2 Uses of Semiconductors: The semiconductor is classified into four types. They are

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Memory: Memory chips transfer data to and from the brains of computer devices and act as temporary data storage. A small number of industry titans, including Toshiba, Samsung, and NEC, are able to maintain their competitiveness due to the persistent market consolidation that has driven memory prices to extremely low levels [30].

Microprocessors: These CPUs are equipped with the fundamental logic needed to do out tasks. With the exception of Advanced Micro Devices, practically every other rival has been driven into smaller niches or entirely distinct markets by Intel's dominance of the microprocessor business.

Commodity Integrated Circuit: These are often made in large quantities for regular processing and are sometimes referred to as "standard chips". This market offers extremely low profit margins that only the largest semiconductor companies can match, and is dominated by very large Asian chip manufacturers [31].

Complex SOC: The term "System on a Chip" refers to the process of creating an integrated circuit chip that may house the whole functionality of a system. The market is driven by consumers' increasing need for consumer goods with more features at cheaper costs. The memory, microprocessor, and commodity integrated circuit markets are closed, leaving the SOC segment as the only one that still has enough room to draw a diverse set of businesses.

2.2 Semiconductor manufacturing process operations

A number of crucial steps in the semiconductor manufacturing process are necessary to produce high-quality semiconductors. Among these operations are:

Wafer fabrication: Silicon wafers, the building blocks of semiconductor devices, are produced during this process. Wafers are put through a number of critical processes, including doping, polishing, and slicing, in order to get the required structure [32].

Lithography: Lithography is a crucial process in the production of semiconductors, which entails employing photomasks and ultraviolet (UV) rays to pattern circuit designs onto the wafer. This procedure is essential for precisely designing complex circuit designs.

Etching: The process of creating the desired circuit structure on a wafer involves etching away undesired material. Wet etching as well as dry etching is the two primary etching methods employed for the production of semiconductors.

Deposition: The process of depositing thin material layers onto a wafer surface in order to form the structures required for semiconductor devices is known as deposition. Physical vapor deposition (PVD) as well as chemical vapor deposition (CVD) are two common deposition methods [33].

Doping: The process of adding impurities to semiconductor material to change its electrical characteristics is known as doping. Transistors and other electronic components with particular conductivity values must be made using this procedure.

Metallization: The process of adding metal layers onto the wafer surface in order to connect different parts of a semiconductor device is known as "metallization." For the device to perform properly and be reliable, this operation is essential.

All things considered, these processes are vital to the production of semiconductors, and each of them affects the overall stability and functionality of the finished product. To produce semiconductors of high caliber needed to satisfy the stringent specifications of contemporary electronic devices, these processes must be well controlled and optimized.

2.3 Challenges occurred in semiconductor manufacturing process

In the semiconductor manufacturing process, some of the challenges occurred and they are overcome by our proposed method. Some of the challenges are

Efficiency: The ongoing requirement to increase production process efficiency is one of the difficulties faced by semiconductor producers. Numerous things, such as inadequate equipment maintenance, production line bottlenecks, and supply chain management problems, can lower efficiency [34]. These inefficiencies may result in higher manufacturing costs, longer lead times, and eventually reduced earnings for the business. Equipment downtime brought on by inadequate maintenance procedures is a frequent cause of inefficiency in the semiconductor manufacturing industry. Machine malfunctions or subpar performance can cause significant delays and disrupt the manufacturing plan. Manufacturers can reduce downtime and maintain smooth production by putting in place regular maintenance schedules and providing adequate training for workers on how to operate equipment. Production line bottlenecks are another factor that may impact semiconductor production effectiveness. Congestion and delays in the overall production schedule might arise from specific steps in the manufacturing process being slower than others. Manufacturers can improve overall efficiency and optimize their processes by locating and resolving these obstacles. Another important component of efficient semiconductor production is supply chain management. Production delays and disruptions can be caused by problems with inventory management, shipping, or obtaining materials. Manufacturers can guarantee a consistent supply of materials and [35] reduce interruptions in the production process by collaborating

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closely with suppliers and putting strong inventory management systems in place. All things considered, increasing manufacturing efficiency in semiconductors necessitates a thorough strategy that takes supply chain management, production bottlenecks, and maintenance procedures into account. Manufacturers can enhance their bottom line by reducing expenses, raising productivity, and addressing these factors.

Quality control: Defect identification and prevention is a major source of quality control issues in semiconductor manufacturing operations. The performance and dependability of the finished product can be greatly impacted by even the slightest flaws due to the growing complexity and shrinking of semiconductor components. Because the components are small and are created at fast speeds, it can be difficult to detect these faults. Variability in the process is another problem that might result in inconsistent end products. Temperature, pressure, chemical composition, and other variables can vary, which can impact how well semiconductor devices function. Maintaining product quality requires tight control and monitoring of these characteristics. Lastly, one of the main issues with semiconductor production methods is contamination. Defects in the finished product, such as performance problems or failure, can be caused by even the smallest particles or contaminants. To avoid contamination and preserve premium semiconductor devices, stringent cleanliness standards and cutting-edge cleaning methods are required. In general, solving these quality control issues is essential to guaranteeing semiconductor goods' dependability and functionality.

Yield loss: Defects at several phases of the production process can lead to low yield rates in semiconductor manufacturing processes. A variety of problems, including faulty machinery, inconsistent processes, faulty materials, and human error, can result in yield loss.

.**Fault detection:** In semiconductor manufacturing processes, fault detection is critical to guaranteeing the end product's quality and dependability. Due to the intricate and sophisticated nature of semiconductor production, even little flaws or defects in the process can have a big impact on how well the finished product performs. Statistical process control, machine learning algorithms, and real-time monitoring systems are only a few of the methods and resources used for defect identification in semiconductor [37] manufacturing processes. These instruments assist in detecting departures from the anticipated process parameters and notify operators of possible problems before they escalate.

3. AI READY HARDWARE

Hardware designated for AI tasks and algorithms is referred to as AI-ready hardware. To handle the complicated computations needed for AI and machine learning applications, these components often have fast processing speeds, low latency, and strong parallel processing capabilities. Field-programmable gate arrays (FPGAs), graphics processing units (GPUs), tensor processing units (TPUs), and chips designed specifically for artificial intelligence (AI), including Intel's Nervana and Google's TPU, are a few examples of hardware that is ready for AI. Faster processing speeds and lower energy consumption are possible with AI-ready technology, which can greatly increase the effectiveness and performance of AI applications. Applications requiring large-scale data processing or real-time analysis may find this to be extremely crucial [38].

3.1 Graphics Processing Units (GPUs)

GPUs are essential to semiconductor production processes because they improve performance and optimize procedures. These specialized processors are made to speed up data processing, conduct intricate computations, and produce images. GPUs can be used in semiconductor manufacturing to simulate, model, and test different parts and processes, enabling quicker and more effective production techniques. Businesses can decrease time-to-market, speed up semiconductor product design and [46] development, and increase overall operational efficiency by utilizing GPUs. Through the use of more precise simulations and analyses, GPUs can also contribute to the overall improvement of the product's quality. GPUs can also be used for activities like image processing, pattern recognition, and machine learning algorithms, which further improves the capabilities of semiconductor production processes. In general, the incorporation of GPUs into semiconductor production processes facilitates enhanced efficiency and productivity, resulting in technological progress and industry innovation [39].

3.2 Tensor processing units (TPUs)

Tensor Processing Units (TPUs) are specially engineered integrated circuits intended to carry out machine learning tasks in an effective manner. In order to maximize activities like speech recognition, image identification, and natural language processing, these specialized processors are used in semiconductor production processes. Through the utilization of TPUs, semiconductor producers can enhance productivity and efficiency by quickening the rate of data processing and analysis. TPUs have the ability to execute intricate calculations at breakneck speeds, which makes them perfect

for managing the massive volumes of data produced during semiconductor production operations. Moreover, TPUs are incredibly energy-efficient; they perform better than conventional CPUs or GPUs while using less power. This minimizes the environmental impact of semiconductor manufacturing activities while simultaneously lowering operational expenses. All things considered, the incorporation of TPUs into semiconductor production procedures has changed the game, allowing producers to remain at the forefront of technological advancement and preserve a competitive advantage in a sector that is growing faster by the day [40].

3.3 Field-Programmable Gate Arrays (FPGAs)

Because they provide a versatile and changeable means of optimizing operations, FPGAs are an essential part of the semiconductor production process. These gadgets are integrated circuits that can be programmed to carry out particular tasks, which makes them perfect for a range of uses in the semiconductor sector. FPGAs can be utilized in industrial processes to decrease power consumption, enhance performance, and speed up complex algorithms. FPGAs help manufacturers swiftly adapt to changing requirements and improve their processes for optimal efficiency by enabling rapid prototype and iteration. All things considered, FPGAs' adaptability and dependability make them a vital instrument for increasing production and maintaining competitiveness in the dynamic semiconductor market [41].

3.4 Google's Tensor Processing Unit (TPU)

The Tensor Processing Unit (TPU) from Google is an application-specific integrated circuit (ASIC) that was created especially for workloads including machine learning and artificial intelligence. TPU is used to optimize processes in the semiconductor manufacturing process by offering high-performance, energy-efficient computing capabilities for AI workloads. TPU's distinct architecture and design allow Google to quickly execute and enhance overall performance by processing massive volumes of data and accelerating machine learning models. Google is able to lower operational costs, improve the effectiveness of its AI operations, and provide consumers with more sophisticated AI-powered services by integrating TPUs into their data centers. All things considered, the incorporation of Google's TPU into the semiconductor production process has markedly advanced AI capabilities, permitting quicker and more effectively handling complicated data, as well as propelling advancements in machine learning [42].

3.5 Intel's Nervana

The semiconductor manufacturing process has been enhanced and optimized by the integration of Nervana technology from Intel. Nervana's machine learning and artificial intelligence algorithms enable it to anticipate and assess possible problems in the production line, enabling proactive real-time modifications. This lessens faults in the finished products, boosts production, and decreases downtime. Nervana can also schedule manufacturing runs optimally, which improves throughput and reduces costs overall. All things considered, Nervana technology from Intel is taking the semiconductor production industry by storm and opening the door to more streamlined and effective operations [43].

3.6 Role of AI ready hardware in semiconductor manufacturing process to optimize operations

Hardware that is AI-ready is becoming more and more necessary in semiconductor production processes to maximize efficiency. These cutting-edge hardware systems have the processing power and memory required to run AI algorithms that can instantly examine and comprehend enormous volumes of data. Semiconductor makers may increase overall productivity, improve product quality, and automate and streamline processes with AI-ready gear. Predictive maintenance is a crucial function of AI-ready hardware in the semiconductor manufacturing process. AI algorithms can identify possible problems before they arise by evaluating data from sensors and equipment [44] in real-time. This allows manufacturers to take proactive measures to address the issues and save expensive downtime. AI-ready technology may also detect equipment problems, find bottlenecks in production processes, and suggest changes to increase overall efficiency. Furthermore, by evaluating data from numerous sources, such as sensors, cameras, and inspection systems, AI-ready hardware can assist semiconductor makers in improving the quality of their products. Manufacturers can detect flaws early in the [45] production process and take corrective action to guarantee consistent quality by utilizing AI algorithms to understand this data. All things considered, AI-ready hardware plays a critical role in semiconductor manufacturing to drive efficiency, enhance product quality, and optimize operations. Manufacturers may keep a step ahead of the competition and satisfy the expectations of the quickly changing semiconductor industry by utilizing AI algorithms on cutting-edge hardware systems.

4. RELATED WORKS

Ref no: [47].

Author name: Senoner, J., *et al.*, 2022.

Title: Using Explainable Artificial Intelligence to Improve Process Quality: Evidence from Semiconductor Manufacturing

Description: In particular, we suggest utilizing nonlinear modeling with Shapley additive explanations to deduce the relationship between a collection of production parameters and a manufacturing system's process quality. In an actual application, the decision model is verified at a top producer of high-power semiconductors. This paper used a decision model to choose improvement activities for a transistor chip product in an effort to increase production yield. In comparison to our sample's average yield, the experiment yields a 21.7% reduction in yield loss. Additionally, we present findings from a post-experimental implementation of the decision model, which yielded noteworthy enhancements in yield. We illustrate the practical usefulness of explainable AI by demonstrating that crucial factors influencing process quality might be overlooked by utilization of traditional technique.

Ref no: [48].

Author name: Chien, C.F *et al.,* 2020

Title: Advanced Quality Control of Silicon Wafer Specifications for Yield Enhancement for Smart Manufacturing.

Description: The UNISON framework is utilized to determine the ideal raw material specifications for various products in the researcher's advanced quality control (AQC) solution for raw wafers for enhanced yield enhancement. An empirical study was carried out in a top semiconductor fabrication facility to determine the best practices for enhancing quality indices such as yield, overlay errors, defect count, and anti-contamination capability. The outcomes have demonstrated the suggested analysis approach's practical applicability. The developed solution is, in fact, applied in actual environments.

Ref no: [49].

Author name: Liu, C.W *et al.,* 2013.

Title: An intelligent system for wafer bin map defect diagnosis: An empirical study for semiconductor manufacturing.

Description: The author suggested an intelligent method based on edges for diagnosing WBM defects in order to increase wafer production yield. WBM clustering solution, knowledge database, and graphical user interface made up the suggested system. Specifically, the developed WBM clustering approach integrates Moment Invariant (MI), Cellular Neural Network (CNN), Adaptive Resonance Theory (ART) neural network, and spatial statistics test to efficiently cluster various patterns. Furthermore, an interactive conversational interface is designed to document the diagnosis expertise from the domain experts into the knowledge database and display potential root causes in a similarity-matching sequence. Purity, diversity, specificity, and efficiency were the four performance indices that were employed in the assessment. Ultimately, the suggested WBM intelligent system has a more effective ability to identify fault patterns.

Ref no: [50].

Author name: Wang, C.H *et al.,* 2006.

Title: Detection and classification of defect patterns on semiconductor wafers.

Description: This study proposed an autonomous method to validate actual and simulated data, which consists of a spatial filter, a classification module, and an estimating module. Based on experimental results, it is possible to successfully extract and classify three types of typical defect patterns: (i) a linear scratch; (ii) a circular ring; and (iii) an elliptical zone. For elliptic and linear patterns, a Gaussian EM technique is employed, whereas a spherical shell approach is employed for ring pattern estimation. Moreover, a hybrid clustering technique may concurrently identify convex and nonconvex fault patterns.

Ref no: [51]

Author name: Harada, M *et al.,* 2019.

Title: Defect Detection Techniques Robust to Process Variation in Semiconductor Inspection.

Description: With (a) an Integration of Multiple Comparison-Detection findings (IMCD) to reduce the number of defect candidates and (b) a Discrimination Based on a Normal Image Model (DNPM) to determine whether the candidate is a defect or normal, the author suggested a defect detection approach. Combining the IMCD and DNPM results in a complaint information discrimination rate of 84.4% and a defect identification rate of 93.3%, which are greater than those of the one-class Support Vector Machine (SVM), according to an examination conducted using SEM pictures of a processed wafer. Moreover, flaws can be more effectively manually tagged for the automatic defect classification function, opening the door to effective defect analysis.

Ref no: [52]

Author name: Nakata, K *et al.,* 2017.

Title: A Comprehensive Big-Data-Based Monitoring System for Yield Enhancement in Semiconductor Manufacturing.

Description: The author concentrated on the yield analysis assignment, which involves engineers using production records and chip breakdown map patterns to determine the

cause of failure. We divide the yield analysis activity into three stages: monitoring failure map patterns, identifying failure causes, and monitoring failure recurrences. To aid engineers in their work, we integrate machine learning and data mining technologies into each step. Additionally, we used deep learning to classify wafer failure map patterns. We thoroughly examined the Deep Learning architecture and hyperparameters and demonstrated that it is also well suited for a semiconductor production application. Our all-inclusive, integrated "Big Data Based" monitoring solution is anticipated to result in a significant increase in yield and a decrease in the work required of engineers.

Ref no: [53].

Author name: Saqlain, M *et al.*, 2020.

Title: A Deep Convolutional Neural Network for Wafer Defect Identification on an Imbalanced Dataset in Semiconductor Manufacturing Processes.

Description: For continuous wafer fault diagnosis, the author suggested using a convolutional neural network based on deep learning (CNN-WDI).Rather of obtaining attributes manually, the suggested approach extracts useful characteristics using convolution layers. Our model performed better than any machine learning-based wafer defect classification model that had previously been proposed, according to a comparison of experimental results using a real wafer dataset. With nine distinct wafer map faults, the CNN-WDI model's average classification accuracy is 96.2%, an increase of 6.4% over the previous highest average accuracy using the same dataset.

Ref no: [54].

Author name: Zhang, F *et al.*, 2020.

Title: Semiconductor wafer fabrication production planning using multi-fidelity simulation optimization.

Description: The author suggested using a multi-fidelity simulation optimization technique to quickly assess and choose the optimal production plan from a wide range of plans that were being considered. We create an approximate model of an open queue for a wafer production system and subsequently employ the low-fidelity lead time estimations derived from the approximation model in a recently devised multi fidelity simulation optimization technique. The multi-fidelity technique considerably increases the computing efficiency of simulation-based production planning, according to the results of simulation experiments.

Ref no: [55].

Author name: Hsu, C.Y *et al.*, 2021.

Title: Multiple time series convolutional neural network for fault detection and diagnosis and empirical study in semiconductor manufacturing.

Description: The purpose of this research is to suggest a Multiple Time-Series Convolution Neural Network (MTS-CNN) model for semiconductor manufacturing problem diagnosis and detection. The diagnostic layer in the suggested MTS-CNN also determines the significance of each sensor. The experimental results show that the MTS-CNN works better than other multivariate time series classification techniques currently in use by accurately detecting the fault wafers with high recall, precision, and accuracy. We can determine the association between each fault and various sensors by analyzing the diagnostic layer's output value in MTS-CNN. This provides important information that may be used to associate an excursion with a defect.

Ref no: [56]

Author name: Lee, S**.** *et al.*, 2020.

Title: Dynamic dispatching system using a deep denoising autoencoder for semiconductor manufacturing, Applied Soft Computing, 86, p.105904.

Description: The study suggests applying a DDAE to solve a dispatching rule selection issue, which is a significant issue in the production of semiconductors. The importance of dispatching systems for storage allocation has grown recently as operational problems generate inefficient transfers, which in turn cause output losses. Furthermore, when determining the optimal sending decision, current methods did not account for the potential for a class imbalance issue.The testing results showed that, in terms of machine usage and throughput, the suggested strategy performed better than the current approaches.

Ref no: [57]

Author name: Azamfar, M *et al.*, 2020.

Title: Deep Learning-Based Domain Adaptation Method for Fault Diagnosis in Semiconductor Manufacturing.

Description: A deep learning-based domain adaptation technique for wafer fault diagnostics in the semiconductor manufacturing procedure was put out by the author. For fault identification in semiconductor manufacturing, they employed a deep learning-based domain adaptation technique. The deep neural network optimizes the greatest mean discrepancy measure using the high-level data representation it has learned. Based on real-world semiconductor manufacturing dataset experimental findings, the suggested method appears to provide a broad and efficient data-driven defect diagnostic strategy for quality inspection.

Ref no: [58]

Author name: Shim, J. *et al.*, 2021.

Title: Adaptive fault detection framework for recipe transition in semiconductor manufacturing.

Description: To reduce the performance drop brought on by the recipe change, an adaptive fault detection approach is suggested. In this framework, unsupervised adaptation is used to minimize the performance deterioration just after the recipe switch. Semi-supervised adaptation is utilized to promptly recover the performance with limited labeled information following the acquisition of inspection findings for a few novel dish wafers. The result showed via empirical studies that the suggested framework can adapt to the new recipe with less deterioration in performance.

Ref no: [59]

Author name: Xue, C.X. *et al.*, 2021.

Title: A CMOS-integrated compute-in-memory macro based on resistive random-access memory for AI edge devices.

Description: In traditional computing designs, the requirement to transport data between the processor and memory limits the creation of compact, energy-efficient artificial intelligence edge devices. Such problems may be solved by non-volatile compute-in-memory (nvCIM) architectures, but the creation of high-bit-precision configurations needed for dot-product operations is still difficult. In this instance, we present a 2 Mb nvCIM macro that is based on single-level cell resistive random-access memory devices and was created using a 22 nm complementary metal-oxide-semiconductor manufacturing approach. It comprises memory cells and associated peripheral circuitry. Our macro can execute multibit dot-product operations with higher input–output parallelism, less cell-array size, better precision, lower processing latency, and lower energy consumption as compared to earlier nvCIM techniques.

Ref no: [60]

Author name: Jiang, D. *et al.*, 2020.

Title: A Novel Framework for Semiconductor Manufacturing Final Test Yield Classification Using Machine Learning Techniques.

Description: A unique and scalable system that uses machine learning approaches to forecast the yield of Final Tests (FT) in semiconductor production. Comparing this framework to previous research, it can estimate FT yield during the wafer fabrication stage, allowing FT yield reduction issues to be identified sooner in the manufacturing procedure. Regarding data pre-processing, the current methodology uses the Gaussian Mixture Models, One Hot Encoder, and Label Encoder approaches. Model selection and model ensemble utilizing the F1-macro technique is proven to boost the accuracy of the models for both binary and multi-class classification. Three mass-production products with various wafer technologies and manufacturing flows have been subjected to the framework's application. They all received good F1-macro test scores, demonstrating the stability of our architecture.

4.1 Survey based on existing techniques

Author name	Proposed methodology	Technique	Result	Limitations
Jiang, D *et al.*, 2020.	A new and scalable methodology for predicting the yield of Final Test (FT) in semiconductor production.	Machine learning (Guassian Mixture Model)	High F1-macro test score demonstrating our Framework's resilience.	One drawback of encoders is that they introduce pointless numerical comparisons among various types.
Jang, S.J *et al.*, 2018	a novel method for quick production parameter optimization and data	Deep learning neural network	The suggested method effectively increases wafer map production at the beginning of the phase	To increase accuracy and prevent over-fitting, more training data is needed; the model cannot be created

			of design by forecasting yield of new wafer maps with new die sizes and placements.	using a straightforward regression technique.
Choi, H.C *et al.,* 2020	a novel method for quick production parameter optimization and data driven, precise electrical modeling of transistors, the most basic semiconductor units component.	Gradient Descent network	Our comprehensive optimization method swiftly and precisely modifies the manufacturing parameters to achieve the required figure-of-merits, while the neural-network based model immediately estimates figure-of-merits with competitors' precision.	Take more training time to take the output.
Aydt, H et al., 2011	A symbiotic simulation-based issue solver agent is presented that automatically handles decision-making difficulties concerning the several tools that make up a semiconductor manufacturing plant (fab).	Symbiotic simulation-based approach	higher throughput can be achieved contrasted with ordinary practice decision making.	There is a certain amount of time available to solve an issue because symbiosis simulation is utilized for short-term decision making.
O'Leary, J *et al.,* 2020.	The suggested approach is intended to leverage sensor data to identify the root causes of faults and automatically classify the defect state of wafers.	Multivariate LSTM-fully Convolutional Network (MLSTM-FCN)	The suggested MP-DN effectively categorizes and detects wafer flaws using sensor data from multi-stage processing machinery.	Noteworthy relationships found between various manufacturing methods.

4.2 Survey based on AI techniques to optimize process

A fault diagnostic prediction has been offered [42], as a way to get around quality control in semiconductor manufacturing. The utilization of GPUs yields better results with shorter training times. Using a case study from the semiconductor manufacturing business, which uses DNNs for vision-based position detection in their legacy equipment? When compared to an optimized DNN deployment, the observed result shows a 44% improvement in inference timing efficiency. When compared to other AI models, the deep learning-based domain adaption method for fault identification in semiconductor production [61] shows promise.

5. RESULT AND DISCUSSION

This section explains the results of analyzed research papers for semiconductor manufacturing by optimizing operations using AI. Research papers related to various methods for optimizing the operations for obtaining better output. Below figures explain various techniques used to optimize the operations.

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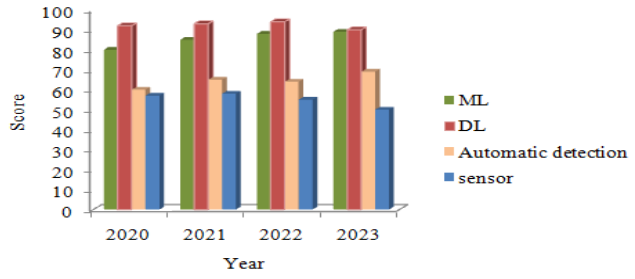

Fig 2: Score analysis for various techniques

Fig 2 explains the score analysis compared with various years. In each research paper the author explains by optimizing the operations in semiconductor manufacturing using various methods such as AI (ML and DL), automatically detecting faults and improving the process and by using sensors. Here, different year publications were considered to take the score analysis.

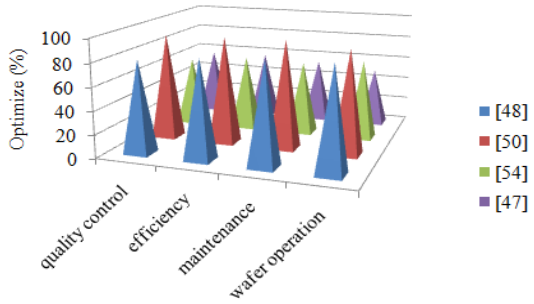

Fig 3: Optimize operations

In the fig 3 explains various authors optimize the operations in semiconductor manufacturing via various ways. Here, in the x-axis we have described quality control, efficiency, maintenance, wafer operations and these are some of the important parameters to optimize the operations of semiconductor manufacturing using AI.

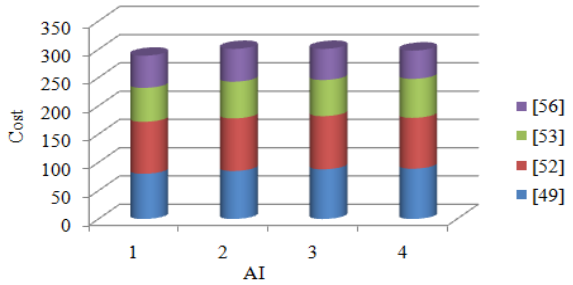

Fig 3: Cost analysis

In the fig 3 explains the cost analysis reviewed using various authors. In the growing semiconductor manufacturing cost is one of the main factors to minimize. The existing methods can take more cost to manufacture semiconductors. Here, AI is one of the emerging techniques to reduce the cost during manufacturing.

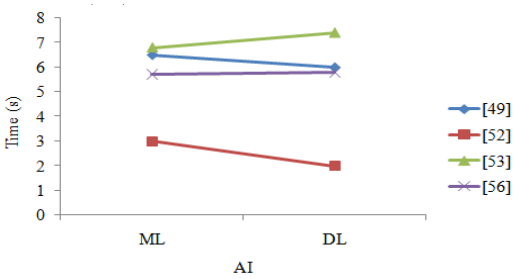

Fig 4: Time analysis

In the fig 4 explains the time analysis reviewed by various authors. Here, the x-axis represents AI algorithms and is compared with time. Compared with existing methods AI can reduce the processing time and scheduling time in the semiconductor manufacturing process.

CONCLUSION

Semiconductor manufacturing is one of the most growing hardware sectors and many of the electronic devices run it. In that optimizing operation process wafer, photolithography, etching etc is challenging nowadays. This paper reviewed various researches and they developed semiconductor manufacturing using various methods to optimize the operations. Also, we have discussed challenges to overcome the operations in semiconductor manufacturing. Here, integration of AI into manufacturing to optimize the operations is the easiest way to handle all those operations in a minimum time.

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