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Enhancing Energy Efficiency in VLSI Circuits: Strategies for Dynamic Power Dissipation Reduction

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Abstract
Dynamic power dissipation has historically been a major concern in VLSI circuits and systems, primarily resulting from changes in the output of logic gates. To address this issue, various techniques have been developed to reduce dynamic power consumption by targeting key parameters in the power consumption formula, including capacitance (C), supply voltage (V), clock frequency (f), and switching activity (α). This paper explores strategies such as clock gating, dynamic voltage and frequency scaling (DVFS), and power leakage minimization to enhance energy efficiency in VLSI circuits. Clock gating involves disabling the clock signal to components or the entire system when they are not in use, significantly reducing unnecessary switching activity and saving power. DVFS is a method for conserving energy in battery-powered devices by adjusting voltage and clock frequency based on workload requirements. Power leakage minimization strategies, such as threshold voltage adjustment and power gating, are crucial to reduce leakage currents and enhance energy efficiency in modern semiconductor devices.

Keywords: *VLSI, Power consumption, Dynamic power, Clock gating.*

INTRODUCTION

Area, performance, cost, and power consumption posed the biggest challenges to VLSI designers in previous decades. Nonetheless, in recent times, things have started to shift, with power consumption now receiving an equal amount of weight as area and speed estimates [1]. These days, electricity is the main component responsible for the amazing development and success of personal computers and telecommunication systems, which require complex functionality and fast calculation at low power output. Application and circuit-specific factors influence why power consumption should be decreased [2]. Reducing the weight and length of battery life while increasing packaging efficiency is the goal in the field of micro-powered, battery-operated portable devices, including cell phones [3]. For ultra-portable PCs with great performance, such as laptop and mobiles, the objective is to reduce the power dissipation of the electronics circuits of the system to a point which is about half of the total power dissipation. The goal is to minimize the power dissipation of the system's electrical circuits to a point where it is roughly half of the overall power dissipation, like in laptops and mobile devices[4]. Ultimately, the main objective of power reduction for high-performance non-battery-operated systems, like workstations, is to lower system costs while maintaining long-term device reliability. Process technology has thrust power to the forefront for all elements in such designs for such high performance systems. Power consumption from leakage has joined switching activity as the main power management concern at process nodes below 100 nm technology [5]. The reasons for cutting power consumption vary depending on the application. The objective in the category of small, portable, battery-operated devices, such PDAs and mobile phones, is to maintain a suitable weight and battery life while keeping packaging expenses to a minimum[6].

SOURCES OF POWER CONSUMPTION

When we recognized power consumption as a design constraint, Power per MHz is commonly used representation of a component. With a closer look at power dissipation, it becomes obvious that the subject is not that simple. Electric current is not constant during operation and peak power is an important concern [7]. The device will malfunction due to electro- migration and voltage drops even if the average power consumption is low. The equation for the average power consumption is given as

$P_{avg} = P_{dynamic} + P_{short} + P_{leakage} + P_{static}$

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So the total average power consumption depends on Dynamic power consumption, Short-circuit power consumption Leakage power consumption and static power consumption [8]. The leakage current which is primarily determined by the fabrication technology consists of reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage [9]. The short-circuit current which is due to the DC path between the supply rails during output transitions and the charging and discharging of capacitive loads during logic changes. The short- circuit and leakage currents in CMOS circuits can be made small with proper circuit and device design techniques. The main source of power dissipation is the charging and discharging of the junction capacitances. Switching activity is a measure for the number of gates and their outputs that change their bit value during a clock cycle. To toggle between logic zero and logic one can discharged and charged the junction capacitor [11-13]. The electric current that flows during this process causes dynamic power dissipation $P_{dynamic}$. The dynamic power is depend upon the capacitive output load Cout and the supply voltage Vdd and frequency of clock signal.

$Pdynamic = K\ Cout\ Vdd^2\ f$ [2]

K is the average number of positive transitions during one clock cycle and f the clock frequency. By reducing power supply will therefore have the greatest effect on saving power, taking into consideration that typically $P_{dynamic}$ is responsible for 80% of $P_{avg.}$

LOW POWER DESIGN STRATEGIES

There are different strategies available at different level in VLSI design process for optimizing the power consumption.

Table 1: Different strategies for optimizing power consumption.

Design Level	**Strategies**
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit / Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

LOW POWER TECHNIQUES FOR VLSI

There are many techniques that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools.

Table 2 Techniques for power reduction

Traditional Techniques	**Dynamic Power Reduction**	**Leakage power reduction**	**Other Power reduction Techniques**
Clock Gating	Implement Clock Gating	Minimize usage of low VT cells	Minimize Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance by custom design
Variable Frequency	Use variable frequency	Back Biasing	Power-efficient circuits
Variable Voltage Supply	Utilize variable voltage supply	Reduce Oxide Thickness	----------
Variable Device Threshold	Set variable device threshold	Variable island	Use FET

It is an overview of known techniques which gives an idea of what methodology is applicable. Optimizing for power entails an attempt to reduce one or more of these factors. To address the challenge to reduce power, the semiconductor industry has adopted a multifaceted approach, attacking the problem on four fronts:

1. Reducing chip and package capacitance: It can be achieved by process development like SOI with partially or fully depleted wells of semiconductors, CMOS scaling to submicron device areas, and advanced

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interconnect substrates such as Multi- Chip Modules (MCM). This process is very effective but very expensive and has its own pace of development and introduction to the market.

2. Scaling the supply voltage: This technique can be very effective in reducing the power dissipation in circuit, but requires new IC fabrication process. Supply voltage scaling also requires support circuitry for low-voltage operation including level-converters and DC/DC converters.
3. Employing better design techniques: This approach promises to be very successful because the investment to reduce power by design is relatively small in comparison to the other three approaches and because it is relatively untapped in potential.
4. Using power management strategies: The power savings that can be achieved by various static and dynamic power management techniques are very application dependent, but can be significant. Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offers another technique for minimizing power consumption. Interconnect plays an increasing role in determining the total chip area, delay and power dissipation, and hence, must be accounted for as early as possible during the design process.

POWER MANAGEMENT TECHNIQUE

Dynamic power dissipation, which results from changes in the output of logic gates, has historically been the primary source of energy consumption in VLSI circuits and systems. To mitigate this, various techniques aim to reduce dynamic power by focusing on key parameters in the power consumption formula: capacitance (C), supply voltage (V), clock frequency (f), and switching activity (α). Strategies include using smaller transistors, voltage scaling, optimizing clock frequencies, and minimizing switching activity through encoding and gating techniques, all with the goal of enhancing energy efficiency in VLSI circuits.

Clock Gating

Clock gating is a powerful method to reduce dynamic power consumption in electronic systems. It involves disabling the clock signal to components or the entire system when they are not actively in use. This technique effectively minimizes unnecessary switching activity in flip-flops, gates, and the clock distribution network, leading to significant power savings and a transition to a low-power STANDBY state when the system is idle.

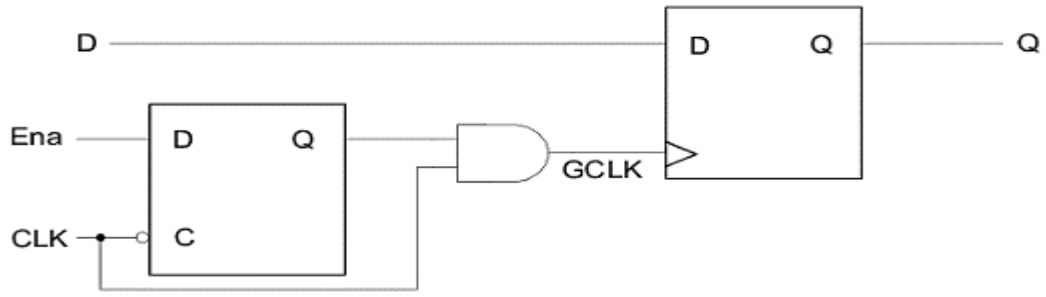

Figure 1. Clock Gating

Clock Gating - Verilog code

```
module ClockGatingExample (
  input wire clk,       // Main clock signal
  input wire enable,   // Enable signal for clock gating
  input wire data,     // Data input
  output reg q         // Flip-flop output
);
always @(posedge clk or posedge enable) begin
  if (enable) begin
    q <= data;// Flip-flop is clocked when enable is high
  end
end
endmodule.
```

Dynamic Voltage and Frequency Scaling

Dynamic Voltage and Frequency Scaling (DVFS) is a crucial method for conserving energy in battery-powered portable devices without compromising quality of service. It involves adjusting voltage and clock frequency to match workload requirements. In non-real-time scenarios, interval-based scheduling is employed, but it can struggle with variable workloads. Real-time applications benefit from techniques like intra-task voltage scheduling and software

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feedback loops, allowing for efficient energy management while meeting deadlines.

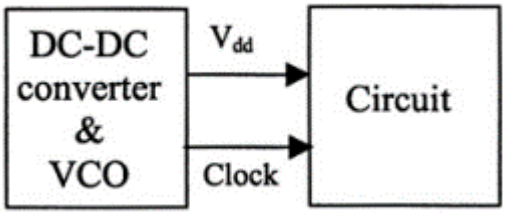

Figure 2. Dynamic Voltage and Frequency Scaling

Predicting future workload is a key challenge in Dynamic Voltage and Frequency Scaling (DVFS) techniques, whether applied in real-time or non-real-time scenarios. DVFS architecture typically includes a DC-DC converter for supply voltage and a Voltage Controlled Oscillator for clock generation, with voltage selection based on system performance needs. To simplify the design, using quantized supply voltage levels instead of continuous variations can reduce complexity, making it particularly useful when dealing with highly variable workloads.

Power Leakage Minimization

Lowering supply voltage in CMOS technology has reduced dynamic power consumption but poses challenges such as increased gate delays. To counteract this, the threshold voltage of transistors must be scaled down, which, unfortunately, leads to a significant increase in leakage currents. These unwanted currents can flow through reverse-biased diodes or tunnel through the gate oxide insulation to the substrate. Advanced techniques like high-K gate dielectrics are used to control these leakage currents. Sub-threshold current is another issue, driven by the minority carrier diffusion in OFF transistors. Managing these leakage currents is critical for enhancing energy efficiency and performance in modern semiconductor devices.

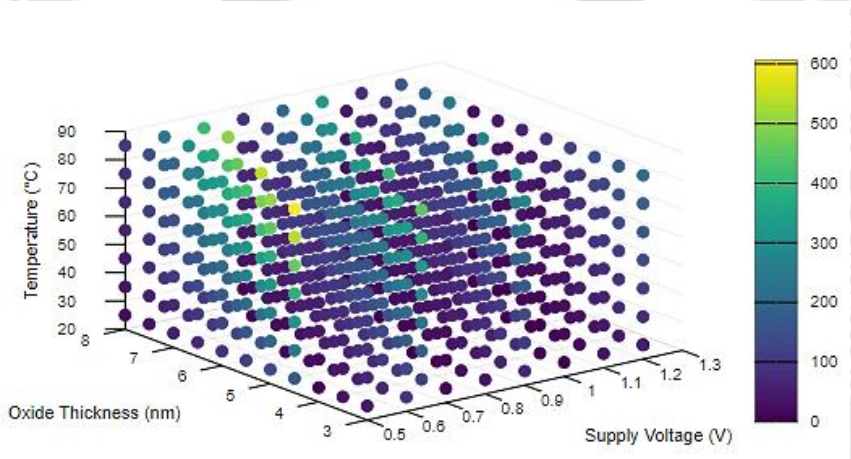

Figure 3. Leakage current trends

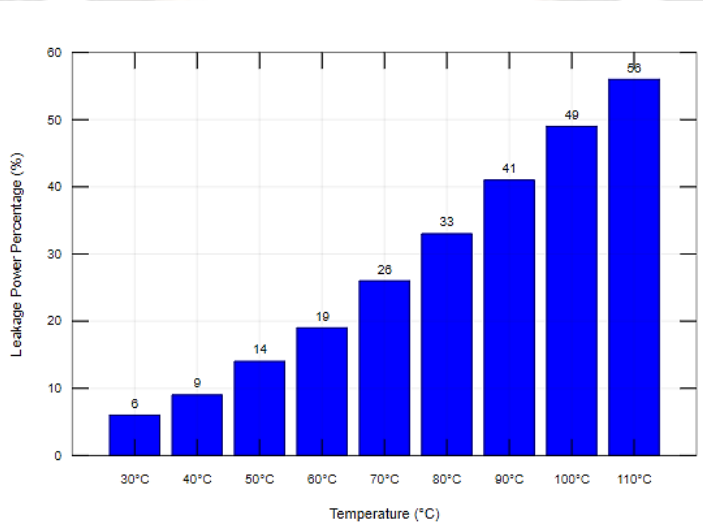

Figure 4. Power consumption of die function temperature

Figure 4 illustrates the power consumption of die function temperature. Notably, at 30°C, leakage power contributes to only 6% of total power, but at 110°C, it spikes to 56%. This underscores the importance of leakage power reduction. Three methods are discussed: power gating, threshold voltage adjustment, and input value-dependent techniques. These strategies are applicable during system sleep states and effectively mitigate leakage power, promoting energy-efficient electronic designs.

CONCLUSION

This paper addresses the persistent challenge of dynamic power dissipation in VLSI circuits and systems. It introduces effective strategies such as clock gating to reduce unnecessary switching activity, Dynamic Voltage and Frequency Scaling (DVFS) for efficient energy management, and methods to tackle power leakage. These approaches, when applied wisely, contribute to energy-efficient VLSI systems that meet the growing demands for performance and functionality while sustaining the development of electronic devices in the future.

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