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Efficient Design & Analysis of Phase Locked Loop Using High Performance Voltage Control Oscillator with Four Outputs for Communication Standard Applications

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Abstract: -
Phase Locked Loop (PLL) with multiple outputs in low power and high speed is designed with 45nm size IC's. Proposed PLL is designed using BSIM4 model for n and p channel CMOS transistor which is supported by microwind 3.1 VLSI software. To obtain the layout of proposed PLL, CMOS circuit of each element of proposed PLL is converted into physical layout using lambda based rules of microwind 3.1 software. After cascading the layout of each element, final layout is obtained. This paper particularly focuses on analysis and design of phase-locked loop with low power consumption with high performance using VLSI technology. When compared to conventional design, here focus is made on VCO. The input frequency is collected from external source which is used to generate four frequencies provided for the circuits of communication standard in high-speed Integrated Circuits.

Keywords: **-** VLSI (Very Large-Scale Integration), NB (Normal Distribution), CMOS (Complementary Metal Oxide Semiconductor), HP-VCO (High Frequency-Voltage Controlled Oscillator)

Introduction: -
Wireless transceivers must still be able to generate a wide range of frequencies in order to up convert the outgoing data for transmission and down convert the received signal for processing. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation and distribution in microprocessor and frequency synthesis in wireless application.

Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock such as injection locking. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application. A phase locked loop (PLL) is widely applied for different purposes in various domains such as communication and instrumentation. In the microwave range they have been applied in frequency synthesis and phase recovering among others.

Due to the advantage and current demand in communication technology, the effort has been taken to design proposed Phase-Locked Loop (PLL) using VLSI technology. The question arises, why we have chosen the 45 nanometer (nm) CMOS/VLSI technology. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. Some of the key features of 45 nm technologies are as given in table 1.1 below.

S.No.	Parameter	Value
1	VDD (V)	0.85-1.2 V
2	I_{off} N (nA/um)	5-100
3	I_{off} P (nA/um)	5-100
4	Gate dielectric	SiON, HfO_2
5	No. of metal layers	6-10

Table 1: Specifications of 45 nm technologies for PLL

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Organization of Work & Methodology: -

The Phase locked loop is a feedback system. It is a basic building block used in communications system such as mobile phones, which may contain up to 5 PLL's. Another important application is in motor speed control. For optical disk drive (ODD's) as found in DVD's and CD players. The basic PLL can be analog or digital. A good review of PLL's from a control engineering perspective can be found in various references. Thus the research describes the basic component of the PLL and how to build and analyze the proposed PLL using 45 nm VLSI technology.

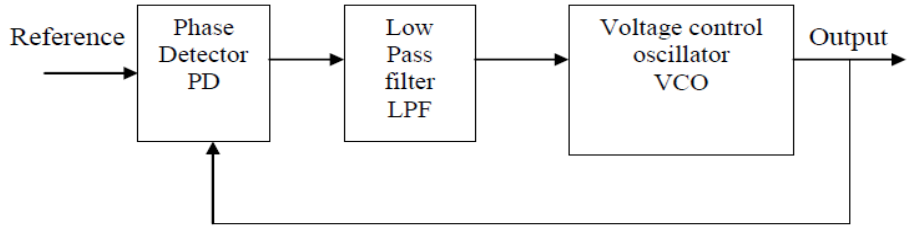

Fig. 1 Block diagram of PLL with Conventional VCO

To achieve the proposed phase-locked loop, different methodology and techniques can be used for research. The MICROWIND3.1 program allow to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

High Performance-Voltage Controlled Oscillator (HP-VCO): - A key circuit use in modern communication is voltage control oscillator (VCO). VCO's output is an AC waveform whose frequency is dependent upon the input voltages. In today's wireless communication system, greater maximum frequency required by the VCO with respect to the digital phones that use this circuit, low power consumption, small size & low fabrication cost are important design factor. The layout of VCO which is develop by us is a modified design of high performance VCO. This is an optimum design for use in industries at 45 nm VLSI technology. In the estimated design more emphases are given on power consumption, layout design and many more. This report is a brief study of high performance VCO on 45 nm VLSI technology to achieve some objectives as mention above.

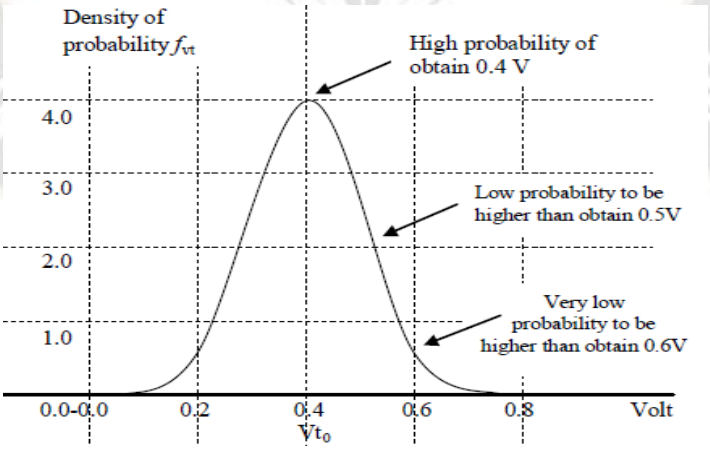

Fig. 2 The normal distribution of Vt, with a typical variation of 10%

The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The high performance VCO provides very good linearity as compared to previous one.

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Design of Efficient PLL with HP-VCO Using 45 nm Technology: -

Since the multiple outputs Phase Locked Loop (PLL) provides multiple clock generation, it is to be needed to design PLL with multiple output for modern communication Engineering applications with low power, high stability and low jitter. In this phase locked loop the conventional VCO is replaced by high performance VCO. Fig 9.1 shows the block schematic of PLL with high performance VCO. The high performance VCO provides very good linearity. The principle of this VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a p- channel MOS in series, controlled by Vcontrol, and a pull-down n-channel MOS, controlled by Vplage. The delay dependence on Vcontrol is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point Vc. The rise edge is almost unchanged.

For low power, low leakage transistors are used and will compromise on little frequency. Also there will be a shutdown input in proposed circuit which will bring the PLL to hold or there can be a pin, which if enabled then will make the PLL frequency to half.

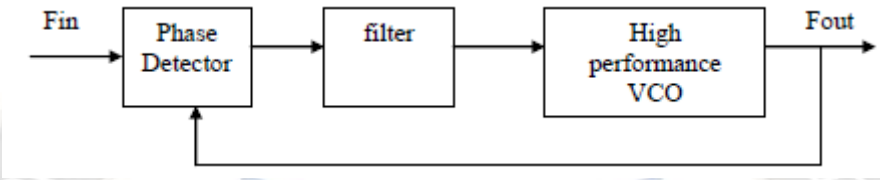

Fig. 3 Schematic Diagram of Phase locked loop with high performance VCO

Sr. No.	Vdd(V)	freq(GHz)
1	0.80	6.211
2	1.00	6.211
3	1.20	7.770
4	1.40	9.116

Table 2: Voltage variation of V_{DD} verses frequency of node V_{high}

Result Analysis of PLL-

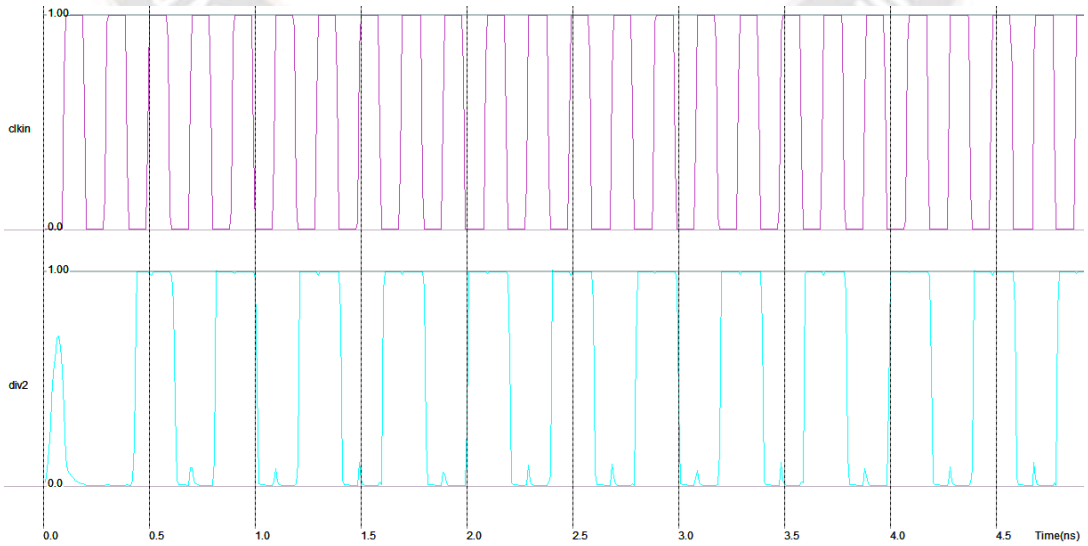

Fig. 4 Voltage verses Time waveform of Dregister/Dflipflop

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Since the PLL, provide multiple clock generation, it is a research problem to design PLL using 45nm process technology parameters which will offers high speed performance at low power. Optimum layout for 3.45 GHz PLL is designed using high performance VCO, which is almost stable when Vc reaches to 0.501 volt. From the parametric analysis of design tool shown in fig 9.5, it is observed that the power dissipation measured by VDD at 1Volt is found 0.113miliwatt, which shows that power consumption is very low.

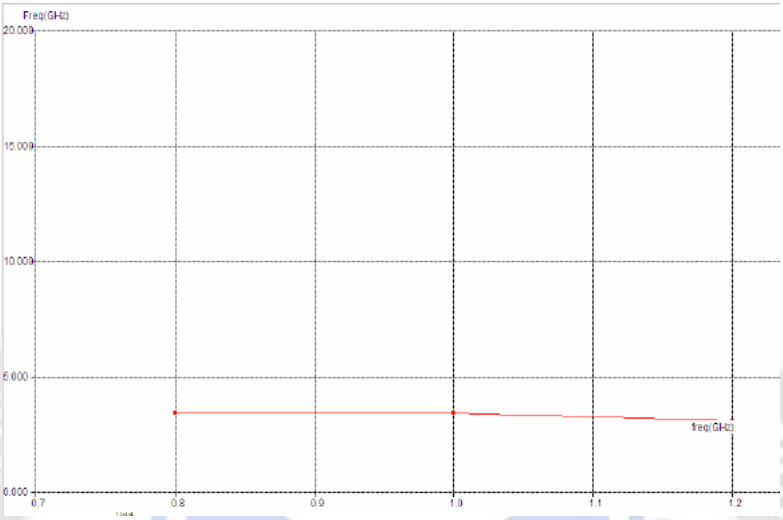

Fig. 5 Voltage variation of vdd verses frequency of node Vhigh

As a result of technology scaling, there are increased process variations of circuit parameters such as the transistor channel length and transistor threshold voltage. The increased process variations can have a significant effect on circuit performance and power variations also have an impact on how exactly a parallel system should be designed. This layout design is implemented using 29 NMOS along with 28 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the lambda based rules of microwind 3.1 software.

Conclusion: -

The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of VDD emerges as a very effective means of limiting the power consumption. For the proposed PLL, power supply VDD of 1 volt is used. The optimum, high efficient chip design of low power PLL with multiple (Four) output using 45nm VLSI technology. For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The modelling of CMOS device behaviours are analyzed with the equations including threshold voltage, short channel effect narrow channel effect, electron temperature effect, hot carrier effect and capacitance model. Finally, the BSIM SPICE models BSIM4 are summarized for deep-submicron CMOS transistor.

For low power, low leakage transistors BSIM4 are used and compromised on little bit frequency. Also there is shutdown input in proposed circuit which brings the PLL to hold.

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