International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 11
Article Received: *25 July 2023* ***Revised:*** *12 September 2023* ***Accepted:*** *30 November 2023*

Binary 32-Bit Adder Design Using Carry Look Ahead Adder in Electric

[1]Lahari G R , [2]Ms. Navya K T
[1]Dept. of Electronics and Communication
Manipal Institute of Technology
Manipal Academy of Higher Education
Manipal-576104, India
[2]Asst. Professor-Senior scale
Dept. of Electronics and Communication
Manipal Institute of Technology
Manipal Academy of Higher Education
Manipal-576104, India
Email: laharig8@gmail.com , Email:navya.kt@manipal.edu

Abstract**—** Adders are a part of integrated circuits of today almost everywhere. Smaller and lower-power arithmetic circuits are also required by the rapidly evolving computing industry, in addition to faster arithmetic units. To satisfy its needs, the adder needs to be both speedy and effective in the chip area. We used the Carry Look Ahead Adder (CLA) to build a 32-bit adder utilizing eight 4-bit adders for our project. Because it propagates carry before the sum output is reached, it takes less time than other adders and performs brilliantly, earning it the nickname "fast adders." We used LT Spice simulation to create the CLA's schematic and architecture. 45nm technology was used, with an area of 898.6 μm^2 and a power efficiency of 0.215 μ watt.

Index Terms**—** *Adder, CMOS, Electric, CLA, VLSI.*

I. INTRODUCTION

Addition is the basic building block for numerous processing operations in electronics, including Arithmetic Logic Units, addresser, multiplier, and so on. One typical technique used to simplify a digital circuit's construction and operation is the addition of a certain number of bits. A one- bit full adder design is created and simulated for transient simulation. The CLA is a combination of ripple carry adder and carry look ahead logic unit. The is analogous to the carry-skip adder in that it assesses both Carry generate and carry propagate signalsto see if the first group creates a carry instead of waiting for a ripple from the previous adder. In [1], the addition of a given number of bits is basic operation to reduce the difficulty of the circuits. All the types of 4-bit adders are compared that have been designed, simulated and verified using the Xilinx synthesis tool.

In [2], the adiabatic logic behind 16-bit adder using carry look ahead adder is explained. Also, it reduces the power consumption during the propagation and computation.

In [3], a 1-bit full adder cell is proposed which is less power consuming and high performance. For the simultaneouscreation of XOR and XNOR functions, the Gate Diffusion Input (GDI) technique was applied.

In [4], explains that these the large family of addition structures as it shares minimum logical depth. It is possible to obtain accurate results both in area and low power/cost than other cases, as its transitional structure shows the trade- offs amongst the amount of internal wiring and the fanout of intermediate nodes.

If the implementation was using ripple carry adder, it faces the propagation delay problem. In some technique there is more difficulties in the circuits as well as in the operation. So, we have implemented CLA to overcome from these problems which is having less propagation delay.

II. CARRY LOOK-AHEAD ADDER

I. 4- bit CLA

CLAs depends on two terms, Carry Propagate and Carry Generate, which are denoted by C_p and C_g. The propagate bit is passed on to the next stage, and the generate bit is utilized to generate the carry out bit, which isdistinct to the input carry bit. CLA of 4-bit architecture is shown in Fig1.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 11
Article Received: *25 July 2023* ***Revised:*** *12 September 2023* ***Accepted:*** *30 November 2023*

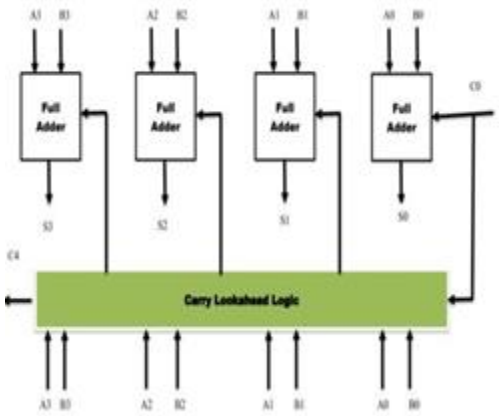

Fig1: 4-bit CLA block diagram

In Fig1 [1], C_0 input is given to both one-bit full adder and carry look ahead logic. As C_0 is applied to carry look ahead logic circuit the propagating carry inputs for other full adders is applied with reduced propagation delay. It will calculate other next stage carry inputs without waiting for previous stage output instead it will calculate as soon as C_0 is applied. This is one of the main advantages of CLA.

Next, we can express the output sum Si and carry Ci as follows:

- $S_i = P_i \oplus C_i$ ……. (a)
- $G_i + (P_i * C_i) = C_{i+1}$…… (b)

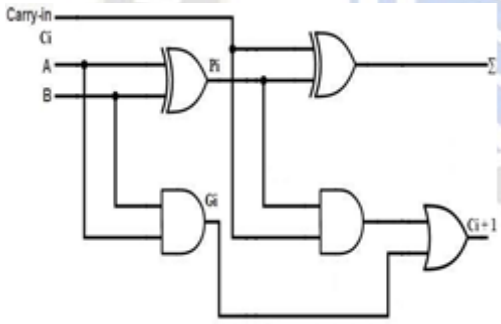

Fig2: Carry generate and propagate circuit using logic gates.

The AND, OR and XOR gates needed to calculate the single bit generate and propagate signals using two inputs, A_i and B_i.

From Fig2 [5], the equation for 'Carry generate' and 'Carry propagate' can be written as,

- $G = AB$ (where G represents carry generator)
- $P = A \oplus B$ (where P represents carry propagator)

Based on equation (b), the carries of the first four bit are as follows:

$C_1 = C_0.P_0 + G_0$……. (c)
$C_2 = C_1.P_1 + G_1$……. (d)
$C_3 = C_2.P_2 + G_2$…….....(e)
$C_4 = C_3.P_3 + G_3$……..... (f)

By substituting C_1, C_2 , and C_3 in equation (c) to (f) The following equations are obtained:

$C_1 = C_0.P_0 + G_0$

$C_2 = C_0.P_0.P_1 + G_0.P_1 + G_1$

$C_3 = C_0.P_0.P_1.P_2 + G_0.P_1.P_2 + G_1.P_2 + G_2$

$C_4 = C_0.P_0.P_1.P_2.P_3 + G_0.P_1.P_2.P_3 + G_1.P_2.P_3 + G_2.P_3 + G_3$

II. 32-bit CLA

Fig 3 consists of eight 4-bit blocks to form a 32-bit carry-look ahead adder. Each single block represents a CLA of 4-bit which computes the sum of 4-bit at faster rate and also calculates carry propagate and generate which passes to thenext stage. The carry in is applied to the 4-bit CLA from logic circuit.

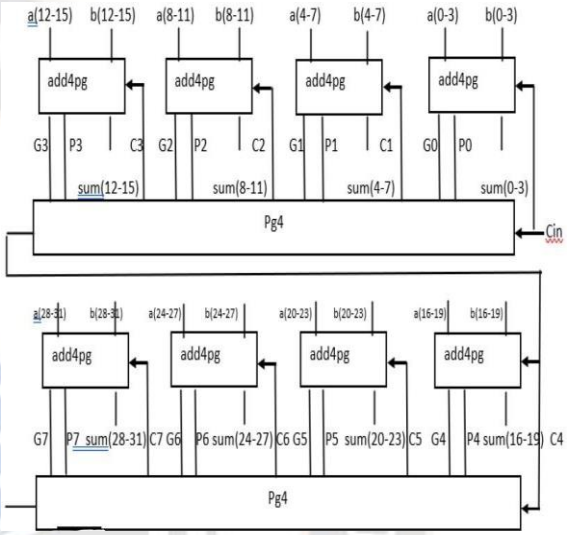

Fig3: 32-bit CLA block diagram

III. IMPLEMENTATION

A. Implementation CLA of 4-bit

In Electric binary, design of a 4-bit CLA has been designed as shown in Figure9. The proposed technique computes carry-out terms using the carry- propagate and carry generate. The suggested 4-bit CLA architecture's performance parameters were simulated and validated by using Electric VLSI design system. Simulations were run using Electric VLSI design system with a 45 nm technology and LT Spice software in order to accomplish this.

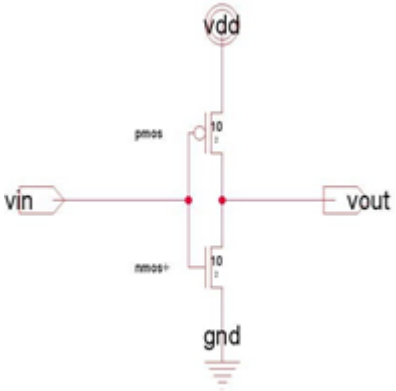

Fig 4: Schematic of NOT gate

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 11
***Article Received:** 25 July 2023 **Revised:** 12 September 2023 **Accepted:** 30 November 2023*

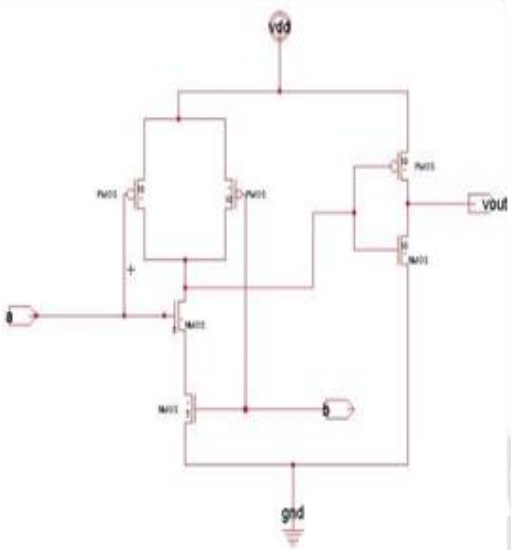

Fig5: Schematic of AND gate

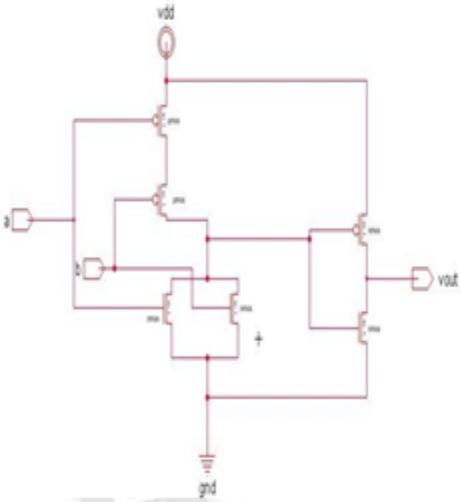

Fig 7: Schematic of OR gate

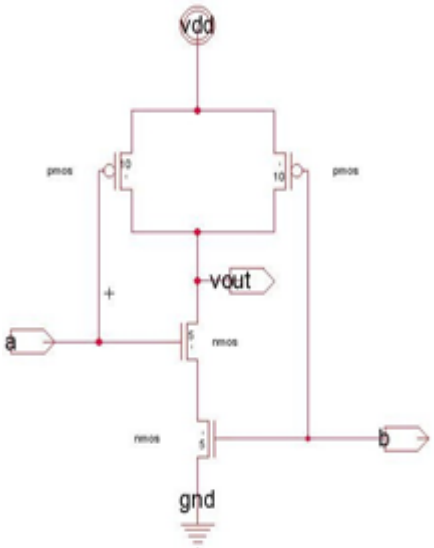

Fig 6: Schematic of NAND gate

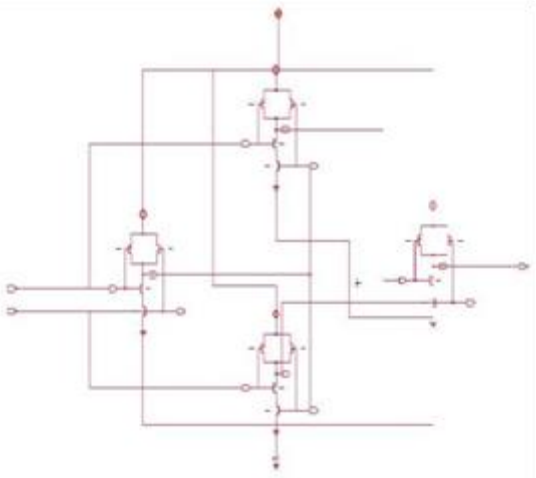

Fig 8: Schematic of XOR gate

The above schematic from Fig5 to Fig8 has been used to compute one-bit adder, generate and propagate circuit and logic circuit to produce carry out. Using all the schematics in Fig4, Fig5, Fig6, Fig7 and Fig8 a 4-bit CLA schematic isdesigned.

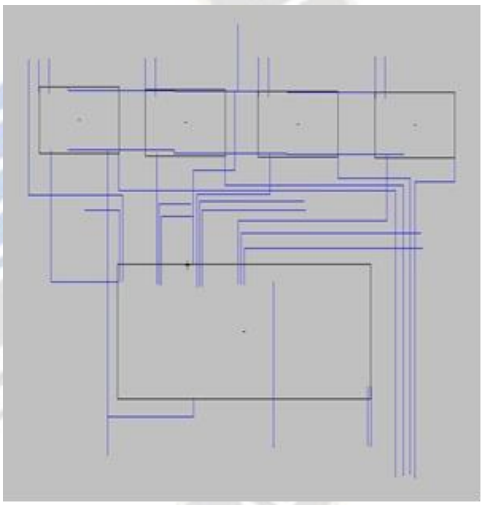

Fig 9: 4-bit CLA Schematic

The Figure10 shows the transient analysis of 4-bit CLA which is simulated in LT spice using Electric binary at 45nm technology.

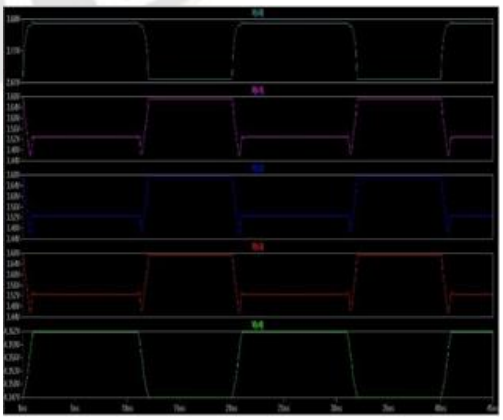

Fig 10: 4-bit CLA Transient Analysis

B. Implementation of CLA of 32-bit using Electric

In Electric VLSI Design System, the 32-bit CLA has been designed using eight 4bit CLA along with Carry generation and Carry propagation circuits. The below figure11 shows the schematic of 32-bit CLA.

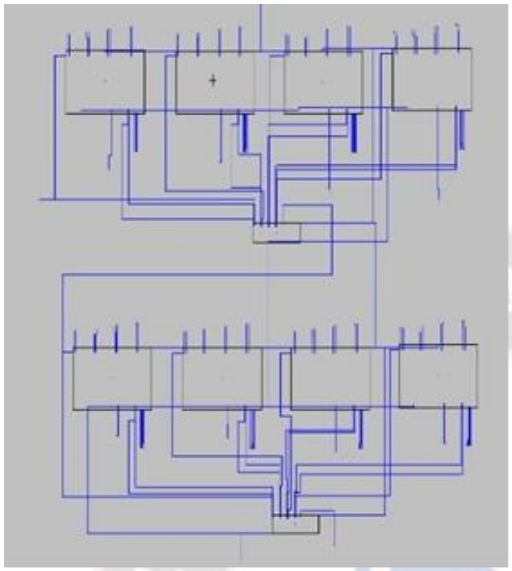

Fig 11: 32-bit CLA Schematic

Comparison Table

Technology	Power (in μ watt)	Area (in μm^2)
45nm	0.215	898.6
90nm	1.40	4549.9
180nm	2.65	8935.5

The Figure12 represents the transient analysis of 32-CLA which is simulated in LT spice using Electric binary at 45nm technology.

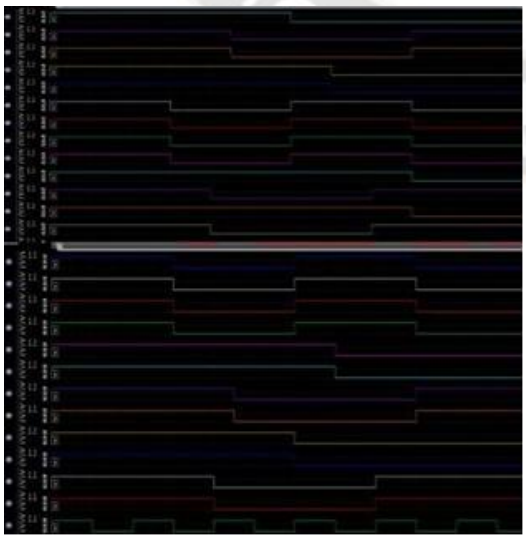

Fig 12: 32-bit CLA Transient Analysis

IV. CONCLUSION

In order to minimize the adder's carry propagation latency, the CLA is highly utilized. Though compared with other different logic design approaches CLA logic calculates carry propagating to the next stage as soon as inputs are applied. The schematic of 4-Bit adder and 32-bit adder is implemented using CLA logic designed using electric binary 9.07 tool with less Power efficiency of 0.215 μ watt and Area 898.6 μm^2.

REFERENCES

[1] AainaNandal and Dinesh Kumar “A Study on Logic Circuits for Low Power Applications” Special Issue –2017.
[2] Ashwini A. Pote and Prof.Ashwini Desai “Design and Implementation of Low Power 16-bit Carry lookahead Adder Using Adiabatic Logic”.
[4] PoonamKadam “Comparative Analysis of Different types of adder Techniques”
[5] A comparative study on adders by Bhavani Koyada, N. Meghana 2. Comparision between various typesof adders by Jasbir Kaur, Lalit Sood
[6] Bazzazi and B. Eskafi, “Design and Implementation of Full Adder Cell”, Volume 2, 2009 4. S. Knowles, (June 2001)
[7] "A family of adders", Proceedings of the 15 IEEE Symposium on Computer Arithmetic. Vail, Colarado, pp.277-281 5.
[8] Fast carry lookahead adder by K. Raahemifair, M. Ahmadi 6. R. Zlatanovici and B. Nikolic, (2003)
[9] Arithmetic Circuit Design by University of California, Davis (2000).