*International Journal on Recent and Innovation Trends in Computing and Communication*
*ISSN: 2321-8169 Volume: 11 Issue: 11*
***Article Received:*** *25 September 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *30 November 2023*

# "Design and Implementation of Low power, High Performance FINFET –Based SRAM Cells".

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***Abstract:*** This research paper presents a comprehensive analysis ofelectrical simulations of FinFET-based SRAMs conducted across various technological nodes to conduct a comprehensive examination of static and energy liability behavior.. The second step, we are designing 14nm, 12 nm and 7 nm FinFETs and extracting their characteristics by using Sentaurus TCAD. Simulated results of the device shows that it can be governed at the nanometer - scale regime and itsperformance is analyzed in terms of power consumption, propagation delay, power delayproduct (PDP) for nanoscaledtechnologies.Furthermore a digital register-transfer level (RTL) structure focusing on the implementation of static random access memory (SRAM) was studied meticulously to evaluate read and write operations controlled by configurable bit lines with multi-level voltage applications. CMOS circuits are implemented using the MICROWIND tool, facilitating accurate representation and simulation of SRAM components. The analysis includes an assessment of voltage-versus-current characteristics and an evaluation of the structural parameters of Double Gate (DG) FinFET transistors within the RTL structure. The 6T SRAM cell architecture is explored, highlighting its importance in the memory hierarchy and emphasising stability and performance considerations. The study also scrutinises system performance concerning input frequency through delay lines, providing insights into responsiveness and speed. Simulation analyses across different CMOS technologies and frequencies offer a thorough understanding of SRAM behaviour, aiding in optimisation and refinement for practical applications.

***Keywords:*** SRAM ,FinFET, High-Performance, Low-Power,Power Consumption,SPICE, TCAD,MICROWIND Tool

## Introduction

As the demand for portable consumer devices with increased functionality, long battery life, and small physical size continues to rise, there's a critical need to balance ultra-low power consumption with area-efficient design [1]. This challenge is particularly evident in devices like wristwatches and hearing aids, where both energy efficiency and compactness are paramount [2].

One straightforward approach to minimize SRAM energy consumption per operation is by reducing the supply voltage (VDD). This reduction not only decreases active power (proportional to $CVDD^2$) but also mitigates leakage power. However, excessively lowering VDD can lead to increased delay times, resulting in the integration of leakage power over longer intervals and consequently raising the power-delay product (PDP). Research has demonstrated that achieving a minimum PDP necessitates operating in the sub-threshold region [3-5].

Implementing SRAM in the sub-threshold region involves a delicate trade-off between stability and area efficiency. Traditional 6T SRAM designs rely on ratioed current strengths determined by transistor lengths and widths to achieve desired read/write margins [6]. However, the heightened sensitivity to threshold voltage (VT) process variations and degraded Ion/Ioff ratios make these length/width-based ratios unreliable for sub-VT SRAM designs.

To enhance read/write stability in subthreshold SRAM, additional peripheral circuitry or modifications to the 6T memory cell design may be necessary, albeit at the expense of increased chip area [7]. This trade-off between area and performance underscores the importance of investigating optimal strategies for subthreshold SRAM designs.

## Methodology

In the proposed system, Comparative performance analysis of FINFET- based SRAM have been performed which

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comprises of different Technological nodes and design parameters.A three-dimensional model of a FinFET SRAM was initially developed using SentaurusTM TCAD. We have more control over the physics of the device, such as where ionizing particles hit, than we do in SPICE simulations. The work functions of the metals were fixed at 4.623 eV, and the physical characteristics needed to calibrate the SentaurusTM tool's transistor model for a 14 nm , 12 nm and 7nm as well as a comprehensive analysis has been undertaken, focusing on the digital Register-Transfer Level (RTL) structure to assess the implementation of static random access memory (SRAM). The core functionality of the system revolves around read and write operations, which are executed in relation to the configurable bit line. Notably, the read and write processes are meticulously controlled by applying voltages with multi-level values.

The 6T SRAM cell, being a fundamental building block in the memory hierarchy, plays a pivotal role in the system design. Comprising six transistors, this configuration ensures the static storage of a single bit of information. The stability of the stored data is maintained as long as power is consistently supplied to the circuit, emphasising the static nature of SRAM.

Furthermore, the system's performance is scrutinised concerning the input frequency of operation through delay lines. This evaluation is crucial for understanding how effectively the SRAM implementation can operate under different frequency conditions. By assessing delay lines, the system's responsiveness and speed in processing read and write operations can be gauged, providing valuable insights into its overall efficiency.

**Structural Parameters:**

The important structural parameters of a Double Gate (DG)FinFET transistor are depicted in figure 1.

***$T_{Si}$:*** Thickness of silicon fin determined by the space betweenfront and back gate oxides.

***$T_{OXF}$, $T_{OXB}$***: Front- and back-gate thickness of oxide layer.

***$H_{FIN}$***: Height of silicon fin decided by the distance betweentop gate and buried oxides.

***$H_{GF}$, $H_{GB}$:*** Front- and back-gate thickness.

***$L_{GF}$, $L_{GB}$***: Physical front- and back-gate lengths defined by thespacer gap.

***$N_{S/D}$:*** Source/drain doping.

***$N_{BODY}$:*** Body doping.

***$L_{SPF}$, $L_{SPB}$***: Front- and back-gate spacer thickness.

***$L_{UN}$:*** Gate-drain/ source underlap.

***FP, GP:*** Fin pitch, Gate pitch.

***Wfin***: Geometrical channel width. It is determined by Wfin=2Hfin+ Tsi.

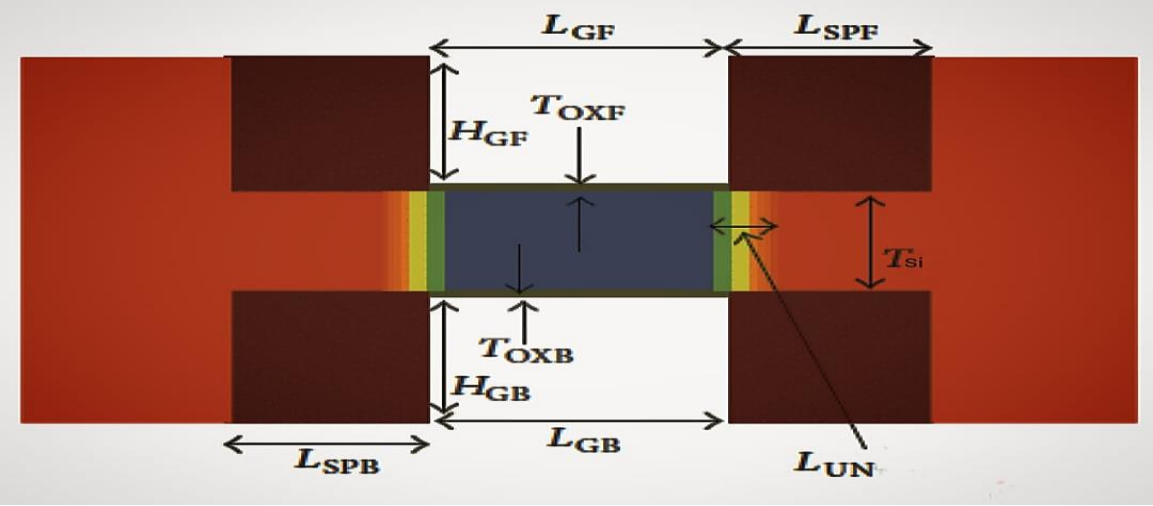


**Figure. 1:** 2D Finfet Structure

By considering these structural parameters, the methodology ensures a comprehensive analysis and accurate representation of the DG FinFET transistors' behavior within the implemented digital RTL structure, facilitating the evaluation and optimization of SRAM performance.

**Here is a high-level overview of the 6T SRAM cell:**

1. Bitlines (BL and BLB): These are the lines that carry the actual data. BL (Bitline) is used to read the data, and BLB (Bitline Bar) is the complement of BL.
2. Wordlines (WL and WLB): These lines control the access to the memory cell. WL (Wordline) is used to

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write data into the cell, and WLB (Wordline Bar) is the complement of WL.

3. Access Transistors (T1 and T2): These are NMOS transistors that connect the storage nodes (nodes storing 0 and 1) to the bitlines when the wordline is activated.

4. Cross-Coupled Inverters (Q and Qn): These are formed by the complementary metal-oxide-semiconductor (CMOS) inverters. They store the data in a latch configuration.

Here is a simplified description of the read and write operations:

**Read Operation:**

- Apply the appropriate voltages to the wordline and bitlines.
- The access transistors (T1 and T2) connect the storage nodes to the bitlines.
- The data stored in the SRAM cell is sensed by the sense amplifiers connected to the bitlines.

**Write Operation:**

- Apply the appropriate voltages to the wordline and bitlines.
- The access transistors (T1 and T2) connect the storage nodes to the bitlines.
- Change the state of the storage nodes based on the desired data.
- The new data is latched into the SRAM cell.

When designing a 6T SRAM cell, it's crucial to consider various parameters like read and write stability, static noise margin, access times, and power consumption. Additionally, the design needs to account for process variations and technology scaling.

**Working of 6T-SRAM**

A Static Random-Access Memory (SRAM) cell is a fundamental building block of computer memory that operates in three distinct modes: retention mode, read mode, and write mode. Each mode serves a specific purpose in storing and retrieving data.

**Read Mode**

The process of reading from an SRAM cell should be quite straightforward. It involves enabling the Wordline, which allows the access transistors (AC1 and AC2) to turn on. This action should facilitate reading the state of the SRAM cell using only one access transistor and a bit line (either BA and AC1 or BL and AC2).

However, in practice, this process is not as efficient as one might expect. This inefficiency arises from the fact that the bit lines, which are used to store the data in SRAM cells, tend to be relatively long and have significant parasitic capacitances. These parasitic capacitances slow down the read process significantly.

To speed up the reading process, a more complex technique is employed. First, both bit lines (BA and BL) are pre-charged to a high voltage level. This pre-charging prepares the bit lines for a more rapid read operation.

Once the bit lines are pre-charged, the next step involves triggering the Wordline. This action allows the access transistors (AC1 and AC2) to turn on, which should facilitate the reading process. Depending on the stored data in the SRAM cell, there is either a minor drop in the voltage in the bit line (BL) when the pull-down (PD) is enabled and the pull-up (PU) is disabled, or a slight increase in the voltage in the bit line (BL) when the PU is on, and the PD is off.

So, while theoretically, SRAM cell read operations appear simple, practical considerations such as bit line length and parasitic capacitance necessitate more complex techniques to ensure efficient and speedy reading. This involves pre-charging the bit lines and carefully managing the state of the access transistors and bit lines during the read process to ensure accurate data retrieval.

**Write Mode**

In an SRAM cell, the data stored can be set to any binary value, whether it's a "0" or a "1." This operation involves manipulating the bit lines (BL and BLB) in the SRAM cell. To write a "0" to the cell, you set BL to 1 and BLB to 0. This action changes the state of the flip-flop within the SRAM cell, effectively storing a "0."

Conversely, if you want to write a "1" to the SRAM cell, you would invert the bitline values. This process involves changing the values of BL and BLB such that BL becomes 0 and BLB becomes 1. This operation reaffirms the wordline, effectively locking in the value to be stored in the SRAM cell as "1."

.Table :1 presents design considerations for transistor parameters across three different technology nodes: 14 nm,

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12 nm, and 7 nm. Let's describe each parameter and analyze the results:

**Table1:** Design Considerations

| Parameters | **14 nm** | **12 nm** | **07nm** |
|---|---|---|---|
| VDD(v) | 0.81 | 0.73 | 0.7 |
| $L_{GB}$(nm) | 14 | 12 | 7 |
| $L_{GF}$(nm) | 1.2 | 1.1 | 1.14 |
| $T_{OXF}$(nm) | 8 | 7 | 7 |
| $T_{OXB}$(nm) | 23 | 21 | 18 |
| $T_{Si}$(nm) | 23 | 21 | 18 |
| $H_{FIN}$ (nm) | 23 | 21 | 18 |
| $H_{GF}$ (nm) | 23 | 21 | 18 |
| $H_{GB}$ (nm) | 23 | 21 | 18 |

**Simulated Results:**.

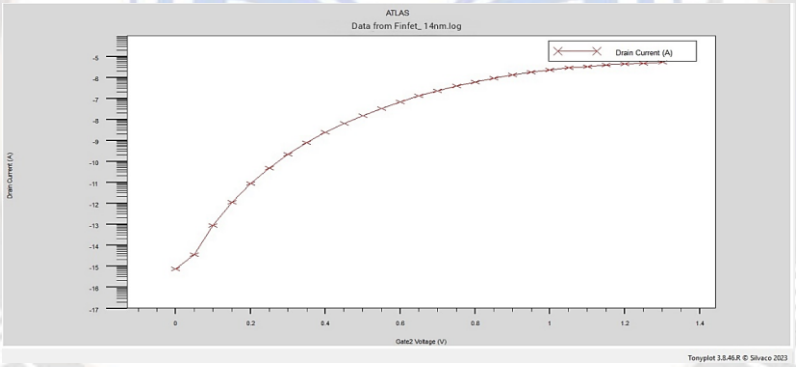


**Figure2:** Simulated ID-VGSTransfer characteristics of 14nm Finfet Structure for drain voltage variation

This figure illustrates the relationship between drain current (ID) and gate-source voltage (VGS) for a 14nm FinFET structure under different drain voltage conditions. It provides insights into how the transistor behaves in response to varying gate voltages and drain voltages, revealing important characteristics such as threshold voltage, saturation behavior, and transconductance.

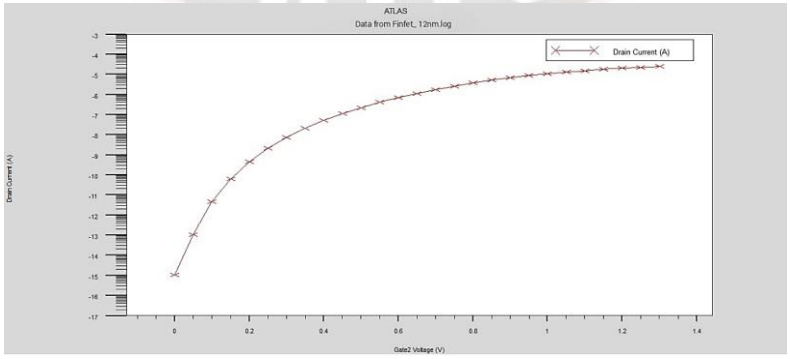


**Figure3:** Simulated ID-VGS Transfer characteristics of 12nm Finfet Structure for drain voltage variation

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Similar to Figure 2, this figure represents the ID-VGS transfer characteristics, but for a 12nm FinFET structure. By comparing with the 14nm structure, one can observe any improvements or differences in transistor behavior due to the technology node shrinkage.

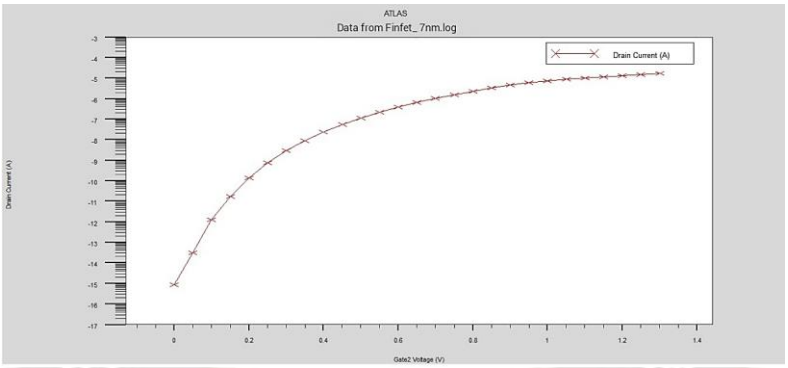


**Figure4:** Simulated ID-VGS Transfer characteristics of 7 nm Finfet Structure for drain voltage variation

This figure depicts the ID-VGS transfer characteristics for a 7nm FinFET structure. Like the previous figures, it showcases the transistor's behavior under varying gate and drain voltages. A comparison with Figures 2 and 3 allows for an assessment of how transistor performance evolves as technology nodes advance.

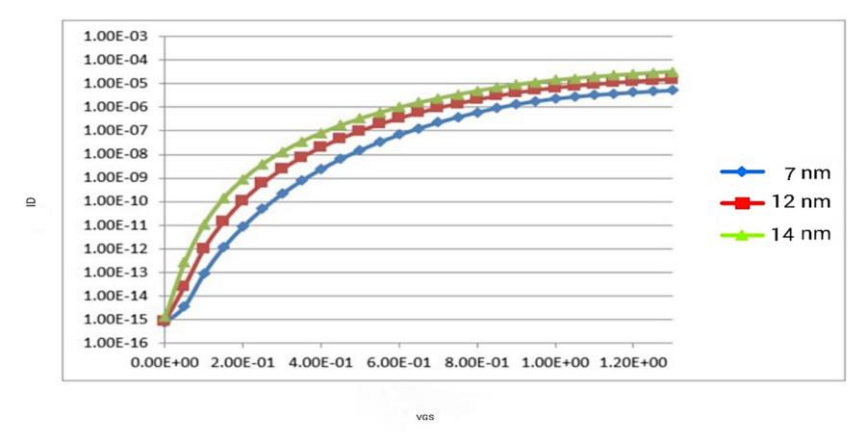


**Figure5:** ID-VGS Characteristic with Various Drain Voltages

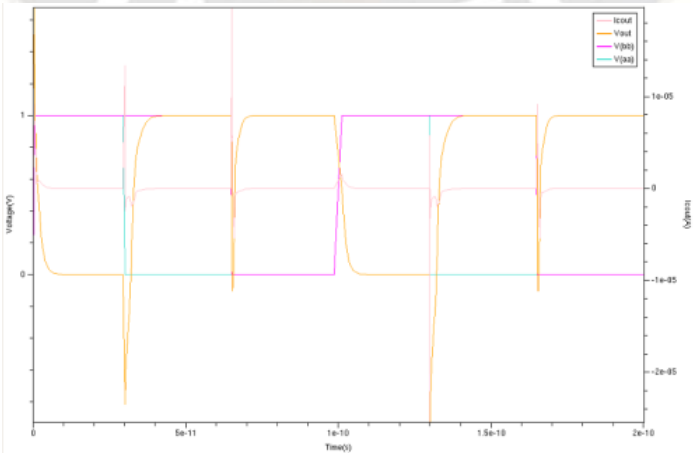


**Figure 6:** Simulated Transient input/output characteristics of 14nm TechnologyFinfet.

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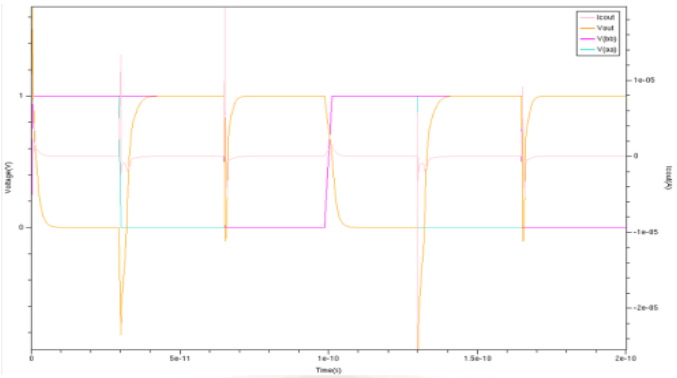

**Figure 7:** Simulated Transient input/output characteristics of 12nm Technology FinFet

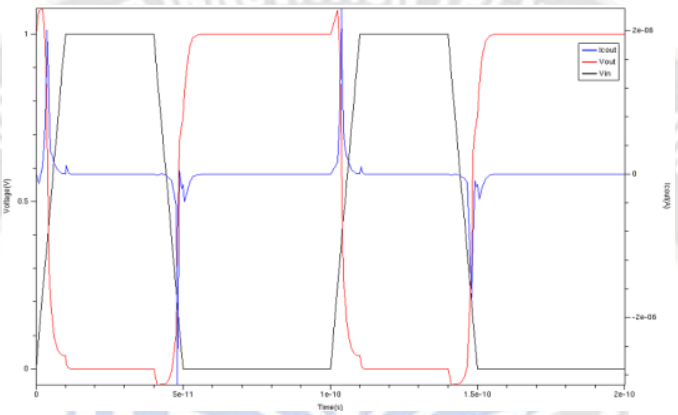

**Figure8:** Simulated Transient input/output characteristics of 7nm Technology

**Finfet.**

**Results and Discussion:**

**Table 2:** Comparative Experimental results in terms of power, delay and power delay product

| Parameters | **Power-Delay Analysis** | | |
|---|---|---|---|
| Technological Node | 14 nm | 12 nm | 7 nm |
| Power(nw) | 14.23 | 12.01 | 9.2 |
| Delay(ps) | 2.75 | 2.0 | 1.3 |
| PDP(aJ) | 0.039 | 0.024 | 0.011 |

The comparative experimental results presented in Table 2 reveal crucial performance metrics—power consumption, delay, and power delay product (PDP)—across various technological nodes, namely 14 nm, 12 nm, and 7 nm. As the technology node shrinks from 14 nm to 7 nm, there's a consistent trend of reductions in power consumption, propagation delay, and PDP, signifying the benefits of advancing to smaller nodes in terms of performance and energy efficiency. Furthermore, Figures 14, 15, and 16 illustrate the variation of leakage power, propagation delay, and PDP, respectively, as functions of technology node for FinFET circuit benchmarks. These visual representations corroborate the findings from the experimental results, showing improvements in leakage control, signal transmission efficiency, and energy efficiency with the transition to smaller technology nodes.

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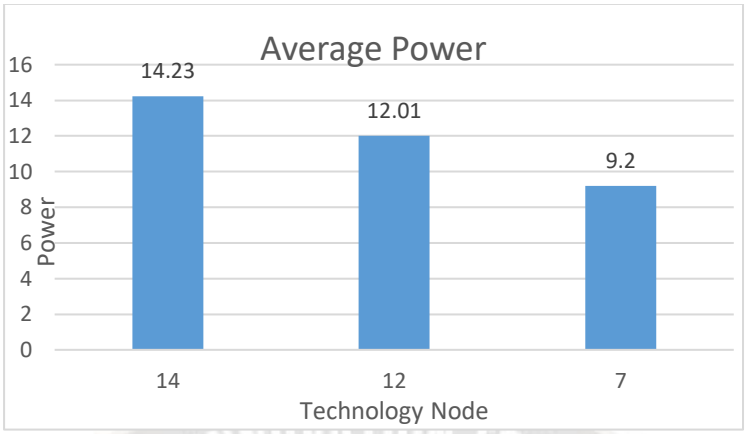


**Figure 11:** Variation of leakage power as a function of technology node for Finfet Circuit Benchmarks

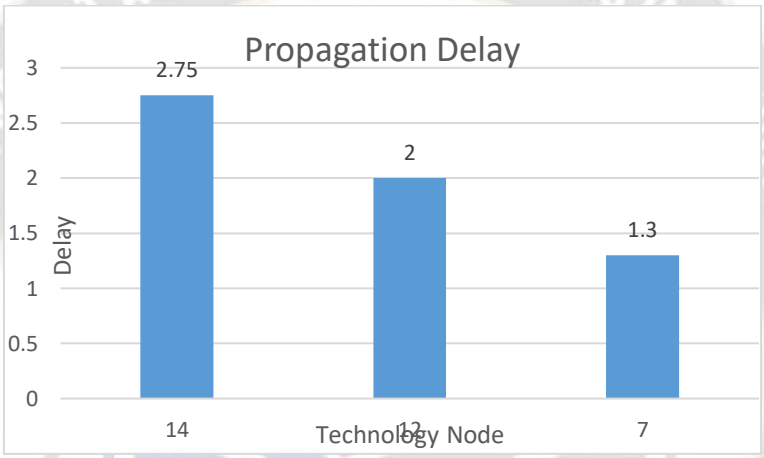


**Figure 12:** Variation of Propagation Delay as a function of technology node for FinfetCircuit Benchmarks

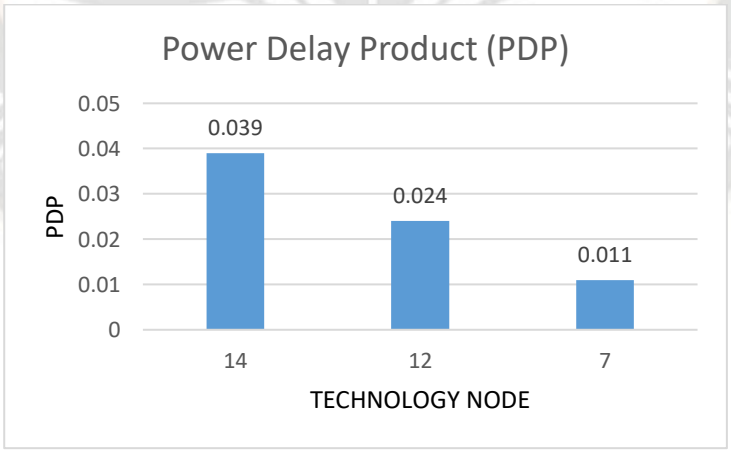


**Figure 13:** Variation of Power Delay Product as a function of technology node for Finfet Circuit Benchmarks

The schematic of the SRAM cell has been meticulously crafted and implemented using VHDL (VHSIC Hardware Description Language) in conjunction with Microwind. The simulation is conducted with a 1V power supply, providing the necessary energy for the system to operate and be thoroughly assessed.

A notable aspect of this analysis is the utilization of different foundry size CMOS technology, specifically at 90nm, 65nm, and 45nm. This deliberate choice allows for an exploration of how the SRAM cell behaves and performs under varying technological constraints. Each foundry size represents a

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different level of miniaturization, influencing the overall characteristics of the circuit.

During the simulation process, the voltage sources (VS1 and VS2) have been set at 0.5 volts. These voltage levels play a critical role in governing the behavior of the SRAM cell during different phases of operation. By adjusting these parameters, the simulation captures the response of the design under specific voltage conditions, enabling a nuanced understanding of its robustness and efficiency.

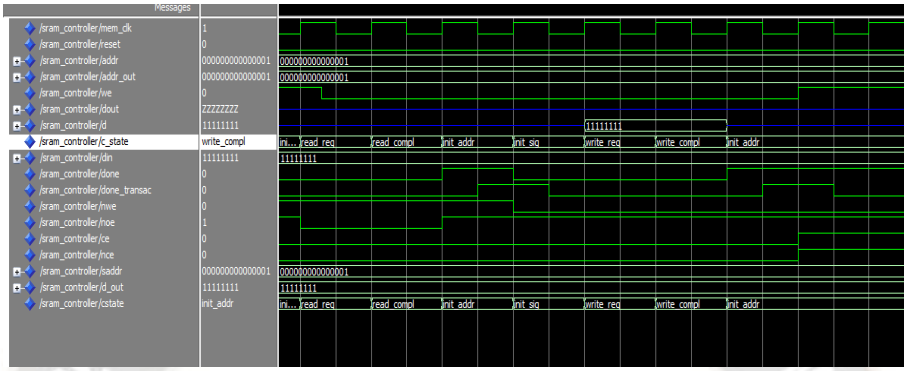


**Figure 9:** Read and Write operation using Micro-Wind

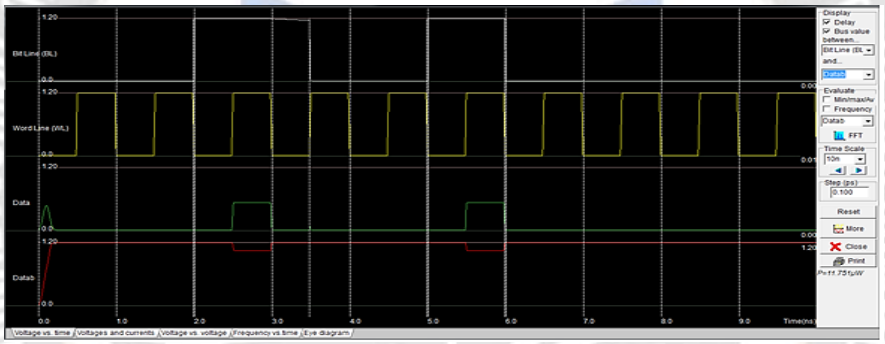


**Figure 10:** SRAM Memory Read and Write Cycle using Micro-Wind

## Conclusion

The research underscores the significance of the proposed SRAM system through meticulous analysis and simulation. By leveraging CMOS technology and sophisticated design methodologies, the study provides valuable insights into SRAM performance across various operational parameters. The investigation of structural parameters and design considerations at different technology nodes elucidates the progressive improvements in transistor characteristics and overall circuit performance. The comparative experimental results demonstrate the benefits of advancing to smaller technology nodes in terms of power consumption, propagation delay, and power delay product. Visual representations further reinforce these findings, showcasing improvements in leakage control, signal transmission efficiency, and energy efficiency with technology node shrinkage. Overall, the research contributes to a deeper understanding of SRAM design and optimization, laying the groundwork for enhanced memory system architectures in future computing applications.

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