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A Review on Codec's for Crosstalk Avoidance in VLSI Interconnects

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Abstract: This paper reviews different encoding and decoding techniques for reducing crosstalk noise, delay and power dissipation using Fibonacci codes. The increasing demand for SOCs lead to several issues like crosstalk, delay, data security, especially area and power consumption. This makes the researchers are tending to resolve all these issues. Here we are concentrating on the crosstalk avoidance in on-chip buses. There are several techniques for crosstalk avoidance that is mainly concentrated on eliminating capacitive crosstalk completely, but not inductance. But due to faster clock speeds, lengthy interconnects and smaller rise and fall times inductive crosstalk's became significant. This paper reviews all the schemes in order to have a better performance in avoiding inductive and capacitive crosstalk.

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I. INTRODUCTION

The abundant development in SOC (System-on-chip), NOC (Network-on-chip), CMP (Chip-level Multiprocessing) and LOC (Lab-on-chip) have resulted in various constraints for the researchers and developers. Some of them are coupling, crosstalk, delay, and speed and accuracy, occurrence of error, area and power consumption. In all these issues the coupling and crosstalk plays a predominant role. The crosstalk effect when adjacent wires simultaneously transition in same or in opposite directions. The delay of such a transition may be twice or more than that of a wire transitioning next to a steady signal, the cross-coupling capacitance is comparable to or exceeds the loading capacitance on the wire. This delay penalty is commonly referred to as the capacitive crosstalk. Figure 1 shows the types of coupled interconnects that leads to cross talk. The capacitive crosstalk delay strongly depends on the transition activities of the adjacent signals, hence the crosstalk type. Here crosstalk Type-4 and type-3 have the worst delay characteristics it is followed by type-2 and then type-1.

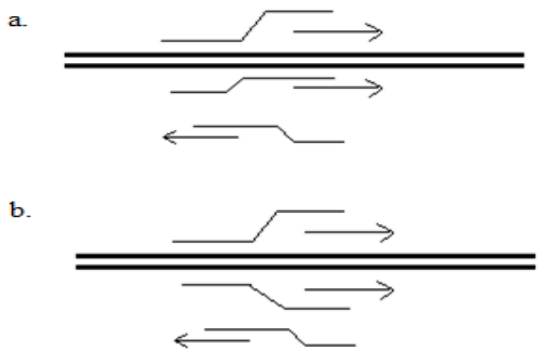

Figure: 1 Capacitive and Inductive coupled interconnects

The inductive crosstalk happens when the data transition happens in the same direction Thus various techniques are introduces in on-chip bus design to avoid these issues. To reduce or to avoid the crosstalk the data those are to be transmitted through ob-chip bus are initially encoded and the decoded at another end.

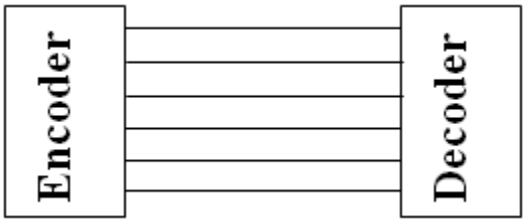

Figure: 1 Cross talk avoidance using CODEC

There are several methods and techniques used to avoid the crosstalk in this manner. In those there are two predominant techniques, forbidden pattern free (FPF) code and forbidden transitions free (FTF) different names have been used in the literatures for the second type of codes. This forbidden transitions free (FTF) code has the property that between any two adjacent wires in the bus, there will be no transition in opposite directions in the same clock cycle. Both FPF-CACs and FTF-CACs yield the same degree of delay reduction as passive shielding while requiring much less area overhead. Theoretically, the FPF-CAC has slightly better overhead performance that the FTFCAC. In practice, for large size bus, this difference is negligible. Both these codes are based on the Fibonacci code algorithms such as NFF4 (Normal Fibonacci Form), RF4 (Redundant Fibonacci Form) and CRF4 (Complement Redundant Fibonacci Form)

II. CROSSTALK REDUCTION TECHNIQUES

Aayushi sharma, Dhriti Duggal, "VLSI Interconnect Delay Crosstalk Models - A Review", in this paper the coupling capacitance and interconnects delay are the advantage of consuming less area overhead than shielding techniques.

Even though several different types of codes have been proposed in the past few years, no mapping scheme was given which facilitates the CODEC implementation. Compounded by the nonlinear nature of the CAC, the lack of a solution to the systematic construction of the CODEC has hampered the wide use of CAC in practice. In this paper, we give what we believe is the first solution to this problem [1].

M. Pavithra, Devireddy Venkatarami REDDY,"Implementation of C-Transform for Memory less Crosstalk Avoidance Applications", Crosstalk avoidance codes are shown to be able to reduce the inter-wire crosstalk and therefore boost the maximum speed on the data bus. It was showed that data can be coded to a forbidden pattern free vector in the Fibonacci numeral system. We first give a straightforward mapping algorithm that produces a set of FPF codes with near-optimal cardinality. The area overhead of this coding scheme is near the theoretical lower bound. The CODEC based on this coding scheme is systematic and has very low complexity. The size of the CODEC grows quadratic ally with the data bus size as opposed to exponentially in a brute forced implementation. Our systemic coding scheme allows the code design of arbitrarily [2].

Anchula Sathisha, Panyam Ranga Reddy Niharika, "A Theoretical analysis of Fibonacci coding techniques on On-chip Data Bus", In this work the Fibonacci numeral system is used to modify the data into a forbidden transitions free vectors. Uncomplicated mapping algorithms are given, that produces a set of NFF, RF and CRF codes with near-optimal cardinality. The average bus energy dissipation of un-coded and coded busses is compared by simulation. The crosstalk classes 4C and 3C are eliminated and experimental results show that the NFF, RF and CRF coding technique offers on average ~50% energy savings and average ~39% delay reduction (or bus speed improved) [3].

R. Prudhvi Raju K Hymavathi, N. M. M. K. PRASAD,"Crosstalk Codeword Generation for Forbidden Pattern Free Codec", The proposed strategy has been applied to a variety of encoding techniques. The properties an encoding technique must possess to be implementable using the proposed strategy are described in this paper. Three of the existing encoding techniques that fit the criteria were implemented using proposed strategy with encouraging outcomes. All three encoding techniques exhibit similar scalable trends in areas such as hardware overhead, power consumption, memory requirements and time complexity [5].

Yeow Meng Chee, Charles J. Colbourn,"Optimal low-power coding for error correction and crosstalk avoidance in on-chip data buses", In this paper, we present the first memoryless transition bus-encoding technique for power minimization, error-correcting and elimination of crosstalk simultaneously.We establish the connection between codes avoiding crosstalk of each type with packing sampling plans avoiding adjacent units. Optimal codes of each type are constructed [6].

Vikas Maheshwari, Anushree, "Crosstalk Noise Reduction Using Driver Sizing Optimization in VLSI RC Global Interconnects Using 90nm Process Technology", this paper presents a reduction and optimizations of crosstalk and driver sizing in much improved 2-π model using 90nm process technology parameters. In this paper we consider a step input signal for the excitation of aggressor line. Different sensitivity expressions are derived for the driver sizing and spacing. By considering the signs of sensitivity expressions, effect of driver sizing spacing (aggressor net and victim net) on crosstalk noise amplitude and width can be examined [6].

Savitha A.C., Siddesh.G.K, PhD, "Crosstalk Delay Avoidance in Long on Chip Buses by using Different Fibonacci Codec Techniques", The proposed encoder and decoder designs have the following features: Both the encoder and decoder have less arithmetic operations, Results in further complexity reduction in implementation. Bus partitioning becomes trivial and less overhead compared to the FPF-CAC CODECs. Both the encoder and decoder are constructed in a systematic Fashion. The encoder consists of multiple stages and a CODEC design for a larger bus can be extended from a CODEC of a smaller bus. This paper presents a memory less transition bus encoding technique for elimination of cross talk. An analytical study of the performance of Fibonacci code is also presented. The crosstalk effect is maximum only when adjacent wires are transitioning in opposite direction. Implementation of encoder and decoder, the overall delays on the bus are reduced for longer buses. Future work will include designing codes such that the coding circuitry can be implemented efficiently in the case of inductance where crosstalk occurs when adjacent lines transition in the same direction [7].

R.Sridevi,Dr.P.ChandraSekhar, Dr.B.K.Madhavi “Efficient Crosstalk Avoidance using Modfied Redundant Fibonacci code (MRFC) in VLSI Interconnect “has proposed a Modified Redundant Fibonacci code and designed encoder and decoder structures with the traction detector which usese this MRFC code for decoding the binary data and concentrates on avoiding inductive crosstalk which was not effectively reduced using existing Fibonacci codes for crosstalk avoidance .the delay incurred in interconnects was 5.018ns when compared to 20.653ns using existing techniques. [8]

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