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Hardware Implementation of SPWM Based Diode Clamped Multilevel Invertr

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***Abstract*:** This paper present three phase three level diode clamped multi level inverter. The control technique used here is sine pulse width modulation. The inverter can reduce the harmonic components compared with that of traditional full-bridge inverter under the condition of identical supply DC voltage and switching frequency. Here this paper presents a operational principles and switching functions are analyzed. The proposed inverter improves the dynamic performances Inverter is simulated using MATLAB/SIMULINK FFT analysis has been done. Proto type hardware is developed in laboratory and simulation results are compared with experimental results. Voltage to frequency control in open loop for three phase induction motor has also been done**.**

Keywords: *Diode-clamped multilevel inverter, sine pulse width modulation(SPWM), Total harmonic distortion.g(THD)*

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I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [1]. Subsequently, several multilevel converter topologies have been developed [2]. In 1981, diode-clamped multilevel inverter also called the Neutral-Point Clamped (NPC) inverter schemes were proposed .The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The multilevel starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM) used Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM) there are many techniques[3] [4], which are applied to multilevel inverter topologies. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents [5]. These features have made them favorable in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems. However, the reduction of harmonic components in output currents is still the main focus to reduce the influences of electromagnetic interferences or noise and vibrations. , a three-phase three-level PWM (Pulse Width Modulation) is presented in the paper. The main objective of paper is to design a three-phase three-level PWM (Pulse Width Modulation) inverter to reduce the harmonic components of the output voltage and the load current. The proposed inverter can reduce the harmonic components compared with that of traditional full-bridge PWM inverter In general, neutral point clamped PWM three-phase inverter which uses four switching elements in each arm has the five- level voltage waveforms that results in considerable suppression of the harmonic currents comparing with the conventional full-bridge type three-level PWM inverters.

II. DIODE CLAMPED MULTI LEVEL INVERTER

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [1]. A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two

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capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors, C1 and C2. The voltage stress across each switching device is limited to Vdc through the clamping diodes Dc1 and Dc2. It is assumed that the total dc link voltage is Vdc and mid point is regulated at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on. Figure 1 shows the circuit for a diode clamped inverter for a three-level. Switching states of the three level inverter are summarized in table I.

SWITCHING STATE TABLE-I

Switch status	State	Output voltage
Sa_1=on,Sa_2=on Sa_3=off,S_{a4}=off	Mode1	Vao=+Vdc/2
Sa_2=on,Sa_3=on Sa_1=off,S_{a4}=off	Mode2	Vao=0
Sa_3=on,S4=on Sa_1=off,Sa_2=off	Mode 3	Vao=-Vdc/2

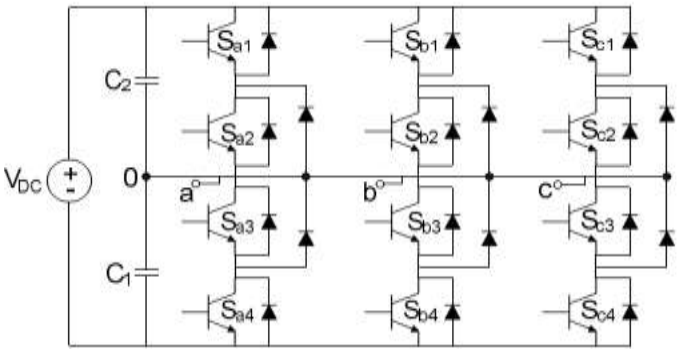

Figure 1 Topology of the diode-clamped three-level inverter

Fig 2 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage Vab consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a (2N-1)-level output line voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is Vdc/ (N-1). Although each active switching device is required to block only a voltage level of Vdc, the clamping diodes require different ratings for reverse voltage blocking.

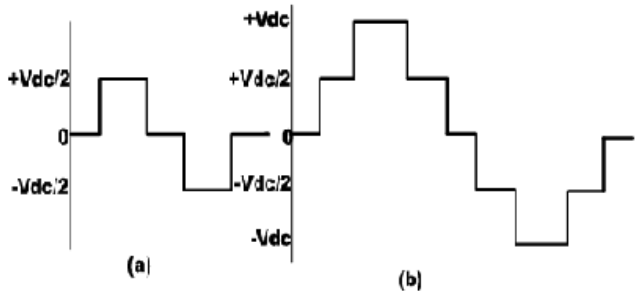

Figure 2: Output voltage in three-level diode- clamped inverter (a) Phase voltage (b) Line voltage

In general for an N level diode clamped inverter, for each leg 2(N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.

III. SIMULATION OF PROPOSED INVERTER

A three-phase full bridge inverter and the SPWM[7] [8]. modulator that has been designed to generate switching signals for three-phase full bridge inverter. In the designed three-level inverter, modulated SPWM [6] Signals have been used to control switches of the inverter, and THD analysis of output voltage and current have been performed as seen in figure 3,4,5.

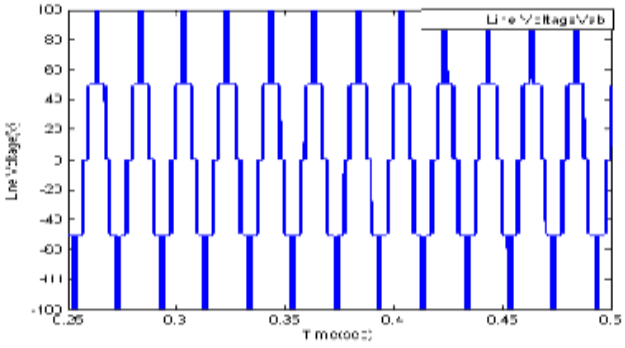

Figure 3: Line voltage wave form.

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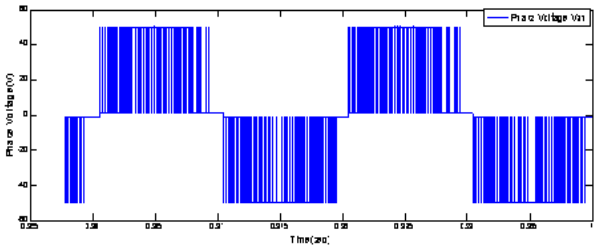

Figure 4: Phase voltage waveform.

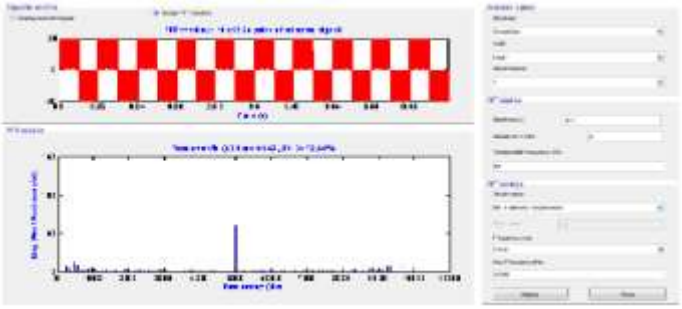

Figure 5: FFT analysis of SPWM based three phase three level inverter

IV. HARDWARE IMPLPMENTATION

In the laboratory a three-level diode clamed inverter prototype is being built. The primary purpose of the prototype is to verify the analytical and control algorithms that are developed here. The prototype built is flexible and robust enough to conduct the experiments.

Specifications of inverter

1. Voltage rating 200Vdc input.
2. Current rating 5 A.
3. Switching frequency 2KHz.
4. All the devices in the inverter are isolated and have separate driving circuits.

Inverter design which include building gate drive, building of power circuit. Microcontroller coding which include coding for sine pulse width modulation using STM-32 microcontroller. Hardware with complete lab setup shown below in Figure-6, 7, 8

Figure **6**: Image of gate drive and isolation circuit.

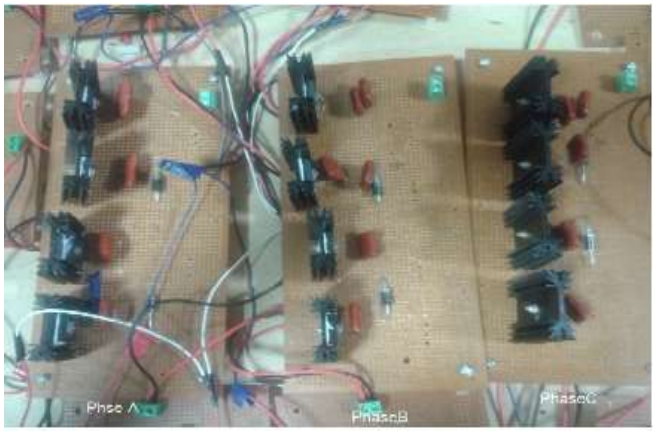

Figure **7**: power circuit of three level inverter

Figure **8**: complete setup.

When inverter is supplied with 100 V d.c. power source and three phase resistive load applied across it the phase and line voltage waveform are shown in figure 11&12 here. Two triangular waveform generated by microcontroller for comparison is shown in figure 9 and gate pulses for any one phase switches is shown in figure 10.

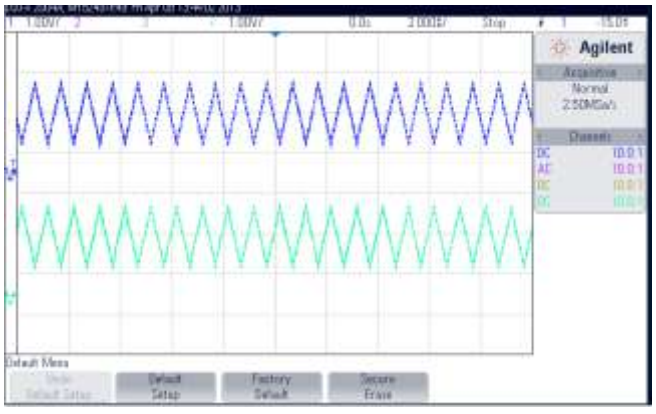

Figure 9: Triangular wave form generated by microcontroller for comparison

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Figure 10: Gate pulses four switches of phase A

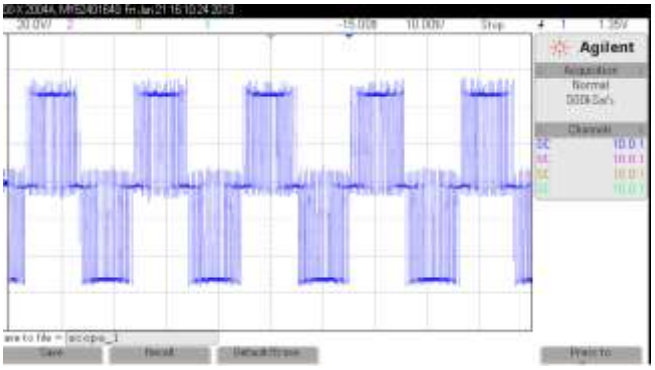

Figure 11: Phase voltage waveform

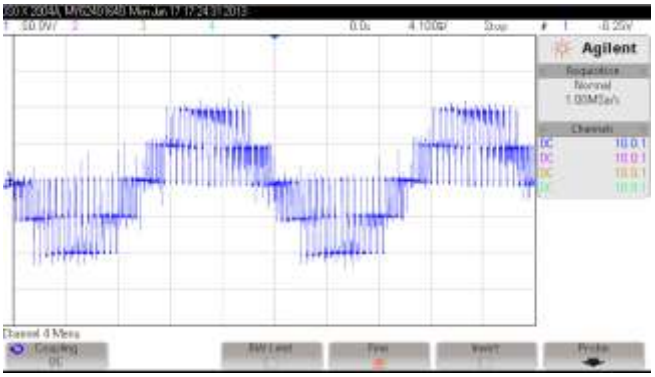

Figure **12**: Line voltage wave form.

V. FFT AND THD ANALYSIS

Table -2 gives the THD values of inverter voltage for different modulation indices with switching frequency of 2 KHz.

TABLE-II

MODULATION INDEX	RMS OUTPUT VOLTAGE	RMS F FUNDAMENTAL VOLTAGE	%THD
0.9	74.8	67.66	47.6
0.8	71.09	58.8	67.9
0.7	66.89	53.7	74.26
0.6	61.6	42.6	104.4

Figure 13 to 16 shows the FFT analysis of the inverter output voltage for different modulation indices. The graph shows all the components from 0 Hz to 32.29 KHz.

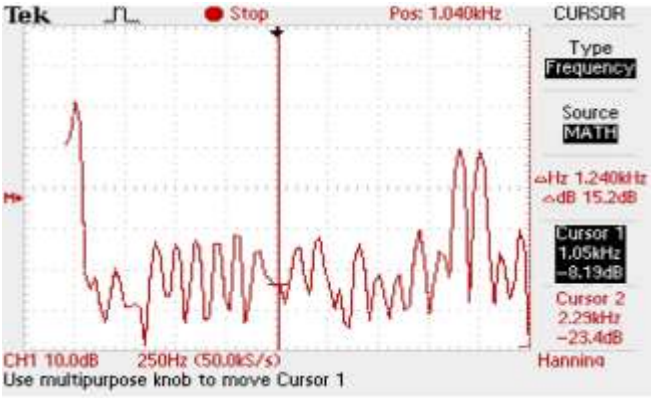

Figure13. FFT window for line to line voltage and 0.9 modulation index

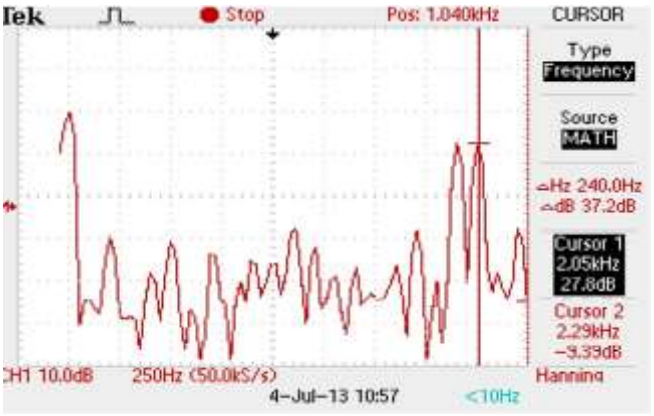

Figure14. FFT window for line to line voltage and 0.8 modulation index

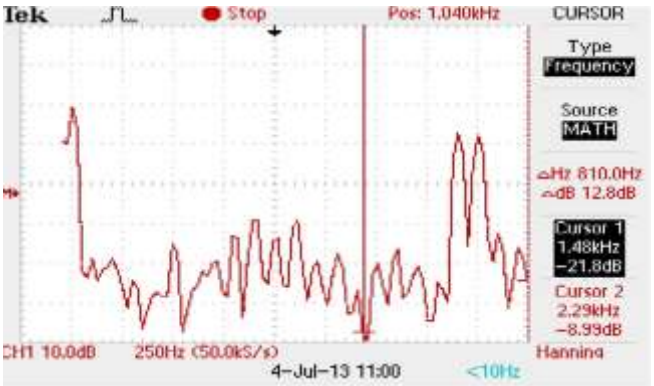

Figure15. FFT window for line to line voltage and 0.7 modulation index

Figure16 FFT window for line to line voltage and 0.6 modulation index

VI. RESULTS AND DISCUSSION

The simulation results for three-level diode clamped inverter is presented in this paper THD analyses for different modulation index and switching frequencies have been carried out. To verify the simulation results, three phase three level prototype hardware has been made in laboratory. Both simulation and experimental results are in close agreement It is seen in both simulation that by using that largest lower order harmonics shifted to switching frequency also value of fundamental voltage is significant.

VII. CONCLUSION

It is concluded from this analysis; SPWM and Three Level with Neutral Point Clamped Inverter are helpful techniques for harmonic reduction and to improve voltage or current. Profile without additional filters requirements. This multilevel inverter improves output voltage, reduces output total harmonic distortion and voltage stress on semiconductors switches, acoustic noise and Electro Magnetic Interference (EMI)also decreases and hence the schemes are confirmed by simulation and experimental.

The principle of the scheme for the three-level diode clamped converter could be extended in generalizing the technique to N level converter. The carrier-based PWM scheme proposed in the present work, developing a generalized logic, which can remove the shorting of the devices for any level of the inverter.

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