International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *25 July 2023* ***Revised:*** *14 September 2023* ***Accepted:*** *28 September 2023*

Novel DC Capacitor Voltage Balancing Strategy of Modular Multilevel Converter based STATCOM for Reactive Power Compensation and Voltage Improvement

Vadlamudi Naresh[1*], Dr. P. Balachandar[2]

[1*]Research Scholar, Department Of Electrical And Electronics Engineering, Faculty Of Engineering And Technology, Annamalai University, Annamalai - 608 002
[2]Assistant Professor, Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology, Annamalai University, Annamalai - 608 002

***Corresponding Author:** Vadlamudi Naresh
*Research Scholar, Department Of Electrical And Electronics Engineering, Faculty Of Engineering And Technology, Annamalai University, Annamalai - 608 002

Abstract: In recent years, the integration of renewable energy sources and their unpredictable nature has posed significant challenges to power grid stability and voltage regulation. To address these issues, the Modular Multilevel Converter (MMC) based Static Synchronous Compensator (Statcom) has emerged as a promising solution for reactive power compensation and voltage improvement. However, one critical concern in MMC-Statcom operation is the voltage balancing of DC capacitors, which directly affects system performance and efficiency. In this research, a novel DC capacitor voltage balancing strategy is proposed for MMC-Statcom to ensure optimal operation and enhanced performance. The proposed strategy employs advanced control algorithms and innovative switching techniques to maintain balanced DC capacitor voltages under varying operating conditions. By achieving balanced capacitor voltages, the MMC-Statcom can effectively compensate reactive power and regulate the grid voltage with improved efficiency and stability. The effectiveness of the proposed DC capacitor voltage balancing strategy is extensively evaluated through simulation studies and experimental validations. Comparative analyses are performed with existing voltage balancing methods, demonstrating superior performance and robustness of the novel strategy. The results showcase its potential for practical implementation in real-world power systems. Overall, this study presents a significant advancement in MMC-Statcom technology, providing an effective solution for reactive power compensation and voltage improvement while ensuring reliable and stable grid operation. The proposed novel DC capacitor voltage balancing strategy holds the promise of contributing to the enhancement of power system stability and facilitating the integration of renewable energy sources in modern electrical grids.

Keywords: DC capacitor voltage balancing, Modular Multilevel Converter, Statcom, Reactive power compensation, Voltage improvement, Power grid stability, Control algorithms, Switching techniques, Renewable energy integration, Power system stability.

I. Introduction

The prevalence of power electronic-driven loads like electric vehicles and electric traction is on the rise. Simultaneously, the power grid is experiencing a swift integration of renewable energy sources. Therefore, there is an increasing occurrence of reactive power, unbalanced load current, and harmonics. The utilization of the voltage-source-based static synchronous compensator (STATCOM) [1] proves to be highly beneficial in addressing power quality issues arising from the increased use of power electronic-driven loads and renewable energy sources. Specifically, it effectively mitigates problems caused by unbalanced loads. Over the past decade, significant progress has been made in the development of STATCOM, particularly by employing modular multilevel cascaded converters (MMCCs). These advancements have extended the scope of compensation applications to medium and high voltage power grids [2].

The MMCC-STATCOM offers the advantage of scalability, allowing for the generation of higher voltages without the need for step-up transformers. Additionally, it demonstrates excellent harmonic performance at lower switching frequencies, reducing the demand for extensive filtering. At the core of an MMCC-STATCOM are its sub-modules, with the single-phase three-level H-bridge converter being the predominant topology utilized [3]. In addition to the single-phase three-level H-bridge converter, there are other well-known topologies utilized, such as the five-level flying capacitor converter (5L-FC) [4] and the five-level neutral

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point clamped converter [5]. These alternative topologies have been extensively studied to assess their respective advantages concerning manufacturing cost, operational performance, and footprint [6]. An essential concern when employing MMCC-STATCOMs for power quality control is the preservation of module capacitor voltage balance. Due to the absence of shared dc-links, the capacitors within the cascaded modules remain isolated from one another. As a result, transferring power between levels within the sub-module stack [7] and between the phase arms [8] becomes challenging. The deviation of module capacitor voltages from their intended level can lead to operational disturbances or even damage to the device. This imbalance in voltage within the cluster can be mitigated within a single-phase arm by implementing closed-loop average capacitor voltage control and adjusting the PWM schemes. However, during the compensation of unbalanced loading in the utility grid, the module capacitor voltage imbalance may worsen.

The cause of the worsened module capacitor voltage imbalance in MMCC-STATCOMs during the compensation of unbalanced loads in the grid is attributed to the supply of negative sequence current to the grid. This supply of negative sequence current results in an active power imbalance between the phase arms of the STATCOM. To address this issue, countermeasures have been devised. For instance, in star-connected MMCC-STATCOMs, a solution involves introducing a sinusoidal zero sequence voltage at the neutral point, thereby shifting the neutral point to a non-zero voltage level [9]. Because of introducing the sinusoidal zero-sequence voltage at the neutral point, the disparities in phase power caused by negative sequence current flowing through the phase arms are eradicated.

This results in a balanced distribution of active power among the phases. Nevertheless, this approach poses challenges because the injected zero-sequence voltage can lead to the converter phase voltages surpassing their rated levels when faced with higher load imbalances. Consequently, the system might operate in over-modulation mode or even become uncontrollable. Efforts have been made to mitigate the issues caused by the injected zero-sequence voltage. One method involves introducing third-order harmonics, which can slightly reduce the peak value of the zero-sequence voltage. However, the effect of this approach is limited, with the peak phase-voltage reduction achieving only approximately 12%. Consequently, this provides an extended compensation range for the maximum load imbalance ratio, increasing it from around 58% to 65%, as demonstrated in [10]. An alternative suggestion to address the redistribution of phase active power in MMCC-STATCOM is by injecting negative sequence voltage onto the converter phase reference voltages [11].

However, this approach is primarily intended for dealing with grid voltage sag conditions. A technique was put forward for MMCC-STATCOM that involves the utilization of both negative-sequence current and zero-sequence voltage [12]. However, it is important to note that this technique is specifically designed for operation during power grid fault conditions and is not suitable for addressing load imbalance issues. The MPC technique is a renowned and extensively utilized method for controlling modular multilevel converters, predominantly in high-voltage direct current (HVDC) applications. This approach involves utilizing a discrete-time model of the MMCC circuit to anticipate the output phase current. Based on this prediction, it identifies the most favourable switching state that minimizes a specified cost function.

One of the main challenges associated with this technique is the real-time determination of the optimal switching state or vector from numerous candidates. Different schemes have been reported in the literature, falling into two categories: finite control set model predictive control (FCS-MPC) [13] and continuous control set model predictive control method (CCS-MPC) [14], also referred to as modulated model predictive control (MMPC). The former approach involves choosing a switching state from a finite set for the respective converter while employing a sorting algorithm to balance the capacitor voltages in the sub-modules during the next switching cycle. While this method has demonstrated excellent dynamic performance and has been applied to various power converters, it has some drawbacks. These drawbacks include variable switching frequency and suboptimal steady-state performance, as only one result can be generated per sampling period [15]. On the contrary, the CCS-MPC approach predicts continuous voltage control signals within a single sample period and subsequently converts them into switching vectors. This technique offers advantages such as reduced current ripples and lower computational requirements. Another variation within CCS-MPC is the optimal voltage level-based-MPC (OVL-MPC) [16]. OVL-MPC employs a cost function like the one used in [17] but evaluates the appropriate number of sub-modules to be inserted or bypassed in each phase arm based on the predicted voltages.

In [18] introduced a novel approach called combined grouping and sorting optimal MPC for MMC HVDC. In this method, the n sub-modules in each arm are divided into m groups. By applying optimized MPC at both the group level and the sub-module level, the computational burden is significantly reduced. Another variation is the dual-stage-based MPC [19], where the first stage aims to determine the optimal voltage level, while the second stage selects the switching states using a separate MPC approach without the need for a sorting algorithm. In MMC applications, the space vector modulation scheme is employed [20] to improve the steady-state performance while maintaining a fixed switching frequency. The determination of optimal times for the three active vectors (two active vectors and one zero vector) is crucial to minimize the cost function value. Additionally, various sine-triangle-based PWM techniques are utilized in [21] specifically for voltage source inverters (VSIs). These techniques offer comparable performance to the space-vector based modulation scheme while additionally reducing the computational burden. Among these methods, the phase-shift PWM (PS-PWM) stands out as the most popular due to its ability to effectively maintain SM voltage balance [22].

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Presently, within medium-voltage distribution systems, numerous power quality challenges arise due to unbalanced loads and nonlinear loads. These issues encompass low power factor, harmonic distortion, and unbalanced voltage. To enhance power quality, static synchronous compensators (STATCOMs) are extensively employed on the grid side to attain a high-power factor and reduce distortion. In recent times, multilevel converter-based STATCOMs have gained significant popularity in medium-voltage networks. These converters include flying-capacitor multilevel converters (FCMC), diode-clamped multilevel converters (DCMC), and cascaded H-bridge multilevel converters (CHMC) [23]. The FCMC and DCMC topologies have a DC bus, providing them with a more robust capability for negative-sequence current compensation compared to the CHMC with a star configuration. This attribute makes them particularly suitable for applications involving ac/dc power conversion. Nevertheless, their limited modularity and the substantial increase in capacitors and power diodes impose restrictions on their usage in medium/high-voltage networks. In contrast, the CHMC with a star configuration offers excellent modularity and is widely ideal for medium-voltage Var compensation applications [24]. In [25], a hierarchical voltage balancing control method is implemented using the phase-shifted unipolar sine PWM technique. This control structure is also utilized in [26] to address the low-voltage ride-through problem.

However, the CHMC with a star configuration exhibits a limited ability to compensate for negative-sequence currents. This limitation can be overcome by adopting the CHMC with a delta configuration [27]. Yet, this alternative introduces another issue as the voltage across the converter's arm becomes the line voltage, leading to a significant increase in the number of submodules (SM) within an arm. Since its implementation in the Transbay project in 2010, the modular multilevel converter (MMC) topology has garnered increasing interest in various applications. These applications span high-voltage direct current transmission systems, flexible alternating current transmission systems, and STATCOM [28]. The MMC topology shows great promise in effectively addressing various power quality issues. There has been extensive research on the structure and operating principles of MMC-STATCOM in the context of distorted and unbalanced grids. An MMC-STATCOM configuration designed for medium-voltage large-current systems and an extended configuration EMMC-STATCOM tailored for high-power applications are designed in [29]. In [30] introduced an MMC-based D-STATCOM system that effectively compensates for heavily unbalanced nonlinear loads while simultaneously regulating all the floating capacitor voltages. However, despite the numerous advantages of the MMC topology in Var compensation, the control of capacitor voltage balancing for all the floating SMs in each leg remains a challenging issue. This challenge is a common problem encountered in most multilevel converters [31]. Typically, achieving capacitor voltage balancing control requires a substantial number of voltage sensors and significantly increases the computational load in controllers. Consequently, this may lead to longer digital control cycles. As the converter voltage levels increase, this situation worsens.

In [32], a novel MMC topology is introduced, employing clamping diodes to regulate the capacitor voltages of a star-configured multilevel converter. This approach significantly simplifies the capacitor voltage balancing control and substantially reduces the number of required voltage sensors. However, it is worth noting that the negative-sequence current compensation capability is relatively weak, necessitating the use of an energy feedback circuit. A diode-clamped modular multilevel converter MMC is developed to address these limitations. Incorporated into each SM is a balancing branch comprising a low power rating diode and an inductor. The balancing branches play a vital role in clamping and naturally sorting the capacitor voltages from the bottom SM to the top SM within each arm. As a result, the clamping current pulse can be effectively controlled. By incorporating the balancing branches, the clamping current pulse can be effectively suppressed. Consequently, only the capacitor voltage of either the top or bottom SM needs to be measured within each arm. With a straightforward voltage control method, the capacitor voltage of the chosen SM can be regulated to the reference value, resulting in the balancing of all SM capacitor voltages in that arm. Despite the inclusion of clamping diodes and inductors in the MMC topology, the advantages of reduced voltage sensor costs and simplified capacitor voltage balancing control are significant. This paper provides a comprehensive discussion on the power circuit and control algorithm of the MMC-STATCOM.

II. MMC-STATCOM

A. MMC

The MMC offers various appealing configurations and finds applications across different domains. In scenarios with high voltages, the MMC removes the requirement for an isolated DC source and transformer. For achieving a voltage waveform of excellent quality, the submodules of the MMC are interconnected in a sequential setup, allowing the creation of the desired system voltage. The submodules comprise a combination of IGBTs, diodes, and capacitors and exhibit diverse shapes and structures. The calculation of the necessary number of submodules for an MMC design depends on distinct factors, such as the application's nature, the operating voltage, and the rating of the involved IGBTs.

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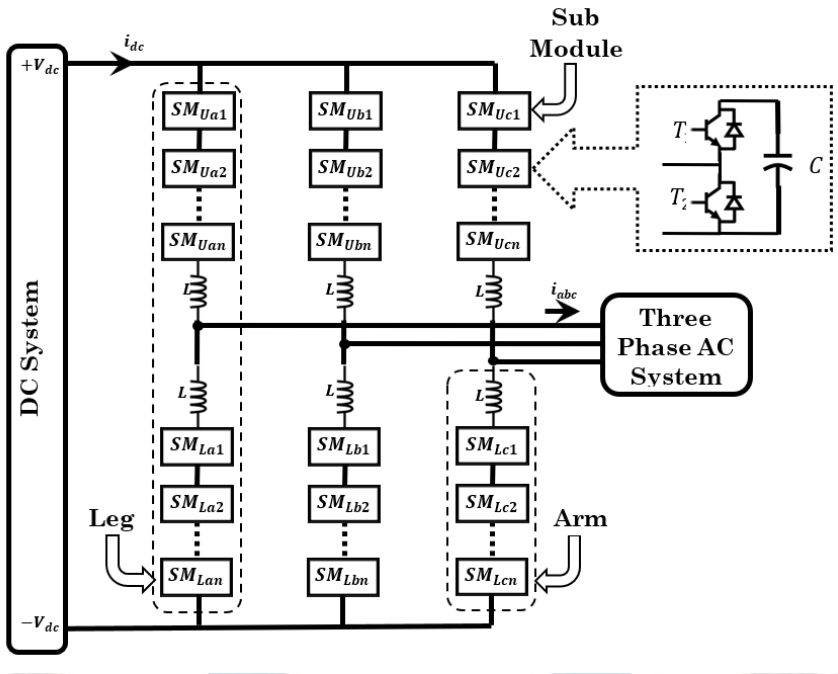

Fig 1. MMC

Figure 1 presents a three-phase MMC configuration used for converting DC to AC. In this setup, the positive and negative terminals of each MMC leg link to the DC link, while the centre point of each leg connects to a 3φ AC system. As a result, the midpoints serve as dividers, creating separate sections within each leg known as the positive arm and the negative arm. Each part of the MMC contains a current-limiting inductor and a series of connected submodules. An inductor is employed as a current-limiting element to avoid the rise of circulating current due to voltage discrepancies between the arms. The MMC design's modular nature offers flexibility in modifying voltage and power ratings by adding or removing submodules. It enables bidirectional conversion of DC voltage into stepped voltage. The MMC demonstrates a low dv/dt ratio, reduced total harmonic distortion (THD), and minimal current ripples. The use of series-connected submodules allows for low switching frequency control and supports fault-tolerant operation. A submodule (SM) is a fundamental circuit that utilizes low voltage switching devices to convert voltage in one direction to bidirectional voltage. It can be powered by a capacitor, enabling the application of unidirectional or DC voltage. The MMC incorporates several types of submodules, including Half-bridge (HB), Full-bridge (FB), flying capacitor (FC), Cascaded half-bridge (CH), and Double clamp (CD) submodules. Figure 2 shows a Half-bridge (HB) submodule composed of a storage element, two switches, and two diodes. The submodule utilizes the complementary action of the two IGBT switches T_1 *and* T_2,, which alternate between on and off states to regulate the voltage of the DC capacitor, v_c. When one switch is on, the other switch is off, and vice versa.

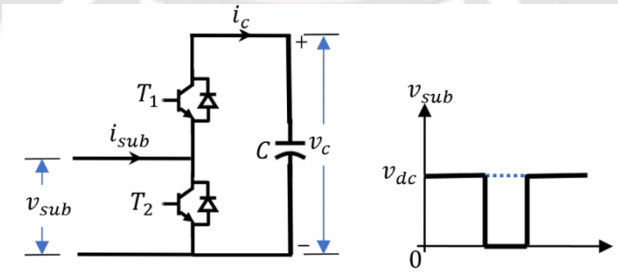

Fig 2 Switching states of MMC.

Equation (3-4) shows the relationship between the DC capacitor voltage (v_c) and the current flowing through it.

$$u_c = \frac{1}{C}\int_0^t i_C(\tau)d\tau \#$$

$$i_C(\tau) = T_1 i_{sub} \#$$

When the T_1switch is turned on, the capacitor current (i_c) aligns with the submodule current (i_{sub}). Conversely, when the switch is turned off, the capacitor current becomes zero. Figure 2 shows two potential energy points at the AC side, labelled as u_{dc} and 0. When the T_1switch is turned on, the

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AC side voltage of the submodule (v_{sub}) equals the capacitor voltage (u_c). The capacitor voltage increases as the capacitor current (i_c) flows in the positive direction, and it decreases when(i_c) flows in the negative direction. On the other hand, when T_1 is turned off, the AC side voltage (v_{sub}) becomes zero, while the capacitor voltage (u_c) remains constant. The various switch states of the half-bridge submodule are concisely presented in Table 1.

Table 1. Transitioning between operational states of the half-bridge switching module

Changing State S	T_1	T_2	v_{sub}	$i_{sub} > 0$	$i_{sub} < 0$
1	ON	OFF	v_c	v_c increases	v_c decreases
0	OFF	ON	0	v_c constant	v_c constant

Through the implementation of series-connected submodules, the MMC can efficiently convert a constant DC voltage into a multilevel stepped voltage waveform, capable of being bidirectional. The number of interconnected submodules within each arm of the system determines the extent of multiple stages achievable in the waveform. Throughout the MMC configuration, these submodules are constructed uniformly. When 'n_{sm}' submodules are connected in each leg with a rated DC side voltage of u_c, the output voltage from the submodules can be denoted as v_{sub1}, v_{sub2}, v_{sub3}…, v_{subn}. With 'n_{sm}' submodules, '$n_{sm}+1$' voltage levels can be achieved, namely 0, u_c, $2u_c$, $3u_c$,…,, nu_c. A voltage level of 0 can be attained by deactivating all submodule switches. By using different combinations of submodule switching states, various voltage levels can be generated. The switch states govern the control and regulation of the capacitor voltage in each submodule. Moreover, the output voltage of each arm in the MMC, represented as v_{arm}, results from the summation of voltages across all the submodules, as shown in equation (5).

$$v_{arm} = v_{sub1} + v_{sub2} + v_{sub3} \ldots + v_{subn_{sm}} = S_1 u_{c1} + S_2 u_{c2} + S_3 u_{c3} + \cdots S_n u_{cn_{sm}}$$

$S_1, S_2, S_3, \ldots, S_{n_{sm}}$ indicate the switching states of the submodules, represented by binary values of 1 or 0.

A. Capacitor Voltage Clamping Principle of MMC-STATCOM

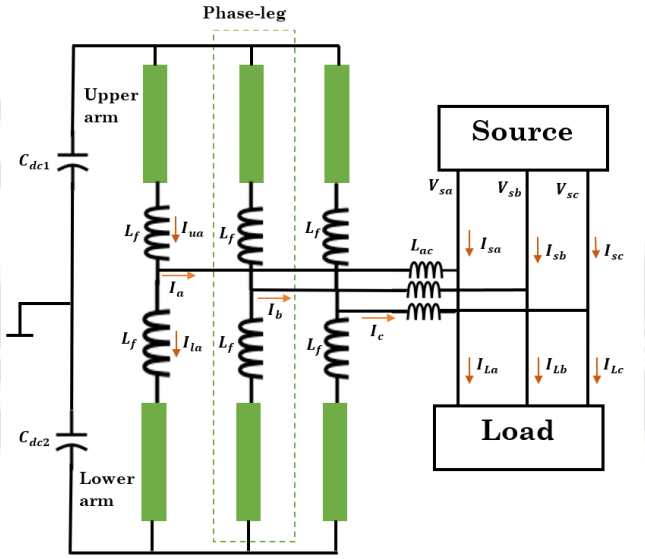

Fig 3. MMC based STATCOM.

Drawing from the conventional MMC (Modular Multilevel Converter) setup, Fig. 3 illustrates the structure of the STATCOM configuration. The voltage sources on the grid side are represented as V_{SJ} (j = a, b, c). The presence of unbalanced and nonlinear loads, such as the single-phase AC traction system, gives rise to power quality problems that the STATCOM aims to address. On the converter side, each phase leg is composed of an upper arm, a lower arm, and two arm inductors. Bulk capacitors are connected to the DC link. The STATCOM establishes a connection to the grid via the AC inductors L_{ac}. A typical SM comprises a DC energy storage capacitor along with two power switches, such as IGBTs. The topology suggested in [33] employs clamping diodes to arrange the SM capacitor voltages within one phase arm. These diodes demonstrate effective performance in the balancing process of the capacitor voltages. Under normal operating conditions, the converter functions smoothly in steady state. However, in abnormal conditions, a potential issue arises when a high-voltage deviation exists between two

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adjacent SM capacitors. As an instance, during the converter's startup process, high pulses of current flow through the clamping diode, posing a risk of damaging the switches. Moreover, the clamping diodes should have a sufficiently high current rating to recover from severe unbalance conditions. To mitigate the current pulses, a buffer inductor is connected in series with the clamping diode. This converter, based on the basic structure of the MMC, is referred to as the diode clamped MMC.

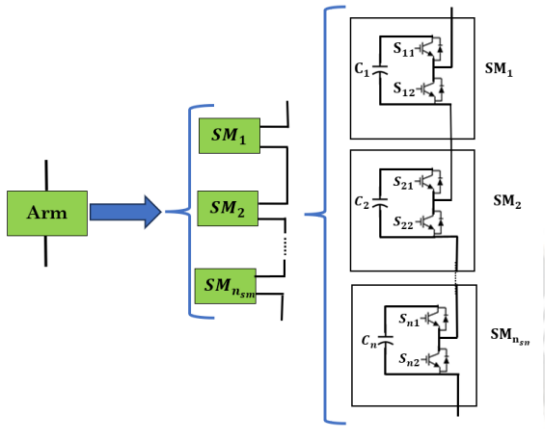

Fig 4. Arm of the MMC based STATCOM

For the sake of simplicity, all devices within the MMC are considered ideal. The paper employs the phase-shifted carrier pulse width modulation (PSC-PWM) method. In adherence to the principles of PSC-PWM, a phase shift θ exists between each pair of neighbouring triangle carrier waves. Due to the significantly higher frequency of the carriers compared to the reference signal and the presence of the arm inductor L_f, the arm current can be approximated as constant within a single switching cycle. As a result, the two adjacent SMs absorb or release nearly equal amounts of energy through the converter's arm current. Consequently, it is reasonable to assume that the capacitor voltage difference between these neighbouring SMs remains unaffected by the arm current.

By neglecting the energy absorbed or released through the main power circuit during each switching period, a closed loop is formed among capacitor $C_i, C_{i+1}, S_i, S_{(i+1)2}$ and the balancing branch when switch $S_{(i+1)2}$ is in the ON state. When the capacitor voltages $u_{c(i+1)}$ is greater than u_{ci}, a current i_{Di} emerges and flows from $C_{i+1}\ to\ C_i$, . Conversely, when $u_{c(i+1)}$ is less than or equal to u_{ci}, no current is present in the balancing branch, and the clamping diode remains off. When $S_{(i+1)2}$ is in the OFF state, the circuit loop is open, resulting in no energy exchange between the two capacitors. Based on the equivalent circuit of the balancing loop, we can derive the following equation:

$$\{C_e = \frac{C_i}{2} = \frac{C_{i+1}}{2}\ u_e = u_{c(i+1)} - u_{ci}$$

The circuit involves an equivalent capacitor, denoted as C_e, across which the voltage is u_e. It is evident that the circuit represents a second-order circuit, and the corresponding linear differential equation can be derived as follows:

$$L_i C_e \frac{d^2 u_e}{dt} + u_e = 0$$

Assume that $p1$ and $p2$ are the eigenvalues of the above differential equation, then.

$$\{p_1 = j\omega_0 = j\frac{1}{\sqrt{L_i C_e}}\ p_2 = -j\omega_0 = -j\frac{1}{\sqrt{L_i C_e}}$$

When $switch\ S_{(i+1)2}$turns on, if the initial voltage of C_e is u_0, we can derive the expressions for ue and the diode current i_{Di} as follows:

$$\{i_{Di} = \frac{U_0}{L_i(p_2 - p_1)}(e^{p1t} - e^{p2t})\ u_e = \frac{U_0}{p_2 - p_1}(p_2 e^{p1t} - p_1 e^{p2t})$$

II Control System

Fig. 5-7 illustrates the control block diagram of MMC-STATCOM.

A. Capacitor Voltage Balancing Control

In Fig. 5, the reference signal of the lower arm is phase-shifted by 180° compared to that of the upper arm. Let's assume the DC component of the PWM duty cycle as D_{dc}. The relationship between the upper arm capacitor voltages u_{jui}, lower arm capacitor voltages u_{jli}, and the DC bus voltage u_{dc} can be derived as follows:

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$$\sum_{i=1}^{n_{sm}} u_{jui} \times D_{dc} + \sum_{i=1}^{n_{sm}} u_{jli} \times D_{dc} = U_{dc}$$

If D_{dc} is 0.5, then

$$\sum_{i=1}^{n_{sm}} u_{jui} + \sum_{i=1}^{n_{sm}} u_{jli} = 2U_{dc}$$

This converter only necessitates n_{sm} voltage sensors, strategically placed in the top SMs within each of the n_{sm} arms. The control of u_{jui}, u_{jli} can be effectively regulated to approximate the reference value U_{dcref}/n_{sm}

$$u_{jui} = u_{jli} = U_{dcref}/n_{sm}$$

Where $j = a, b, c$ and $i = 1,2, \ldots, n_{sm}$

Fig. 7, illustrates the implementation of the pulse width adjustment method used to control the capacitor voltage in each arm. The capacitor voltage is influenced by the active power entering an SM, allowing for voltage regulation through power adjustment. To achieve capacitor voltage control, PI regulators are utilized. The sign function for arm current can be expressed as follows:

$$sign = \{1 \; arm\; current > 0 \quad -1 \; arm\; current < 0$$

In Case 1 (when arm current > 0), the voltage PI controller's output, V_{uai}^{ref}, is combined with the current controller's output, and the resulting value is sent to the PSC-PWM unit. When the capacitor voltage less than in u_{dcref}, V_{uai}^{ref} is positive, leading to an increase in the duty cycle of SM. Consequently, SM absorbs more active power from the arm current, causing capacitor voltage to rise. Conversely, when capacitor voltage is greater than u_{dcref}, V_{uai}^{ref} becomes negative, resulting in a reduction of the duty cycle of SM. This, in turn, causes SM to absorb less active power from the arm current, leading to a drop in capacitor voltage.

In Case 2 (when arm current < 0), the output of the voltage PI controller, V_{uai}^{ref}, is subtracted from the output of the current controller. When the capacitor voltage is less than u_{dcref}, V_{uai}^{ref} is positive, causing a reduction in the duty cycle of SM. Consequently, SM1 emits less active power to the arm current, leading to an increase in capacitor voltage. On the other hand, when capacitor voltage is greater than u_{dcref}, V_{uai}^{ref} becomes negative, resulting in an increase in the duty cycle of SM. As a result, SM1 emits more active power to the arm current, causing capacitor voltage to decrease.

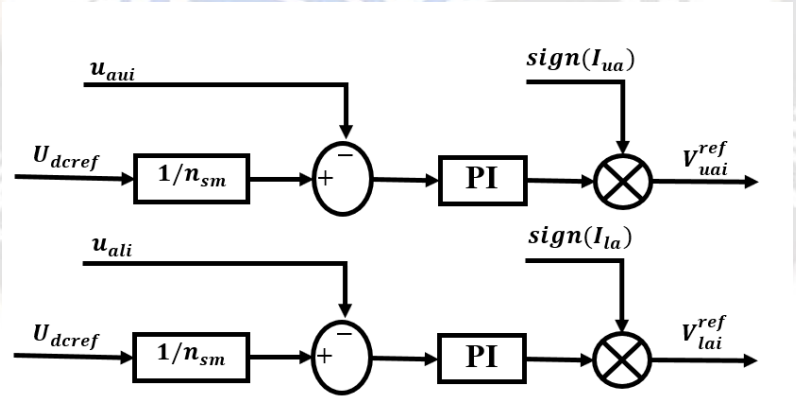

Fig 5. Capacitor Voltage Balancing Control of Phase A where $i = 1 \; to \; n_{sm}$

The objective of PWM duty cycle adjustment is to control SM to either absorb more power or emit less power when $u_{aui} < U_{dcref}$ or $u_{ali} < U_{dcref}$, and absorb less power or emit more power when $u_{aui} > U_{dcref}$ or $u_{ali} > U_{dcref}$. The voltage balancing controllers produce two outputs, V_{uj} and V_{lj} (j = a, b, c), corresponding to the upper and lower arms in the three phases.

B. Power Control in Positive Sequence

In Fig. 6, the system incorporates a phase-locked loop (PLL) module to estimate the phase angle (θ) of the grid voltage. This estimation is essential for coordinate transformation. The output current of the STATCOM is then transformed into the dq coordinates. Subsequently, two feedback control loops are employed—one for the DC bus voltage control and the other for reactive power compensation control. The dc bus voltage is regulated in accordance with U_{dcref}, and to estimate the active power required by the STATCOM, a PI controller is utilized. Additionally, the reactive current controller facilitates V_{ar} compensation. The active and reactive components of the output current in the positive sequence can be derived as follows:

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$$[I_d^+ \; I_q^+] = \frac{2}{3}\left[sin\theta \; sin\left(\theta - \frac{2}{3}\pi\right) \; sin\left(\theta + \frac{2}{3}\pi\right) \; cos\theta \; cos\left(\theta - \frac{2}{3}\pi\right) \; cos\left(\theta + \frac{2}{3}\pi\right)\right] [I_a \; I_b \; I_c]$$

Similarly, the reference reactive current is calculated from the load current as

$$[I_{Ld}^+ \; I_{Lq}^+] = \frac{2}{3}\left[sin\theta \; sin\left(\theta - \frac{2}{3}\pi\right) \; sin\left(\theta + \frac{2}{3}\pi\right) \; cos\theta \; cos\left(\theta - \frac{2}{3}\pi\right) \; cos\left(\theta + \frac{2}{3}\pi\right)\right] [I_{La} \; I_{Lb} \; I_{Lc}]$$

$$[V_{sd}^+ \; V_{sq}^+] = \frac{2}{3}\left[sin\theta \; sin\left(\theta - \frac{2}{3}\pi\right) \; sin\left(\theta + \frac{2}{3}\pi\right) \; cos\theta \; cos\left(\theta - \frac{2}{3}\pi\right) \; cos\left(\theta + \frac{2}{3}\pi\right)\right] [V_{sa} \; V_{sb} \; V_{sc}]$$

Here, I_{Ld}^+ and I_{Lq}^+represent the active and reactive components of the load current I_{lj} (j = a, b, c) in the positive sequence, respectively. Similarly, V_{sd}^+ and V_{sq}^+ denote the active and reactive components of the grid voltage V_{sj}(j = a, b, c), respectively. These components are introduced as feedforward components to enhance the dynamic response of the current control. The achievement of voltage regulation and Var compensation is derived as follows:

$$[V_{pa} \; V_{pb} \; V_{pc}] = \left[sin\theta \; cos\theta \; sin\left(\theta - \frac{2}{3}\pi\right) \; cos\left(\theta - \frac{2}{3}\pi\right) \; sin\left(\theta + \frac{2}{3}\pi\right) \; cos\left(\theta + \frac{2}{3}\pi\right)\right] [V_d^+ \; V_q^+]$$

The quantities V_d^+ and V_q^+ are obtained by summing the output of the current controller and the feedforward component of the grid voltage, as depicted in Fig. 6

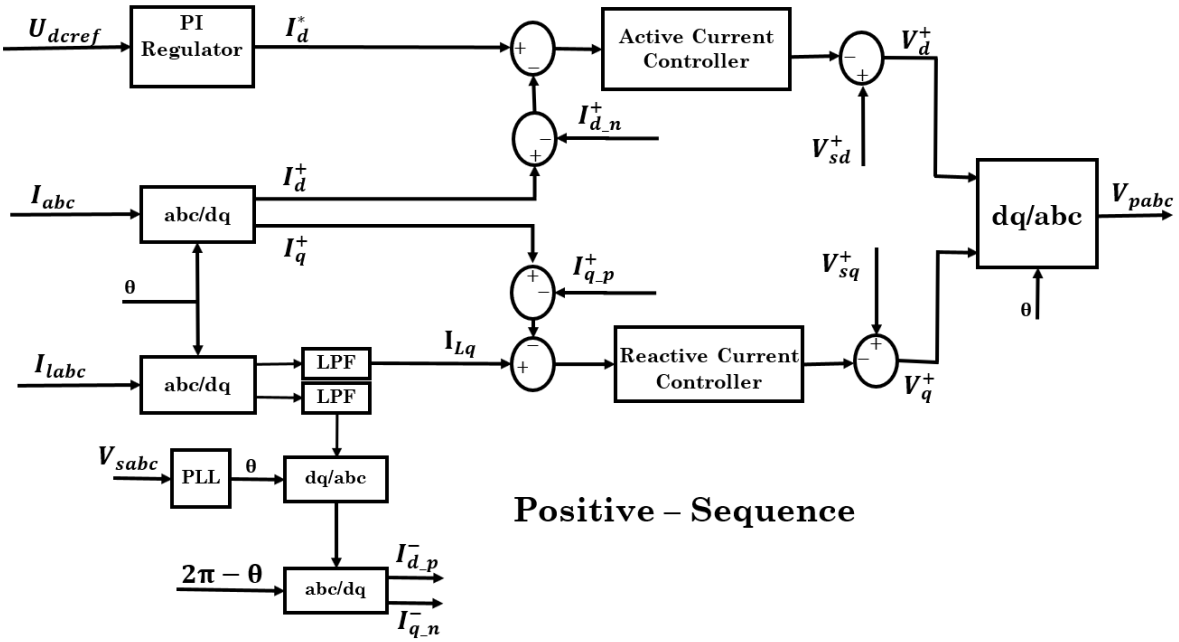

Fig 6. Power Control in Positive sequence

C. Power Control in Negative Sequence

In Fig. 7, like the positive-sequence components of the load current, the active and reactive components with negative-sequence can also be obtained with the coordinate transformation. However, the conversion result includes both a dc component and an ac component with a double line-frequency. The dc components, I_{Ld} and I_{Lq}, are extracted separately through two low-pass filters. The phase angle employed in the negative-sequence coordinate transformation is:

$$\theta_{mod} = 2\pi - \theta$$

The output of negative-sequence compensation can also be achieved as follows:

$$[V_{na} \; V_{nb} \; V_{nc}] = \left[sin\theta_{mod} \; cos\theta_{mod} \; sin\left(\theta_{mod} - \frac{2}{3}\pi\right) \; cos\left(\theta_{mod} - \frac{2}{3}\pi\right) \; sin\left(\theta_{mod} + \frac{2}{3}\pi\right) \; cos\left(\theta_{mod} + \frac{2}{3}\pi\right)\right] [u_d^- \; u_q^-]$$

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ISSN: 2321-8169 Volume: 11 Issue: 10
***Article Received:** 25 July 2023 **Revised:** 14 September 2023 **Accepted:** 28 September 2023*

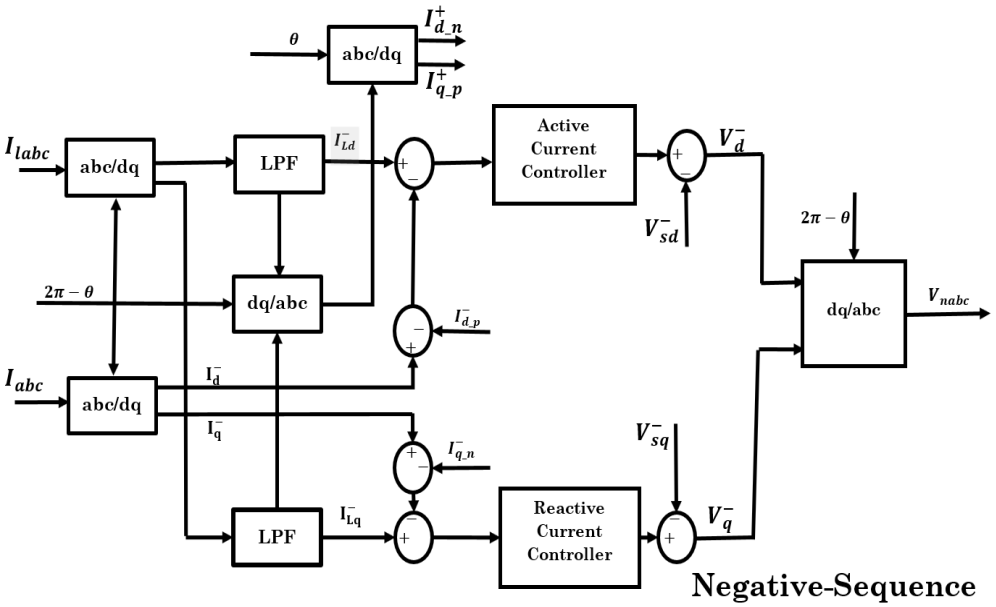

Fig 7. Power Control in Negative Sequence

D. Switching Modulation

In Fig. 8, the PSC-PWM method is utilized to generate the switching signals. The reference phase difference between the upper arm and the lower arm is π, without considering the output of voltage balancing controllers. The resulting modulation waves for all six arms are derived as follows, where $j = a, b, c \; and \; i = 1,2, \ldots, n_{sm}$:

$$[S_{uji}\; S_{lji}\;] = [V_{pj} - V_{pj}\;] + [V_{nj} - V_{nj}\;] + [V^{ref}_{uji}\; V^{ref}_{lji}\;]$$

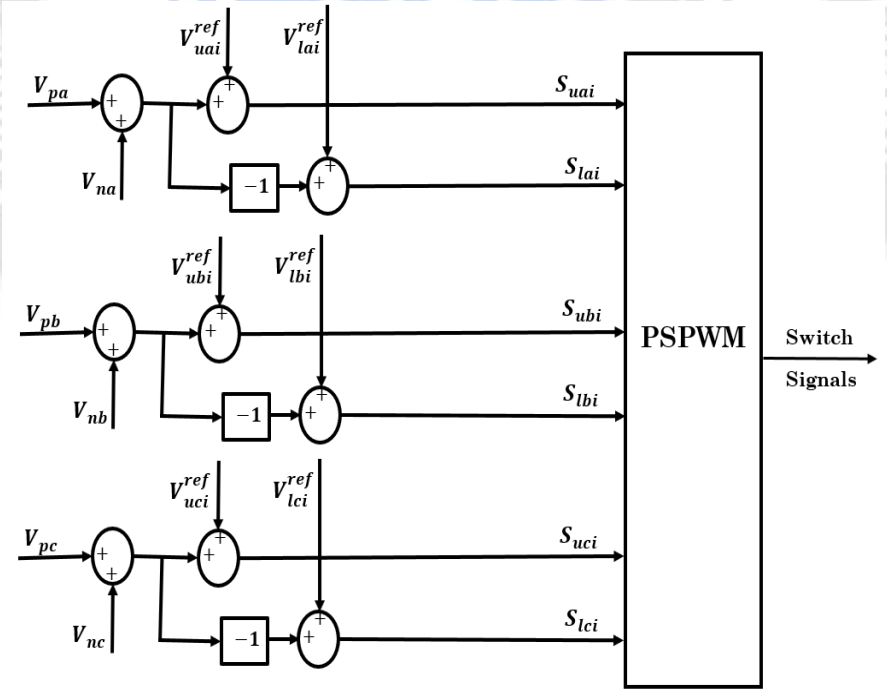

Fig 8. Pulse Width Modulation

IV. Simulation Results

In this study, the performance of MMC-based STATCOM (Static Synchronous Compensator) was thoroughly analysed through simulation using MATLAB-Simulink software. The simulation setup incorporated different types of loads. Balanced load, unbalanced load and nonlinear load comprising a three-phase diode bridge rectifier with R-L load are considered individually to check the performance of

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proposed MMC STATCOM. The solver step size employed in the simulation was 1e-6s, ensuring accurate and detailed capturing of system dynamics. To comprehensively evaluate the performance of the MMC-based STATCOM, dynamic conditions were imposed on the system. The simulation utilized specific system parameters as listed in Table 1, which were carefully chosen to represent real-world scenarios and ensure the validity of the results. The proposed MMC-based STATCOM was then assessed in a 6KV network, simulating a practical power distribution system.

Table 1. System Parameters

Grid voltage and frequency	**6 kV, 50 Hz**
Line resistance and inductance	**0.1 ohm and 0.2 mH**
Filter Inductor for STATCOM	**10mH**
Sub Module Capacitor	**4700 µF**
Arm Inductor	**5 mH**
No. of Sub Modules per arm	**10**
Clamping Inductor	**100 µH**
Switching Frequency	**2 kHz**
DC Link Voltage	**10 kV**

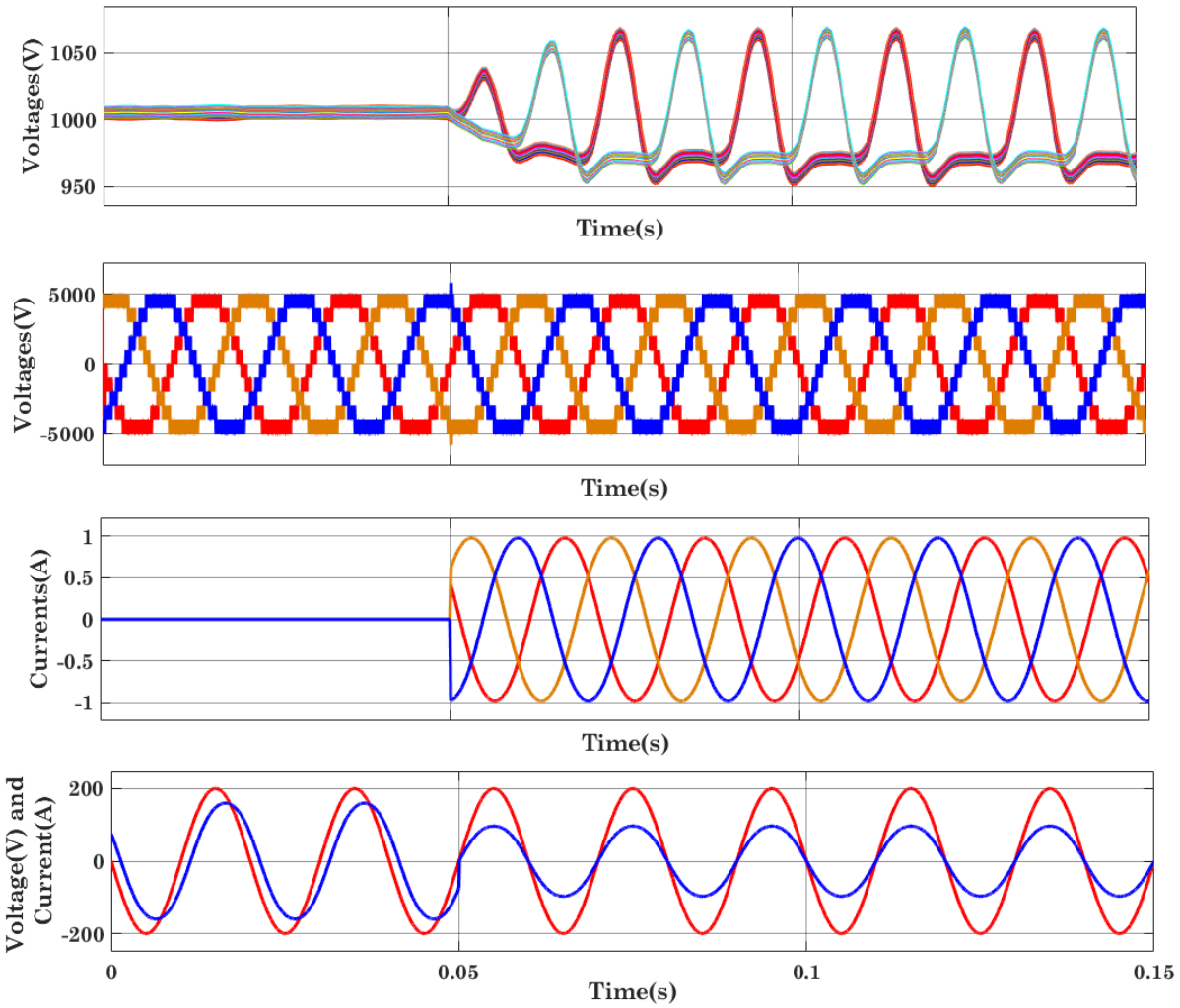

Fig 9. DC capacitor voltages of sub modules, STATCOM voltage, STATCOM currents and source voltage and current for balanced load

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
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Case 1. Balanced Linear Load

In this study, the performance of the MMC STATCOM was evaluated by connecting a balanced RL load to the power source, with the STATCOM being linked to the network at the Point of Common Coupling (PCC). At 0.05 seconds, the STATCOM was activated for positive sequence and negative reactive power compensation. A 10kV DC link voltage was utilized as the reference voltage for the DC side. Before 0.05 seconds, the STATCOM operated with a primary focus on DC voltage regulation. Consequently, the DC voltages across the capacitors of the sub-modules remained almost constant at 1kV, as illustrated in Figure 9a. After 0.05 seconds, the reactive power compensation was activated, resulting in a reduction in the phase difference between the source voltage and the source current. This reduction indicates the achievement of unity power factor operation, as depicted in Figure 9d. The MMC STATCOM was then able to provide the required reactive power to meet the demands of the RL load. Figures 9b and 9c illustrate the voltage and current profiles of the MMC STATCOM, respectively, during its operation. The results indicate the effectiveness of the STATCOM in regulating voltage, compensating for reactive power, and achieving unity power factor operation, which are crucial factors for enhancing power quality and system stability. By demonstrating these outcomes, the study highlights the proficient performance of the MMC STATCOM in dynamically responding to load variations and maintaining a balanced and efficient power flow in the network. This evaluation provides valuable insights into the practical applicability and benefits of using the MMC STATCOM in real-world power systems.

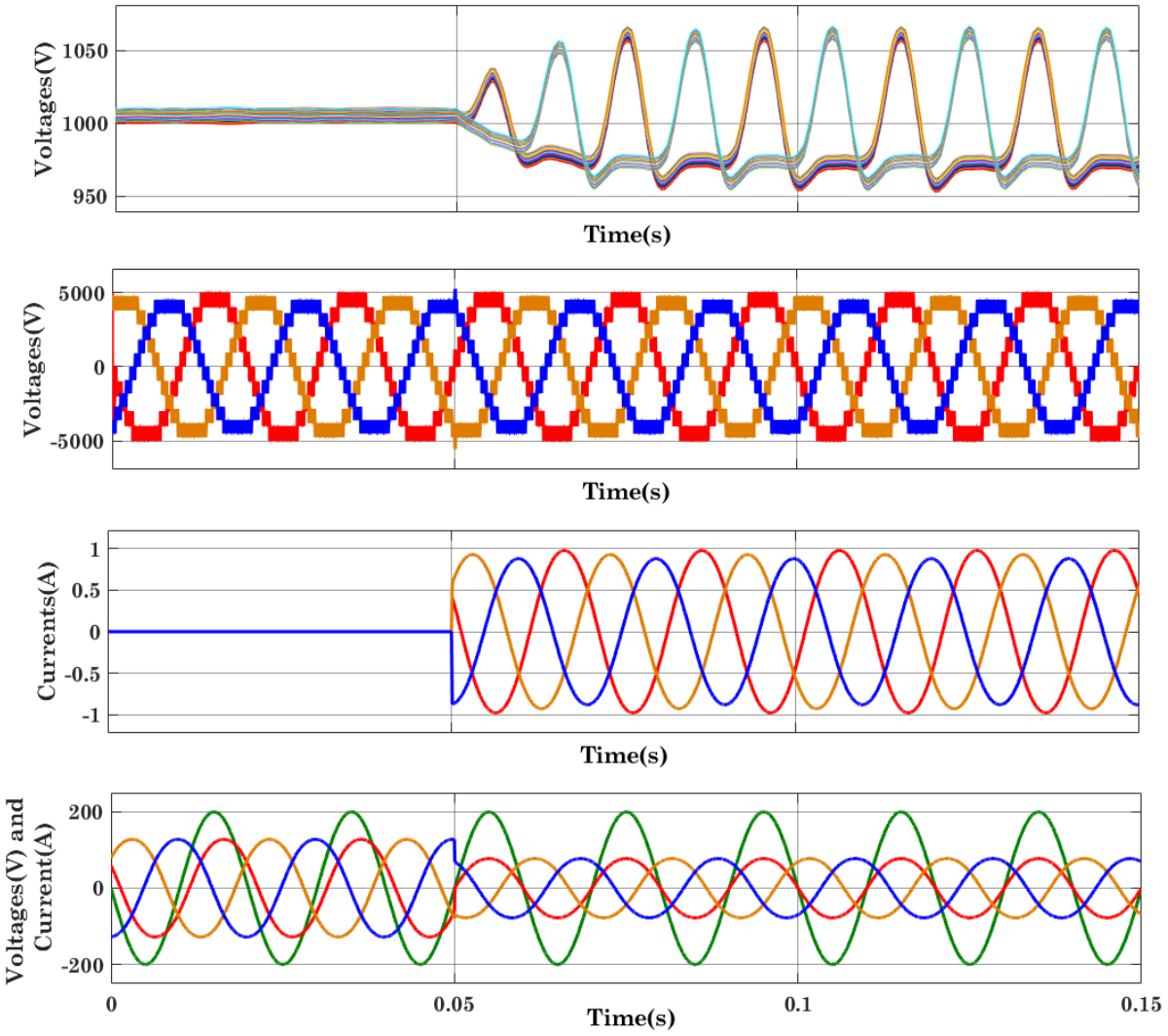

Fig 10. DC capacitor voltages of sub modules, STATCOM voltage, STATCOM currents and source voltage and current for unbalanced load

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
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Case 2. Unbalanced Linear Load

The study evaluated the performance of an MMC STATCOM in a real-world scenario. An unbalanced RL load was connected to the power source, and the STATCOM was integrated into the network at the Point of Common Coupling (PCC). The STATCOM's activation for positive sequence and negative reactive power compensation began at 0.05 seconds, with a 10kV DC link voltage serving as the reference for the DC side. Before 0.05 seconds, the primary focus of the STATCOM was on regulating the DC voltage, maintaining the DC voltages across the capacitors of the sub-modules at an almost constant level of 1kV, as shown in Figure 10a. Once the reactive power compensation was activated after 0.05 seconds, the phase difference between the source voltage and the source current was significantly reduced. This reduction demonstrated the STATCOM's ability to achieve unity power factor operation, as illustrated in Figure 10d. Consequently, the MMC STATCOM effectively supplied the necessary reactive power to meet the demands of the RL load. Figures 10b and 10c provided insight into the voltage and current profiles of the MMC STATCOM during its operation. The results highlighted the STATCOM's efficiency in voltage regulation, reactive power compensation, and attainment of unity power factor operation. These factors play a vital role in enhancing power quality and system stability. The study's findings showcased the proficient performance of the MMC STATCOM in adapting to load variations and maintaining a balanced and efficient power flow within the network. Such outcomes demonstrate the practical applicability and benefits of utilizing the MMC STATCOM in real-world power systems. The evaluation offered valuable insights that can contribute to optimizing and implementing STATCOM technologies in modern power infrastructures.

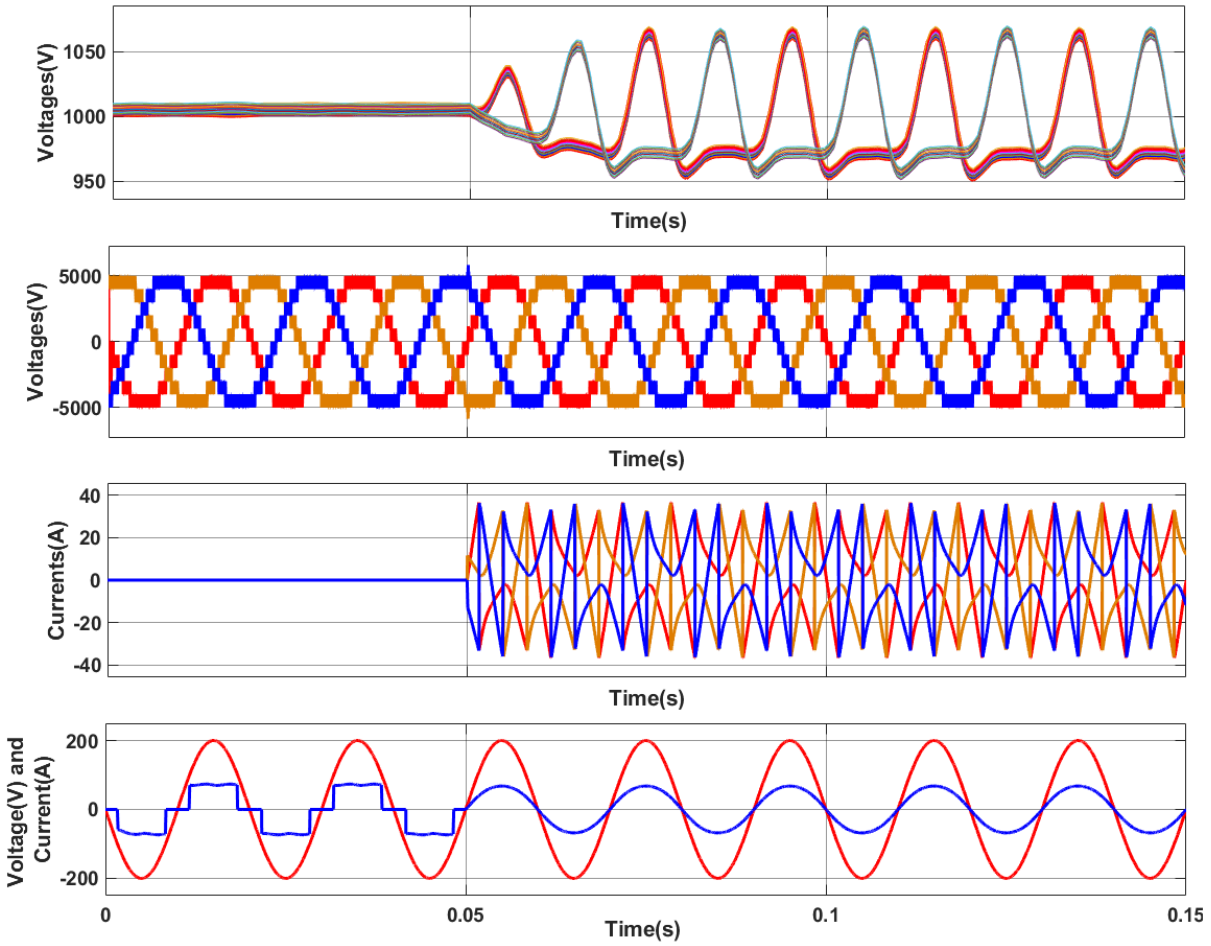

Fig 11. DC capacitor voltages of sub modules, STATCOM voltage, STATCOM currents and source voltage and current for Nonlinear load

International Journal on Recent and Innovation Trends in Computing and Communication
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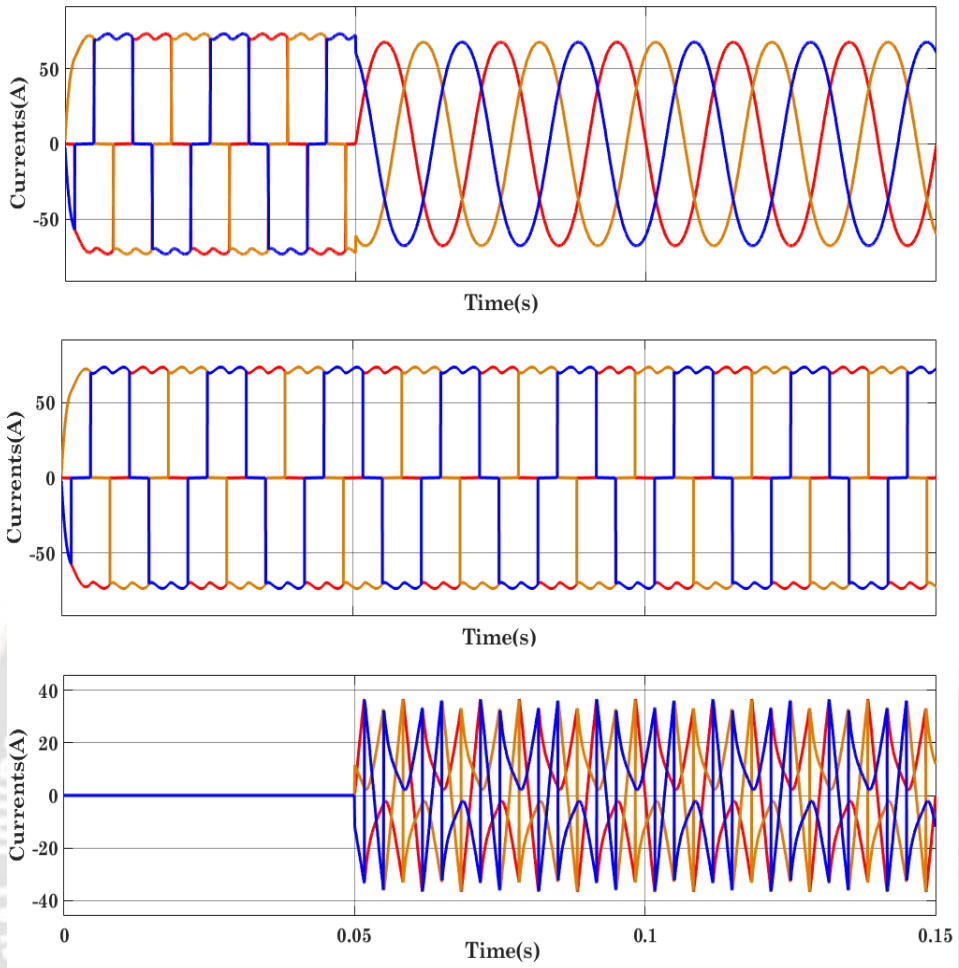

Fig 12. Source current, Load current and STATCOM current for nonlinear load

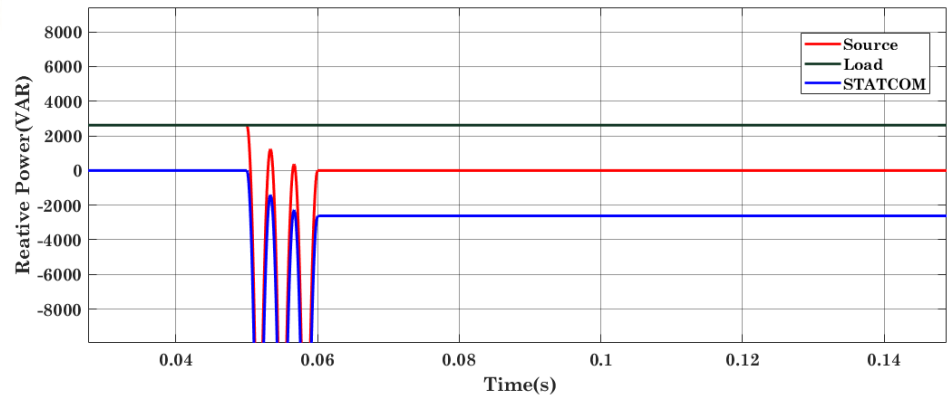

Fig 13. Reactive power compensation with STATCOM with Non-linear Load

Case 3. Non-linear Load

In this study, the performance of the MMC STATCOM was assessed under the influence of a nonlinear load connected to the consumer side. At 0.05 seconds, the STATCOM's reactive power compensation was activated. Figure 12b illustrates the load current, which exhibits a total harmonic distortion (THD) of 32.5% due to the nonlinear load. On the other hand, Figure 12a represents the source current before compensation. After the activation of compensation at 0.05 seconds, the STATCOM injected currents that helped reduce the harmonics in the source currents, leading to a significant improvement. As depicted in Figure 12a, the THD of the source current was successfully reduced to 2.5%. In Figure 12c, the STATCOM current injected into the Point of

Common Coupling (PCC) is shown. This injected current effectively compensates for the harmonic components, contributing to the overall mitigation of harmonic distortions in the system. Figure 13 presents the reactive power profiles at the source, load, and STATCOM. Once the compensation was activated, the source's reactive power was notably reduced. This reduction was a result of the STATCOM injecting the required reactive current to meet the demands of the nonlinear load, thus alleviating the burden on the source. The study's results demonstrate the effectiveness of the MMC STATCOM in mitigating harmonic distortions caused by nonlinear loads. By injecting appropriate currents, the STATCOM successfully improves power quality and reduces the THD levels in the source current. Additionally, the STATCOM's ability to compensate for reactive power ensures stable and efficient operation of the power system under nonlinear load conditions. These findings provide valuable insights into the practical application and benefits of using MMC STATCOM for enhancing power quality in real-world scenarios, particularly when nonlinear loads are prevalent in the consumer side of the power system.

V. Conclusion

In this paper the performance of an MMC-based STATCOM was thoroughly investigated under various scenarios. The primary objective was to assess the effectiveness of the proposed novel DC capacitor voltage balancing strategy in achieving reactive power compensation and voltage improvement in power systems. The study examined the STATCOM's response to different operating conditions, including connecting balanced and unbalanced RL loads, as well as nonlinear loads on the consumer side. The simulation results were obtained using MATLAB-Simulink software, and the STATCOM's performance was compared with conventional control strategies, including PI control. In the case of balanced RL loads, the proposed DC capacitor voltage balancing strategy effectively regulated the DC voltages across the sub-modules, leading to stable and consistent performance. Furthermore, when reactive power compensation was activated, the STATCOM showcased unity power factor operation and effectively supplied the required reactive power to the load, thereby enhancing power quality and system stability. Under the presence of unbalanced RL loads, the STATCOM demonstrated its capability to dynamically respond to load variations, maintaining a balanced and efficient power flow. The reduction in harmonics achieved through injected currents by the STATCOM significantly improved the power quality, reducing total harmonic distortion in the source current. Notably, when confronted with nonlinear loads on the consumer side, the MMC STATCOM showcased remarkable performance in mitigating harmonic distortions. By injecting appropriate currents, the STATCOM effectively compensated for reactive power, alleviating the burden on the source and ensuring stable operation under nonlinear load conditions. The novel DC capacitor voltage balancing strategy proved to be highly effective in addressing reactive power compensation and voltage improvement in a variety of challenging scenarios. Its ability to achieve unity power factor operation, regulate DC voltages, and mitigate harmonic distortions demonstrated its proficiency in enhancing power quality and system efficiency. The findings of this study provide valuable insights into the practical applicability of MMC-based STATCOMs for power systems. The proposed novel DC capacitor voltage balancing strategy exhibits promising potential for real-world implementations, offering a robust and efficient solution for reactive power compensation and voltage regulation. Overall, this research contributes significantly to the advancement of power electronics and its application in modern power infrastructures, benefiting both utilities and consumers alike.

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