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Design of Cost Efficient Noise Tolerant Digital VLSI Circuits based on Probabilistic methods

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***Abstract*—**Noise in digital logic circuits does not reduce with the scaling down of CMOS devices. The conventional CMOS design does not provide noise immunity when the circuits are operated in the sub threshold region. In order to enhance the performance of the circuit and to handle the errors caused due to noise that are random and dynamic in nature, a cost effective probabilistic based noise tolerant circuit design is proposed. The idea is based on master-slave Markov Random Field (MRF) mapping and master-slave MRF logic gate design. To illustrate this concept, simulations have been carried out for a simple NAND gate and later the same idea is implemented in an 8 bit Carry Look Ahead (CLA) Adder. This methodology trades hardware cost for circuit accuracy. The proposed technique offers better noise immunity and tolerance in comparison with the conventional CMOS design. Also, the power consumption is expected to be lesser with increased accuracy and reduced output degradation. Finally, the transistor count is expected to be reduced considerably in comparison with the direct MRF mapping technique.

***Keywords*—** *MRF technique, sub threshold region, probabilistic based,CLA, noise tolerant, master and slave.*

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I. INTRODUCTION

With the amelioration in the VLSI manufacturing technologies power dissipation per chip becomes a major design challenge for scientists and design engineers. There are many proposed ways to reduce the power consumption and one of the impacting methods is to reduce the supply voltage or operating voltage. In near future, the electronic devices are predicted to work at a much lesser operating voltage to make the product portable and it is very much useful in bio medical implants. Unfortunately, the noise in the system does not reduce proportionally as the supply voltage is decreased. When the circuits are operated in lower voltages, the leakage components play a major role and impact the circuit more than the dynamic components. Hence, a major challenge in low power circuit design is noise fluctuation. Ultra deep submicrometer VLSI circuits are hoped to work at lesser noise margin levels and thus, VLSI circuits are more vulnerable to fluctuations created by noise. Several fault tolerant designs were contemplated but majority of them are centered on particular types of noise such as crosstalk noise and substrate noise. The triple-majority-redundant methods are some of the most sought after solutions for device failure. On the failure of a circuit, the other two circuits correct the faults. These designs do not address the issues brought out by*random intrinsic noise* in ultra-deep submicrometer systems. The error correction code (ECC) techniques are predominantlyused to target errors in the data during transmission in communication systems. Nonetheless, we do not possess the prerequisite idea about thepotential types of errors thatmight occur inmicro level circuitry, and hence, it is arduous to select the apt error coding scheme. Moreover, ECC contributesbettererror amending capacities but the time consumed by the circuit is high.These techniques may not bethe optimal choice to eliminate intrinsic noise in VLSI circuits. As these noises arearbitrary and spontaneous, traditional logic design methods used in CMOS circuits are incompetent to crank these faults. This problem is tackled by probabilistic based design approaches. In probabilistic-based noise-tolerant approaches, the noise energy is distributed and averaged by the whole system; thereby drastically reducing the noise signal levels. The designed circuit is operated for input voltages lesser than the threshold voltage of the transistors for achieving low power operation and also the signal voltage levels are applied closer to threshold voltages to test the design.The immunity to noise of the system can be greatly improvised by the application of probabilistic approach.

Here, the probabilistic based circuit design is put forward based on *Markov random field theory*. The designprocedure flow is as follows: Under the probabilistic framework, the logic values in a circuit at a particular time cannot be precisely predictedto be correct. It is only expectedthat the probability distribution value have the highest possibility of being in a correct logic level. The probabilistic based circuits offer better noise immunity when compared to the CMOS counterparts. But, this is brought out at the rate of higher transistor counts. The hardware circuit overhead is higher in the MRF based design. Here, a cost efficientdesign is submitted to deliver a similar performance, with reduced hardware by Markov Random Field simplification. The methodology is based on master-slave MRF mapping and master-slave MRF logic design.The idea has been applied on a 2 input NAND gate, a 3 input NAND gate and an EXOR gate. Also, an 8bit Carry look ahead adder has been realized using the traditional CMOS design style. A significant percentage fall in the transistor count is observed.The highlighting tasks carried out in this research are:

1. ***Cost-effecientcircuit design in MRF style by master-slave grouping and logic design.***

As an alternative to directly map all the valid states, the truth table is categorized into two groups in accordance with the output logic states. Every state in the output that has logic “1”

are combined and placed ingroup *"1"* and the output states that have logic level "0" are grouped as group "0". The implementation of group 1 and group 0 minterms is done separately in master stylewhile the feedback network is designed in a slave style. By adopting this style of design the exponential increase in the hardware is controlled as the logic complexity increases.

2. *Decomposition of MRF network into smaller sub networks for logical realization.*

The complete MRF network is divided into many small-scale MRF subnetworks at the top level of abstraction (architecture) to overcome the circuitintricacy.The circuit is made immune to external noise using a valid min-term feedback convergence loop within individual subnetwork. Every feedback loop is designed by neighbourhood nodes in the same MRF subnetwork to actualize improved noise immunity.

II. PROBABILISTIC BASED DESIGN – AN ANALYSIS AND IMPLEMENTATION

The MRF is a concept that is predominantly applied in pattern identification and in communication systems. The prime idea of the MRF technique is that the output is influenced by their neighboring nodes. By joint estimation, the energy possessed by the noise signal is scattered and distributed among neighbour nodes. Thus, the signal level in the noise will be significantly reduced. Hence, the expected logic states are correctly predicted and the computing circuits are made more reliable.Therefore, a notable increase in reliability of the circuit is observed. The MRF technique gives phenomenal advantage in performance over other logic design styles since the operation is not necessarily dependent on indefectible devices or ideal signals. The MRF method is based on the Markovian property:The neighbouring nodes significantly influence the probability of the given variable. The variables are dependant only on its nodes near by the variable.

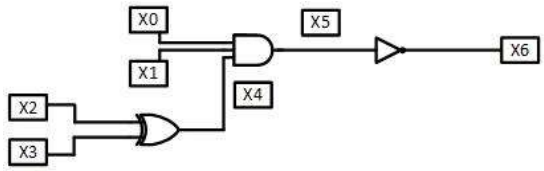

Fig. 1. Circuit for explanation of MRF technique

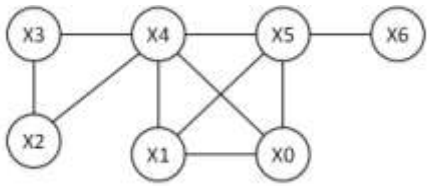

Fig. 2. Dependency graph for the circuit

From the example shown above, the MRF mapping method is explained. In MRF, a set of random variables is defined as follows Φ =(x0,x1,x2,x3,x4,x5,x6). The logic interactions between the nodes is P(x6) = P(x5|x6)P(x5). The connections represent the dependencies of the succeeding nodes on the predecessor node.

The figure below depictsthe design of a fault tolerant circuit through a valid minterm feedback loop. The probability of input nodes existing in the expected states are strengthened by collecting the min terms in a group and connecting back to the respective nodes.

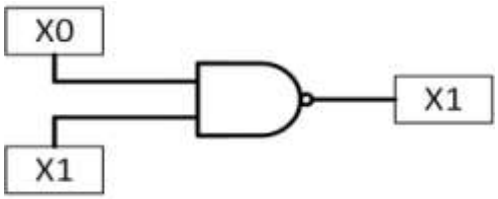

Fig.3 Conventional NAND Gate.

TABLE ILOGIC COMPATIBLITY OF A NAND GATE CONSIDERING ALL THE POSSIBLE STATES.

States	X0	X1	X2	Function
0	0	0	0	Invalid
1	0	0	1	Valid
2	0	1	0	Invalid
3	0	1	1	Valid
4	1	0	0	Invalid
5	1	0	1	Valid
6	1	1	0	Valid
7	1	1	1	Invalid

An illustration of the idea in a simple NAND gate is given below. The design objective is to ensure that the circuit stays in the correct states even in the presence of faults or noise . In the NAND example [x2x1'x0'], [x2x1x0'], [x2x1'x0] and [x2'x1x0] are four valid minterms {x2,x1,x0} = {100},{110},{101},{011}. The TABLE 1shows the compatibility in logic of a nand gate that describes all the probablelogic levels in which the gate can be present. The primary reason for achieving noise immunity is that the MarkovField network is updated repeatedly in many number of iterations corresponding to changes in states of the respective nodes. Finally, the defined logical network boils down to a correct and stable set of logic levels. The correct state energy is to be lesser than the energy of the incorrect state for fruitful operation.

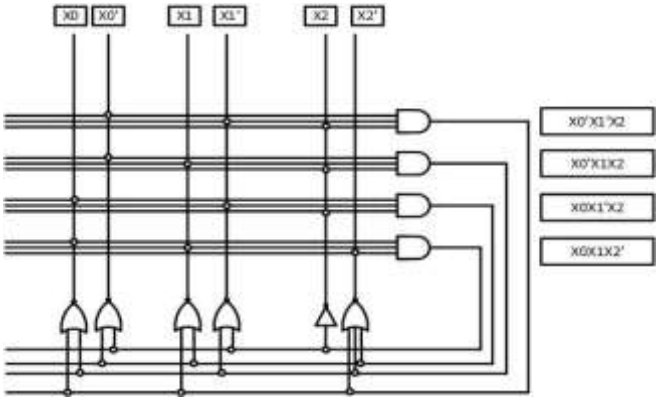

Fig. 5: Structure of a directly mapped MRF NAND Gate

The Fig.4. depicts the structure of a directly mapped MRF NAND gate that uses 4 3i-p AND gates and 6 NOR gates. The Fig.7. shows the modified cost efficient MRF NAND gate that

replicates the function of directly mapped MRF NAND gate with less hardware. Though the MRF circuits consume more number of transistors, it provides notable advantages over the conventional CMOS style when the supply voltage is reduced. The simulations were performed in cadence virtuoso® environment using the 180nm CMOS library. The threshold V_{TH} values of NMOS is 0.8V and that of PMOS is -0.8V.When operated at (gpdk)V_{DD} = 0.7V (V_{DD}<V_{TH}) i.e when the gate is operated at sub-threshold voltage, the output waveforms corresponding to that of CMOS NAND and the MRF NAND is shown.The noise added is Gaussian in nature and a maximum amplitude of 300mV is used.The constructed MRF circuit fails to function if the variation in the noise is large. The figures below show the differences in direct mapping and the cost effective mapping architectures. Itis found that local mapping reduces hardware overhead while retaining the same output.

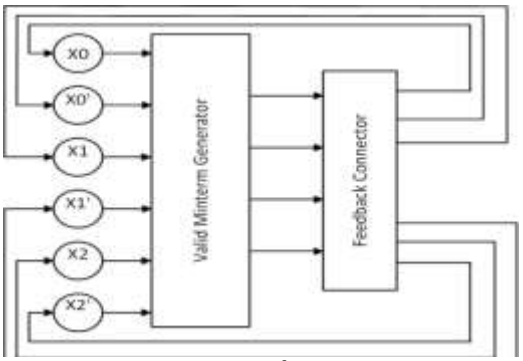

Fig.5: Mapping structure of a MRF NAND Gate.

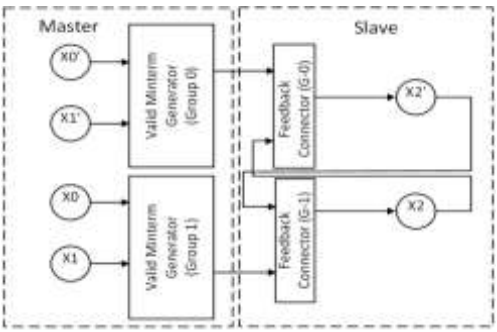

Fig.6: Structure of a cost effective hardware efficient MRF NAND Gate.

The difference between the two mapping architectures is that in the case of direct mapping technique, the valid states are collected together and mapped using AND gates in the min-term generator network and the outputs of the min term generator are generator are fed back to the inputs through a feedback connector that composes of NOR gates. In the case of cost effective mapping the truth table is bifurcated into two different group's *et al*group '1' and group '0'. The implementations of these groups are done in separately. The feedback network ensures that the input remain in the correct logic states even in the presence of single event upsets. The compatibility function of a NAND gate of 2 inputs is given under.

$$\boldsymbol{U(X0,X1,X2)} = X0'X1'X2 + X0'X1X2 + X0X1'X2 + X0X1X2'$$

Using the Boolean difference method the min terms have been reduced and the reduced expression is given below.

$$\boldsymbol{U(X0,X1,X2)} = (X0'+X1')X2 + (X0X1)X2'$$

Another major factor for moving towards MRF mapping techniques is that the operation of the circuit is never dependent on the quality of the input signal and the model of the device. The Fig.8 shows the simulation output when a conventional NAND gate is subjected to input voltages (0.4-0.7V) much lesser than the threshold voltage (0.8V) of the transistor.

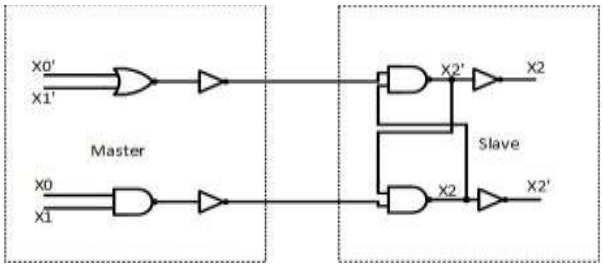

Fig 7. Circuit diagram of a hardware efficient MRF mapped 2 i/p NAND circuit.

The design of a 3 input NAND gate is done in three different styles namely the conventional CMOS style, the direct MRF mapped style and the modified hardware efficient style. The output of the CMOS style implementation in the presence of noise is not reliable, but the MRF style of implementation gives a better output. The problem with direct MRF mapping style is that the number of transistors *et al* the hardware overhead is high. To overcome this problem, the same logic is constructed using the hardware efficient circuit design using the Shanons expansion aka Boolean Reduction. For instance, a 3 input NAND gate when constructed using direct MRF mapped technique gives the following probability density function.

$$\boldsymbol{U(X0,X1,X2,X3)} = X0'X1'X2'X3 + X0'X1'X2X3X0'X1X2'X3 + X0'X1X2X3 + X0X1'X2'X3 X0X1'X2X3 + X0X1X2'X3 + X0X1X2X3'$$

Since the above given expression consumes a lot of gates and thereby increasing the hardware complexity and overhead the expression is reduced using Boolean reduction. After simplification the expression is obtained as follows.

$$\boldsymbol{U(X0, X1, X2,X3)} = (X0'+X1'+X2')X3 + (X0X1X2)X3'$$

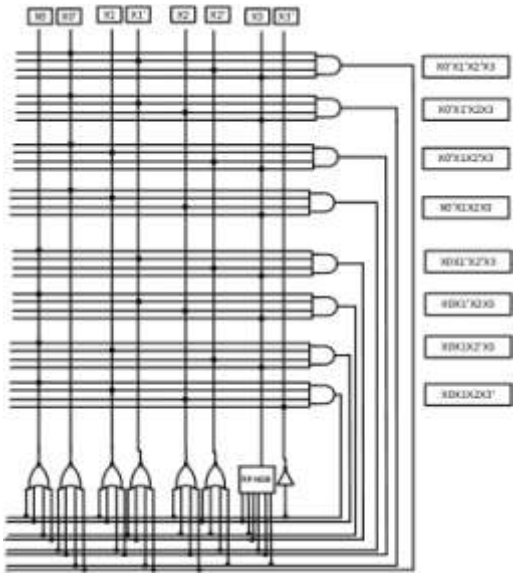

Fig.11. Structure of a directly mapped MRF 3 input NAND gate

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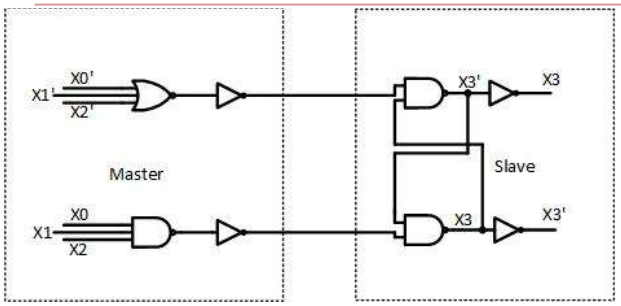

Fig.12. Structure of a cost effective hardware efficient MRF 3 input NAND gate.

An 8-bit Carry Look Ahead Adder is designed using the conventional CMOS style design and the circuit diagram is as follows. The waveform indicate the operation of the circuit at 1.8 V Vdd without noise. There is very less or no loss in data. The circuit is designed using basic blocks/gates like EXOR gate, AND gate, a Multiplexer etc. The Carry Look Ahead Adder consists of a product generator, a sum generator and a carry generator. Ultimately, this circuit is to be implemented using the MRF concept. It is believed that there will be notable change in the quality of the output in the MRF style circuit when both the circuits are subjected to the same level of noise. The signal propagates through several stages till the output levels converge to a state which is logically stable.

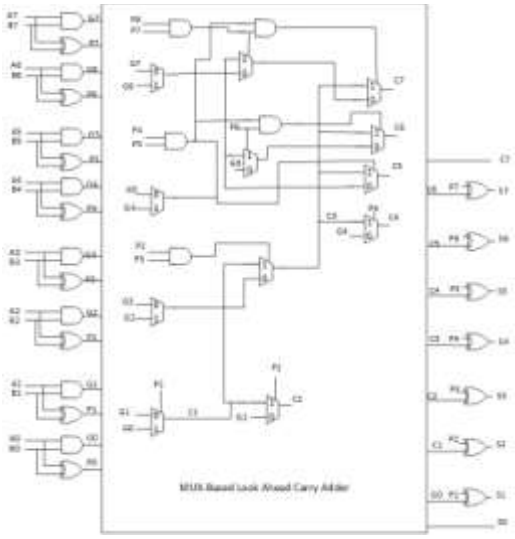

Fig.13. Structure of an 8 bit Carry Look Ahead Adder

III. RESULTS AND DISCUSSIONS

The conclusions have been made and are shown below.

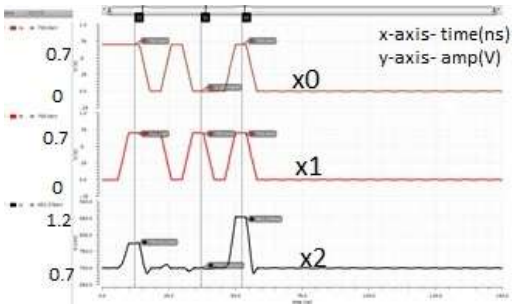

Fig.8 The output waveforms when operated at 0.7V Vdd and 0.7V Vin (Conventional CMOS Style).

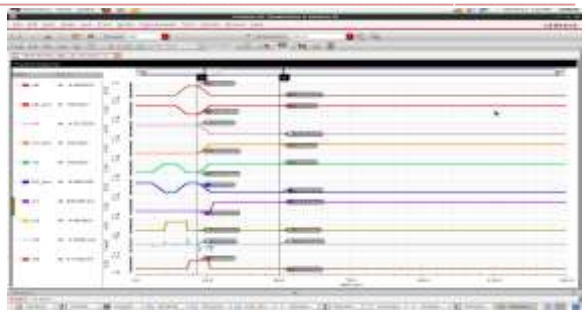

Fig.9 The output waveforms when operated at 0.7V Vdd and 0.7V Vin (MRF).

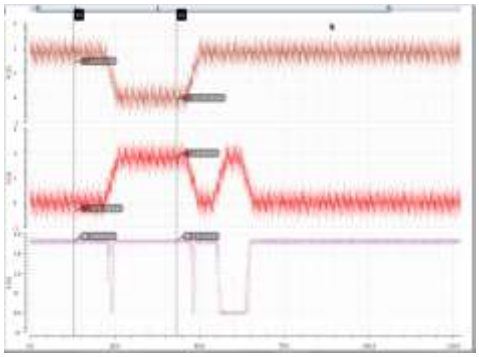

Fig.10. Output waveforms when noise is injected in the circuit [2 input CMOS-NAND]

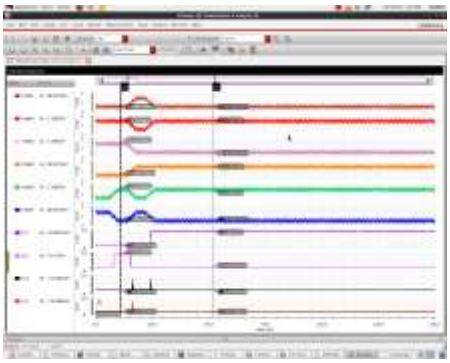

Fig.11. Output waveforms when noise is injected in the circuit [MRF-NAND]

The waveforms shown above give us the proof that the proposed circuit works efficiently in the presence of noise and when operated at input voltages near to V_{TH}. The transition from low to high logic values is found to be accurate. Hence, these kind of circuits can be used in defense applications. In Fig.8 it is observed that the logic 1 and logic 0 levels are disturbed to a large extent when the conventional CMOS NANDcircuit is subjected to 0.7V V_{dd} and 0.7VV_{th}. The logic 0 is at 0.7V and the logic 1 is at 1.2V. This is not the expected performance. In the Fig.9 when the same input conditions are applied to the MRF style circuit we obtain good quality output and the output is found to be at a stable state. Similarly, in figures Fig.10 and Fig.11. We observe that the output waveforms of both the CMOS and the MRF circuits. In the MRF style a stable noise free output logic level is observed whereas in the CMOS style of logic design the noise is reflected at the output which is undesirable. It is to be noted that the circuit is operated at voltages near the Vth of the transistors for low power consumption.

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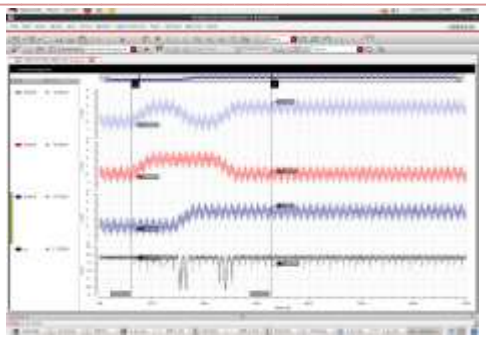

Fig.12. Output waveforms when noise is injected in the circuit [3 input CMOS-NAND]

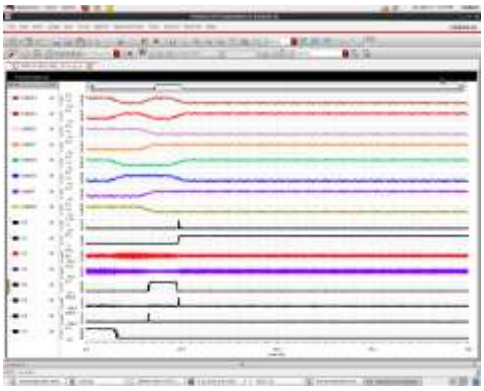

Fig.13. Output waveforms when noise is injected in the circuit [3 input MRF-NAND]

Similar characteristics in the output were observed when a 3 input NAND gate was designed in CMOS and in MRF style. The quality and the stability of the MRF circuits was better than the conventional style of design. Also, in the design of 2 input NAND gate the power consumed by the CMOS NAND gate was 709.7mW whereas in the case of MRF NAND the power consumed for y1 was 35.8 mW, for y2 was 35.69 mW, for y3 was 57.5 mW and for y4 was 35.75mW. The power consumed is observed to be less for circuits of less complexity. As the functionality in the circuit becomes more complicated, the power is significantly found to increase since the signal has to pass through various levels of gates or blocks. The number of transistors used in a 3 input CMOS NAND gate is 6 but the MRF style consumes about 144 but the modified MRF logic style consumes only 36 transistors. The output waveform shown below is that of an 8 bit carry look ahead adder. The circuit is subjected to 1.8V Vdd and 1.8V Vin.

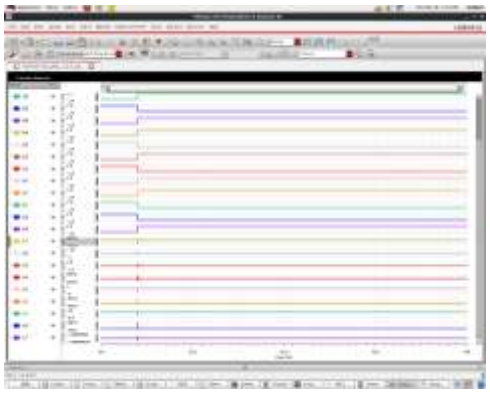

Fig.14. Output waveforms of an 8 bit Carry Look Ahead Adder

TABLE 2. COMPARISON OF VARIOUS PARAMETERS BETWEEN CMOS NAND AND MRF NAND DESIGNS

S. No.	Design	Conventional NAND	Direct MRF Mapped NAND
1.	Process	0.18um	0.18um
2.	Transistor Count	4	58
3.	Noise Tolerance [circuit is fed with a maximum noise of 300m]	Poor[fluctuations in 0 & 1 levels]	Good[no or very less deviation in logic levels
4.	Sub-Threshold Operation[Vdd=700mV]	0 level-700mV 1 level-853.37mV	0 level-4.712nV 1 level-677.98mV
5.	VDD_min[the voltage below which the circuit fails to operate properly]	0.9V	0.45V
6.	Power Consumed in the absence of noise at Vdd-1.8V	709.7mW	35.8mW for y1 35.69 for y2 57.5mW for y3 35.75mW for y4

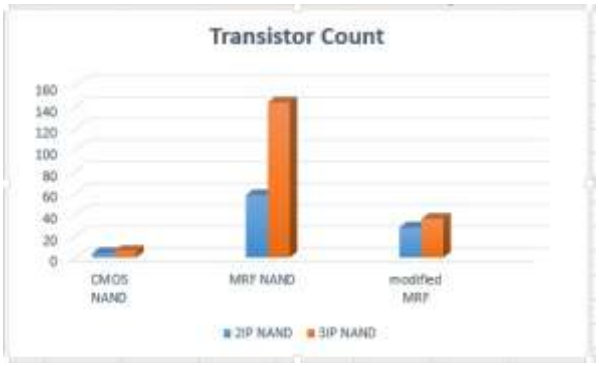

Fig.14. Chart depicting the hardware overhead.

Fig.15. Chart depicting the power consumption.

IV. CONCLUSIONS

1.It is never possible to get an invalid state even in the presence of noise in the MRF mapped technique.
2.The hardware overhead is high in direct MRF mappingtechnique.
3. We get a very good quality output in the MRF technique when operated in sub-threshold region and in the presence of noisy input.
4. It is made sure that the inputs remain in one stable state with the help of the feedback structure.
5. The hardware is considerably reduced in the cost effective MRF mappedcircuit as compared to the direct MRF mapping.
6. The power consumed is slightly higher when compared to the conventional CMOSstyle of circuit design in case of complex circuit design.
7. Since the number of transistors used is high the area is considerably high for both the techniques.

8. The speed of the proposed system is higher when compared with the CMOS style of circuit development.

It is noted that the newly designed circuit operates properly and produces the expected output only for a certain level of noise. The modified MRF circuit fails to function properly when the noise amplitude is of the order 0.9V or over and for the frequency above 10GHz.

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