Design of Low Voltage Process-Insensitive Self-Biased OTA With Rail-to-Rail Input Range

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***Abstract*—** The design of an Operational Transconductance Amplifier under the operation of sub-1 V supply is presented. So, that the all transistors are desired to operate in the sub-threshold region. Pseudo-differential pair with bulk-driven input stage is considered to allow the minimum supply voltage while achieving a rail-to-rail input range .A technique called self-biasing is involved to help the reduction of extra biasing circuitry and enhances the performance of the OTA. To enhance the bandwidth and allow the use of smaller compensation capacitors, a compensation network based on a damping-factor control circuit is exploited. Measurement results show that the OTA provides a low-frequency gain of 63 dB with the bandwidth of 2.3 kHz and rail-to-rail input common-mode range with a supply voltage as low as 0.75 V.

Keywords*—OTA, Bulk-driven, Self-biasing, Rail-to-Rail input range, Low voltage.*

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I. INTRODUCTION

The OTA is as similar to OP-AMP, especially OP-AMP without output buffer stage is considered as OTA. The OTA is voltage controlled current source device i.e., input is the voltage and output is the current. The ratio of output current to input difference voltage names the 'Transconductance'. OTA can drive all the load (capacitive as well as resistor) rather than OP-AMP. The OP-AMP is existence with complex circuit which will causes the larger power dissipation to maintain our gm's and there are so many vertical paths comparatively the OTA are low power almost on-chip so called amplifiers are OTA's. The output of the operational transconductance amplifier is the gm time's difference of the input voltage. In OTA the gm is directly proportional to the bias current , the advantage of this is if we choose the bias current we will change the transconductance which in turn inverse of the gm is none other than the resistance which decides the cutoff frequency of the active-filters. So, the OTA's are majorly used in the realization of active continuous (analog) filters. On silicon an active filter can satisfy both input and output relations by realizing the resistors by $1/g_m$ value.

In this paper, we present an OTA design that operates from a sub-1V power supply while achieving the rail-to-rail input range. The proposed OTA has used the self-biasing technique used to eliminate the effect of extra biasing circuitry. The input stage is pseudo-differential pair with CMFF and bulk-driven PMOS transistors to meet the requirement of the low voltage.

II. PSEUDO-DIFFERENTIAL PAIR INPUT STAGE

The minimum supply voltage for this architecture is the main challenge at the extent of minimum voltage (sub-1V) is capable to drive the whole circuit. The help of two complementary differential pair is utilized to make the input range from 0 to V_{DD} which is shown in fig.1. In turn the technique achieves the rail-to-rail input common mode range ICMR[9].

The supply voltage used in this architecture is expressed as $V_{DDmin}=V_{GSn}+V_{GSp}+2|V_{Dsat}|$, where is the V_{GSn} gate-to-source voltage of the input N(P)MOS transistor and V_{Dsat} is the saturation voltage of the biasing current source of each pseudo-differential pair shown in the fig.2.

Bulk-driven MOS transitor

A bulk-driven differential pair offers an alternative to gate driven input stage which is shown in fig.3. If the supply voltage of the circuit is less than a single p-n junction diode drop, a bulk-driven differential input stage can operate over the entire input range of the circuit without the risk of the forward biasing the diode[7]. The p-n junction is formed at the interface of the n-well and the source region of the PMOS transistor. Despite the low transconductance obtained from bulk-driven transistors, access to the bulk terminal is often available for, at least the PMOS transistors.

Similar to a conventional gate driven MOSFET, the gate source voltage of a bulk-driven transistor is fixed to a level slightly above the threshold level to create a conducting channel between the source and drain regions. However the, channel is modulated the by the ac input signal applied to the bulk terminal .Thus the minimum input voltage is not limited by the threshold voltage of the transistor. This technique circumvents the threshold voltage requirement, thereby extending the allowable operating range.

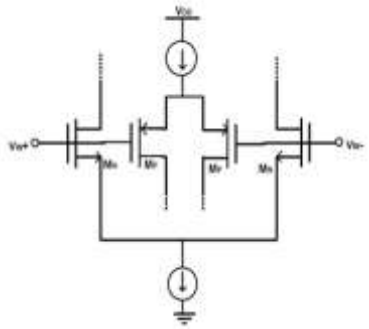

FIG. 1.Rail-to-Rail to input range using complementary differential-pairs

III. THREE-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFER

The fig. 4 shows the three-stage OTA without biasing and without the frequency compensation.

The first stage is the common differential pair which acts as the input stage of the OTA. The second stage is the common source with current mirror load. While the third stage is the common source with current source load. The OTA is designed using 180 nm technology; the supply voltage is 1.8 V. All the transistors are supposed to operate in saturation region to make the circuit as an amplifier [3]. The gain is achieved after the simulation of the circuit is 47 dB.

IV. THE PROPOSED SELF-BIASING BULK-DRIVEN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Fig. 5 shows the proposed self-biasing bulk-driven OTA. The minimum supply voltage is $V_{DD,min}=|V_{gs1}|+|V_{gs2}|$, thus all the transistors are operate in the sub-threshold region. In this technology threshold voltage of the both the NMOS and PMOS transistor is 0.35 V. From the fig. 4 we can notice that for biasing we use the three biasing schemes to input stage and the current mirror and common source stages . An alternative technique is used in the proposed OTA i.e., which does not require a biasing circuitry for generating these node voltages [1]. The first is from the output of CMMF circuit V_{oFF} to V_{b1}, the second is the V_{b1} and V_{b2},and the third from V_{out1} and V_{b3}.The proposed OTA uses the CMMF circuit of the first stage to bias the gates of the transistors $M_1$and M_2 and V_{out1} to bias the gate of the M_8 as indicated by the thick dashed lines in fig. 5. The proposed biasing circuit results the reduce in power consumption than the separate biasing V_{b3}[1].The proposed OTA uses the CMMF circuit of the first stage to bias the gates of the transistors $M_1$and M_2 and V_{out1} to bias the gate of the M_8 as indicated by the thick dashed lines in fig. 5.

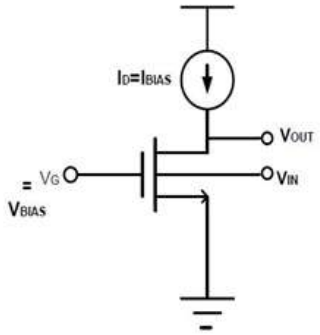

FIG. 2.Pseudo-differential pair with CMFF

The proposed biasing circuit results the reduce in power consumption than the separate biasing.

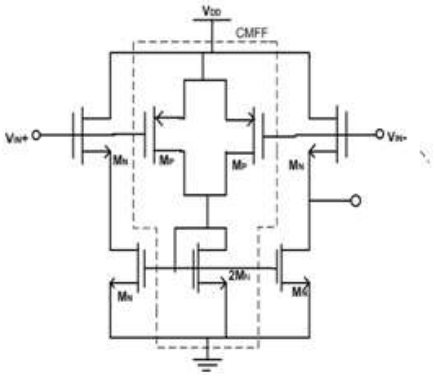

FIG. 3. Bulk-driven MOSFET

V. FREQUENCY COMPENSATION

The network for the frequency compensation is based on the Damping Factor Control scheme proposed in [4] which is shown in fig. 5. The network is established with the two nested miller capacitors and DFC stage G_{MC}.The second stage of the is OTA is non-inverting, while first and third stages are inverting. The third stage needs to be inverting loop for having the negative feedback in the inner loops. For that reason second stage of the OTA is loaded with current mirror and the third is

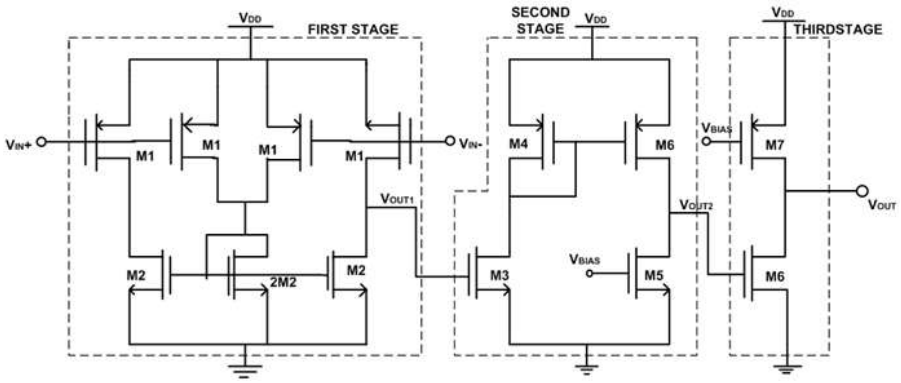

FIG. 4. Three-Stage OTA with separate biasing and without frequency compensation

loaded with the current source. The DFC compensation significantly enhances the bandwidth compared to conventional nested Miller technique and requires smaller compensation capacitors.

The compensation capacitors needed in conventional Miller are C_{C1}=20fF and C_{C2}= 2pF, as opposed to only 300 fF for both C_{C1} and C_{C2} using DFC compensation. This also improves the large-signal behavior of the OTA since for the same current smaller capacitance will be charged or discharged resulting in faster slew rate, i.e., SR=I/Cc. In addition, the need for large transconductance in the third stage (and hence large current) to drive large capacitive loads is obviated compared to conventional Miller compensation [18]. A stack-up of only two transistors can be used to implement the transconductance block which makes the DFC scheme applicable to low voltage applications.

VI. OTA DESIGN AND ANALYSIS

The full schematic of the proposed OTA with self-biasing and Frequency compensation is shown in Fig. 5. The DFC block is implemented using transistors and where the biasing of the gate of transistor is provided by the CMFF circuit. Therefore, the circuit is self-biased and the need for extra biasing circuitry is eliminated. The channel length of the transistors in the three amplifying stages is set to about 2.5 time's minimum length to provide sufficient intrinsic gain. The transistor widths are set to provide the current level required to achieve the desired specifications.

The differential-mode dc gain of the proposed OTA can be obtained from the equivalent small-signal model and is given by,

$$A_{DM} = \frac{v_{out}}{v_{in}} \simeq \frac{1}{2} g_{m_{b_1}} g_{m_3} g_{m_7} \left(r_{o_1} \| r_{o_2}\right) \left(r_{o_5} \| r_{o_6}\right) \left(r_{o_7} \| r_{o_8}\right).$$

The poles and zeros of the circuit can be obtained by further analyzing the small-signal model. Assuming that g_{mc1} (r_{oc1}‖ r_{oc2}) is greater than unity, C_{C1} = C_{C2},and parasitic capacitances are smaller than the load compensation capacitances.

If proper frequency compensation is applied to push the non-dominant poles to sufficiently high frequency, the unity-gain frequency of the proposed OTA can be approximated as,

$$f_T = \frac{g_{m_{b_1}}}{4\pi C_{C_1}}.$$

TABLE I

TRANSISTOR DIMENSIONS FOR VDD=0.75V

TRANSISTORS	W/L
M1	0.18µm/2µm
M2	0.18µm/2µm
M3	0.60µm/37µm
M4	0.20µm/37µm
M5	0.30µm/58µm
M6	0.20µm/37µm
M7	0.18µm/74µm
M8	0.18µm/2µm
MC1	0.18µm/2µm
MC2	0.18µm/2µm

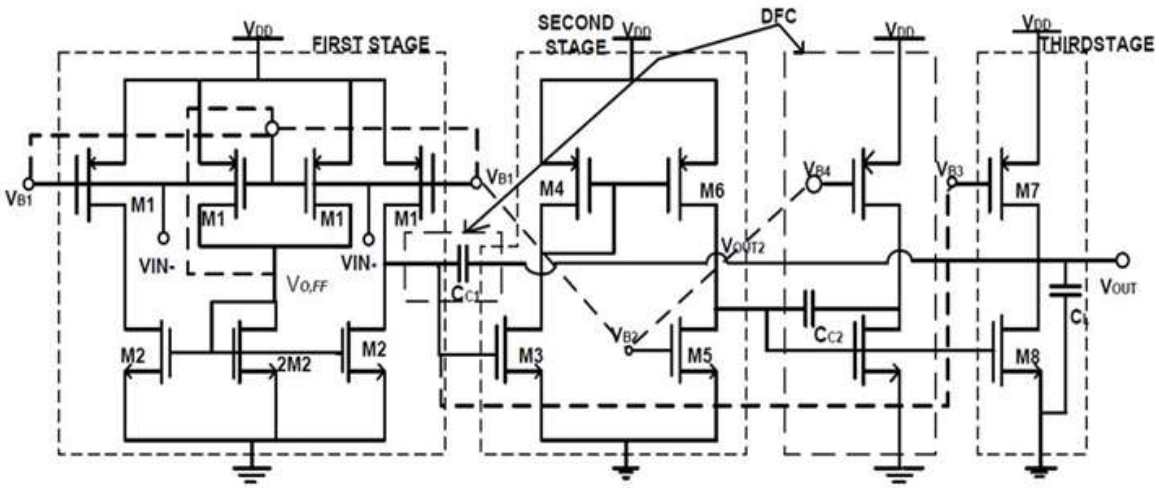

FIG. 5 OTA with self-biasing and frequency compensation

VII. SIMULATED RESULTS

The OTA was designed with for a nominal dc gain of 63 dB and a unity-gain frequency of 28 MHz operating of a 0.75 V supply. The transistor dimensions and operating conditions are listed in Table I. The compensation capacitors C_{C1} and C_C are equal 300fF. The OTA drives a 3pF load capacitance. The measured low-frequency gain is 63 dB in Fig. 6. The unity-gain frequency is 38 MHz, and the phase margin is 52˚ Fig.7.

Table II compares the performance of the OTA from simulations with the measured performance at V_{DD}=0.75 V

and at the different simulations results from the literature survey [8],[13].

TABLE II

COMPARISION OF OTA PERFORMANCE WITH PROPOSED OTA WITH RAIL-TO RAIL INPUT RANGE IN THE LITERATURE

	[13]	THIS WORK
Technology	CMOS 0.35µm	CMOS 0.18µm
Power supply	0.9 V	0.75 V
DC gain	70 dB	63 dB
Gain margin	11.4kHz	3MHz
C_L	15pF	1pF
Phase Margin	63˚	53˚

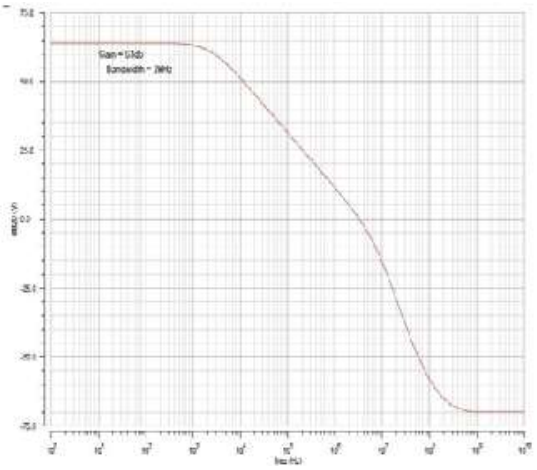

FIG .6. Bode plot

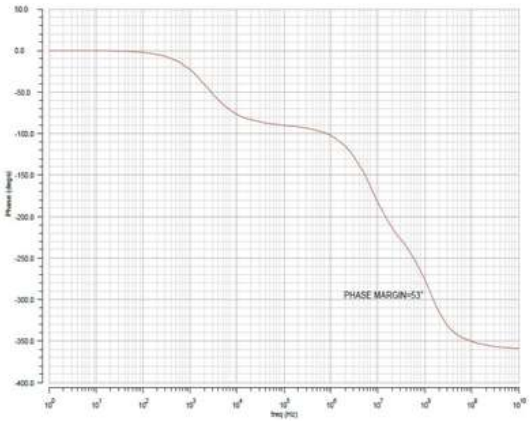

Fig. 7 Measured open-loop frequency response at V_{DD} =0.75 V

VIII. CONCLUSION

An OTA for low voltage operation is proposed to handle the challenges of the present low voltage CMOS technologies. The input stage is designed by pseudo-differential pairs with bulk-driven transistors which helps the low voltage operations. Also this benefits the rail-to-rail input common mode range. The self-biasing technique is used here that reduces the need of extra circuitry which causes low area and less power consumption.

The proposed OTA provides a DC gain of 63 dB at a supply voltage of 0.75 V with 2.3 KHz bandwidth and the phase margin of 52˚.

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