FPGA Implementation of MAC Unit Design by Using Vedic Multiplier

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***Abstract*—**Implementation of MAC unit is essential for any ALU or microprocessor based application specific integrated circuit.Thus implementing such a circuit with either high speed or low power is very essential for the proper operation of the MAC unit.The MAC unit implemented has slower speed due to inefficient implementation of the multiplier. Ancient Indian mathematics proposed a Vedic technique which allows us to implement the Vedic based multiplier on hardware. This multiplier is not only hardware friendly but also improves the speed of operation of the MAC unit. If a MAC unit is used N times in a microprocessor based system and we are able to speed up the multiplier by a factor of K then the overall speed improvement during the given time is NK. In the previous papers the MAC unit implemented has slower speed due to inefficient implementation of the multiplier .The Vedic multiplier is not only hardware friendly but also improves the speed of operation of the MAC unit. Instead of simple Vedic multiplier, in this paper we will be using a parallel or pipelined Vedic multiplier which will give faster outputs than the previous papers.

***Keywords*-*MAC, Vedic Multiplier, Vedic mathematics, high speed and low power, Urdhava Tiryakbhyam Sutra, pipeline*.**

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I. INTRODUCTION

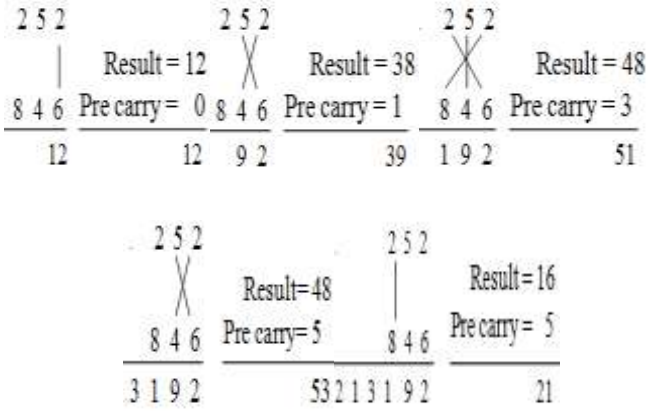
Recently, Multipliers are effective in many applications like as microprocessor, digital signal processing and most often used in critical arithmetic unit in many application such are Fourier transform discrete cosine transforms and digital filtering operations. The throughput of these applications mainly depends on multipliers. When the multiplier operations are too slow in the circuit then the performance of the entire circuits will be reduced. In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit one adder unit and both will get be combined by an accumulate unit. The main advantage of Multiply-Accumulate (MAC) unit are logic units digital signal processors and microprocessors, since it find the speed of the overall system. The efficient designs by MAC unit are Nonlinear Computation like FFT/IFFT, Discrete Cosine or wavelet Transform (DCT). Therefore it is basically use for multiplication and addition the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Basically the delay, mainly critical delay, created due to the long multiplication process and the propagation delay is found because of parallel adders in the addition step. The main aim of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

II. VEDIC MULTIPLIER

The Vedic mathematics applicable over complex calculation it reduces the typical calculation into a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

III. URDHAYA TIRYAKBHYAM SUTRA

The Vedic multiplier is depends on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and crosswise*". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.



252 × 846 = 213192

Fig 1. Multiplication of two decimal numbers –252 x 846

A. *32*32 bit Vedic Multi[plier:*

Using a 16×16 Vedic multiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig.2. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig

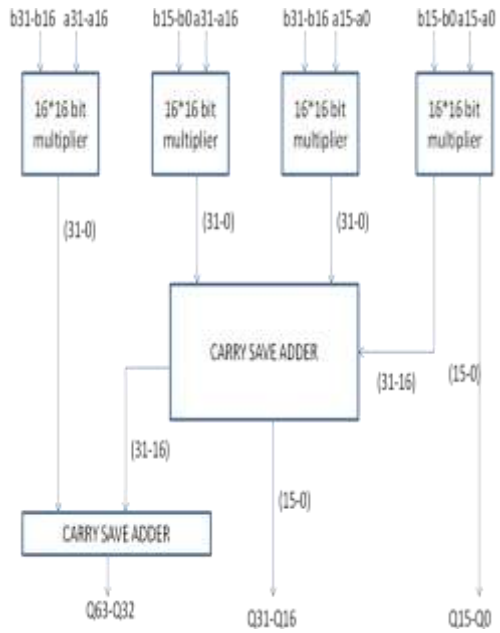


Fig 2. 32 × 32 Vedic Multiplier with Carry save Adder

IV. METHODOLOGY

A. *Implemented Architecture :*

For design of MAC architecture we required 3 sub design

1) Design of 64×64 bit Vedic multiplier.
2) Design of adder using DKG gate reversible logic.
3) Design of accumulator which integrates both multiplier and adder stages

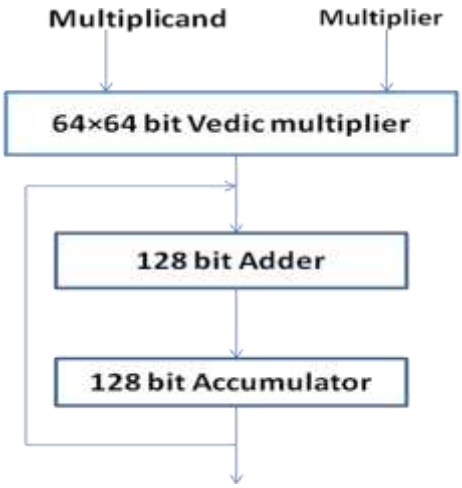


Fig 3. MAC Architecture

B. *64*64 bit Vedic Multiplier:*

Using a 64×64 Vedic multiplier we can design 128 ×128 Vedic multiplier with carry save adder as shown in fig.2. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig

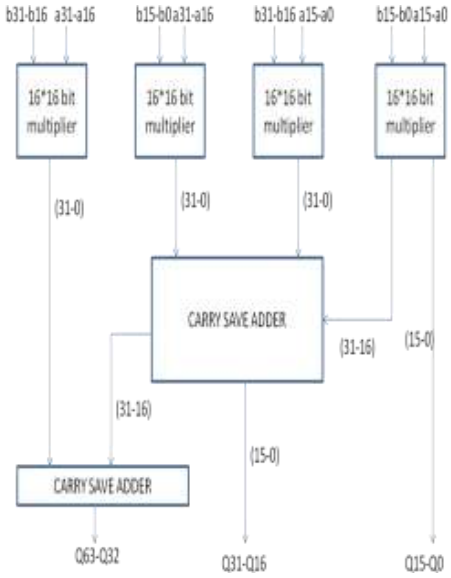


Fig 4. 32 × 32 Vedic Multiplier with Carry save Adder

C. *Reversible Logic :*

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

- **General Consideration For Reversible Logic Gate :**

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [13] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [15] showed

that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

- Fan-out is not permitted
- Loops or feedbacks are not permitted
- Garbage outputs must be Minimum
- Minimum delay
- Minimum quantum cost
- Zero energy dissipation

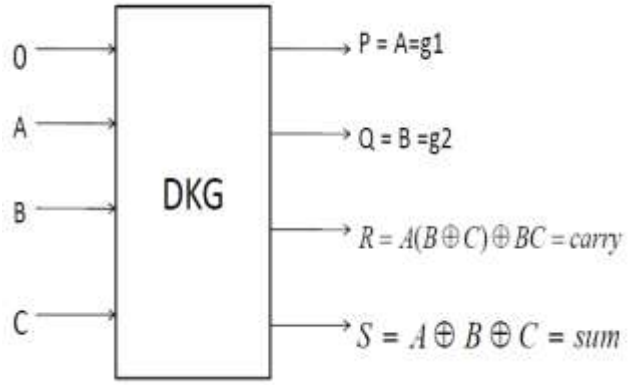


Fig 5. a) DKG gate as a Full adder

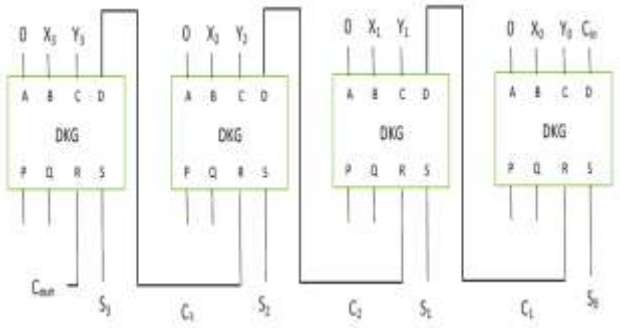


Fig 5. b) Parallel adder using DKG gate

D. Accumulator Stage:

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

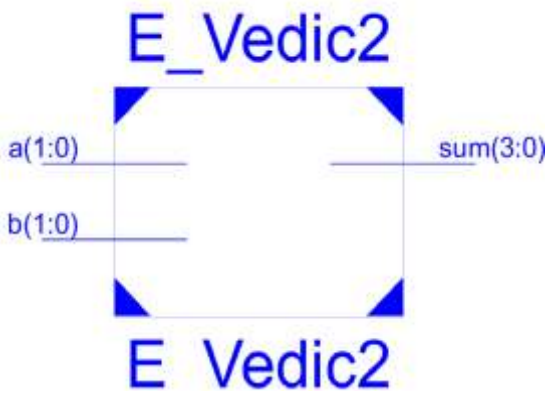
V. RESULT AND SIMULATIONS

A. Overview:

VHDL language is used as the hardware description language because of the flexibility to exchange among environments. The code is pure VHDL that could easily be implemented on other devices, without changing the design. The software used for this work is Xilinx ISE 13.1. This is used for writing, debugging and optimizing efforts, and also for fitting, simulating and checking the performance results using the simulation tools on same. All the results are based on simulations from the Xilinx ISE 13.1 using Timing Analyzer and Waveform Generator

B. Experimental Outcome:

The high performance multiplier with adaptive hold logic are properly designed using Xilinx 13.1 in VHDL. The Schematic and design are to be checked the output are showing in each clock cycle and different parameters calculated are given below in table I. Register transfer level, RTL view



Register transfer view of 2 bit MAC is shown below fig.5.1.

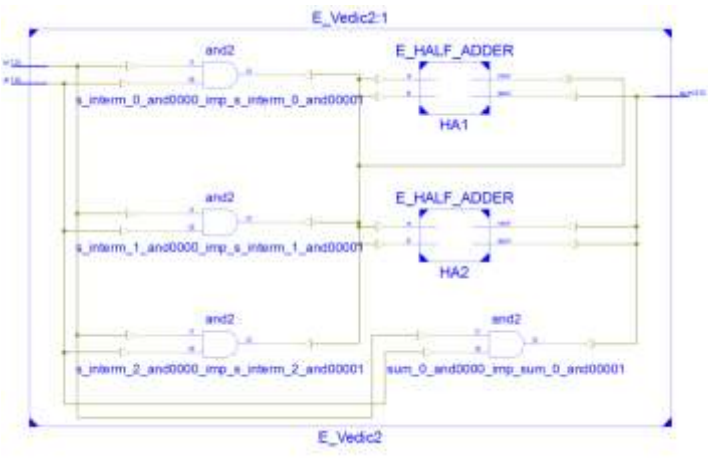


Fig.5.1 Register transfer view of 2 bit proposed architecture.

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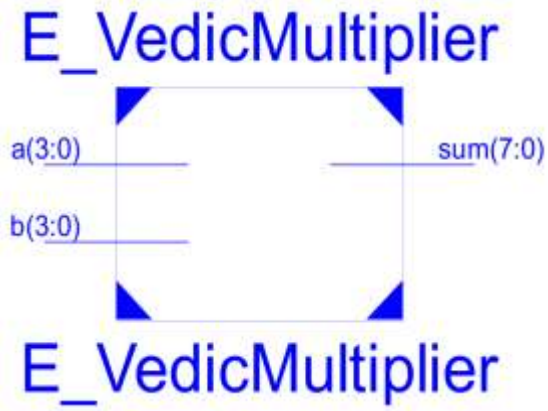


Register transfer view of 4 bit MAC is shown below fig.5.2.

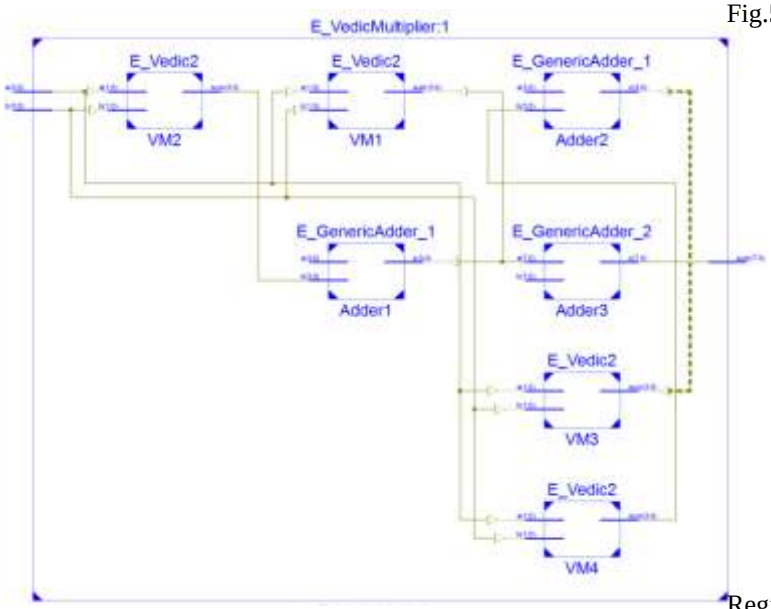
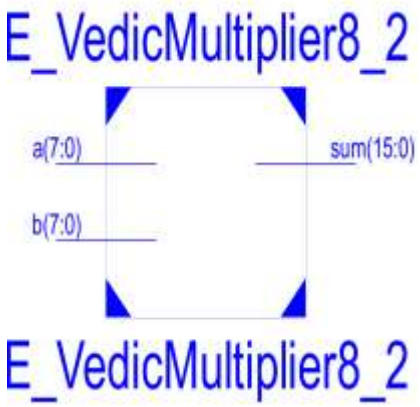


Fig.5.2.Register transfer view of 4 bit proposed architecture.



Register transfer view of 8 bit MAC is shown below fig.5.3.

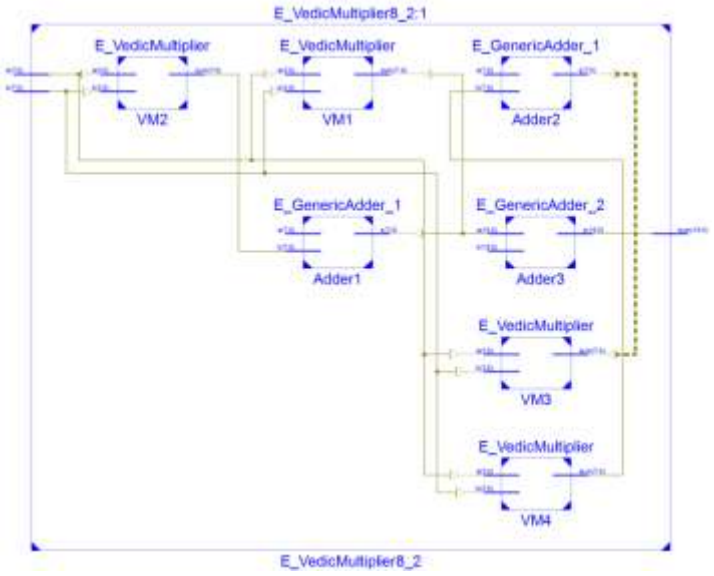
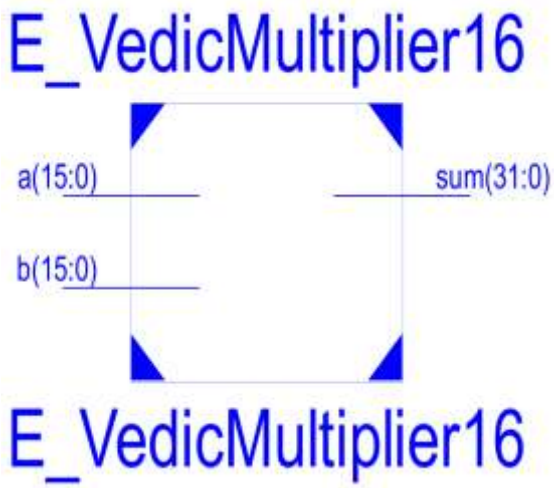


Fig.5.3. Register transfer view of 8 bits proposed architecture



Register transfer view of 16 bit MAC is shown below fig.5.4.

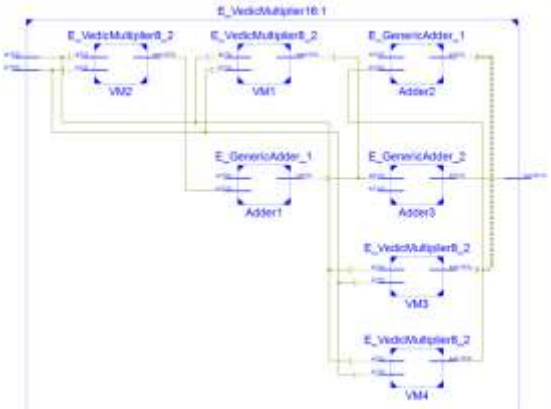


Fig.5.4. Register transfer view of 16 bits proposed architecture

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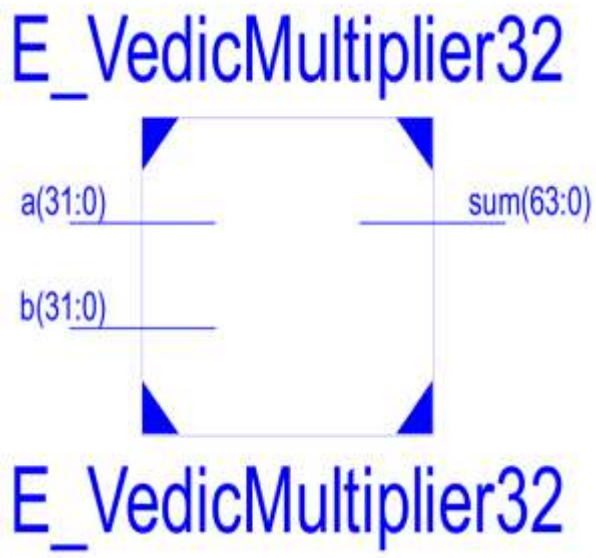


Register transfer view of 32 bit multiplier with is shown below fig.5.5.

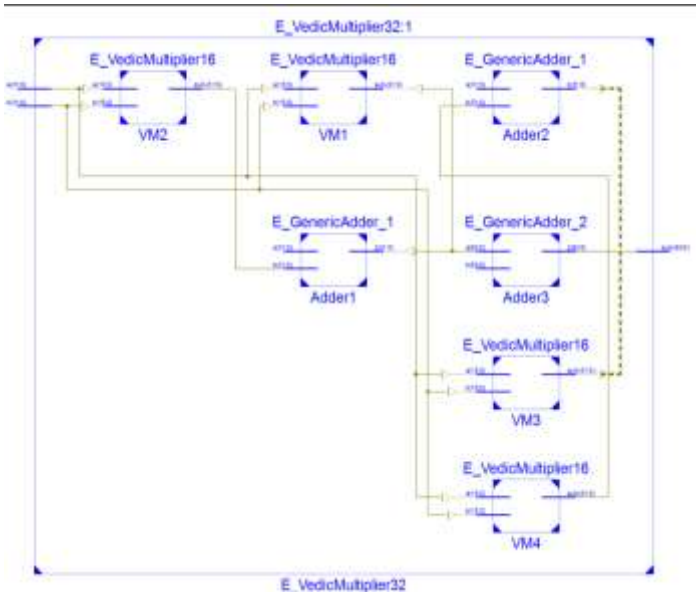
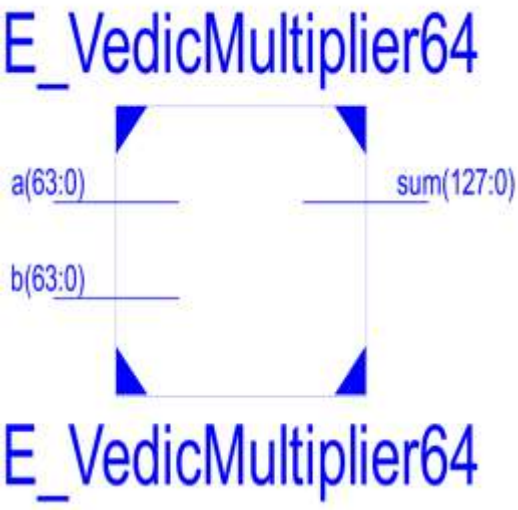


Fig.5.5. Register transfer view of 32 bits proposed architecture



Register transfer view of 64 bit multiplier with is shown below fig.5.6.

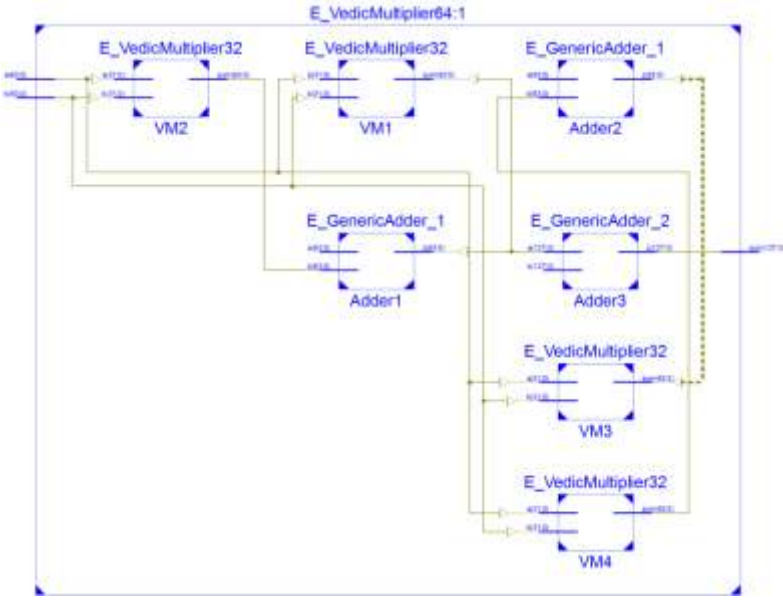


Fig.5.6. Register transfer view of 64 bits proposed architecture

C. Schematic Waveform Of MAC :

This paper includes the Simulation results of all the blocks that are designed. The simulation results of 64*64 bit multiplier.

Following figures shows the Schematic waveform of 32 bits multiplier. The input a and b and output is MAC_output, reset and clk.

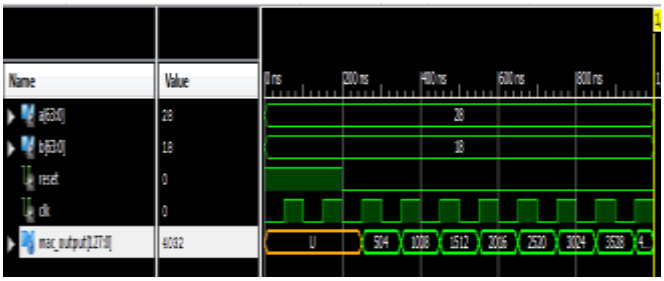


Fig. 5.7 Schematic waveform of 64 bits MAC architecture.

a =28, b = 18 MAC_output =504

D. Design Utilization Summary:

The proposed multiplier shown below using Xilinx 13.4 Family Spartan 3 and targeted devices *xc3s50-5pq208,* the result is shown 2-bit,4-bit,8-bit,16-bit ,32-bit and 64-bit multiplier.

MAC	Delay(ns)
2-bit	**7.34**
4-bit	**10.45**
8-bit	**18.78**
16-bit	**28.47**
32-bit	**38.90**
64-bit	**46.67**

Table 1. Delay result of MAC

VI. CONCLUSIONS

The results obtained by the design of Vedic multiplier with 128 bits and reversible logic are quite good. The work presented is based on 128 bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 128-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity as compared to other architectures. Many researchers are reconfiguring the structure of MAC unit, which is the basic block in different designs and aspects especially using reversible logic which evolves recent days. Spectrum Analysis and Correlation linear filtering which are the applications of transform algorithm further add to the field of communication, signal and image processing and instrumentation, and some other. Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well engineering.

In this thesis we implement high performance multiplier with reversible logic and compare speed, power and area, from this result it indicate that this architecture has useful over conventional multiplier and it increases the performance of circuit . The Urdhava Triyagbhayam and reversible logic is very useful over conventional multiplier in all expect like power, speed and area.

REFERENCES

[1] Vaijyanath Kunchigi ,Linganagouda Kulkarni, Subhash Kulkarni 32-bit MAC unit design using Vedic multiplier International Journal of Scientific and Research Publications, Volume3, Issue 2, February 2013

[2] Ramalatha, M. Dayalan, K. D. Dharani, P. Priya, and S. Deoborah, "High speed energy efficient ALU Design using Vedic multiplication techniques", IEEE Int. Conf. on Advances in Computational Tools for Engineering Applications (ACTEA-2009), pp. 600-603, July 15-17, 2009.

[3] Garima Rawat, Khyati Rathore, Siddharth Goyal, Shefali Kala and Poornima Mittal,"Design and Analysis of ALU: Vedic Mathematics Approach", International Conference on Computing, Communication and Automation (ICCCA2015), ISBN:978-1-4799-8890-7/15/©2015 IEEE.

[4] Pushpalata Verma, K. K., Mehta,"Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool", International Journal of Engineering and Advanced Technology (IJEAT) Vol. 1, Issue 5, ISSN: 2249-8958, June 2012.

[5] M.E.Paramasivam, Dr.R.S.Sabeenian, An Efficient Bit Reduction Binary Multiplication Algorithm using Vedic Methods, IEEE 2nd International Advance Computing Conference 2010.

[6] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics, Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, IIT Kharagpur.

[7] Ramalatha M, Thanushkodi K, Deena Dayalan K, Dharani P, A Novel Time and Energy Efficient Cubing Circuit using Vedic Mathematics for Finite Field Arithmetic, International Conference on Advances in Recent Technologies in Communication and Computing 2009.

[8] Anvesh Kumar, Ashish Raman, Dr. R.K. Sarin, Dr. Arun Khosla, Small area Reconfigurable FFT Design by Vedic Mathematics, 2010 IEEE.

[9] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho, Multiplier design based on ancient Indian Vedic Mathematics, International SoC Design Conference 2008.

[10] Sumita Vaidya and Deepak Dandekar, Delay-Power Performance comparison of Multipliers in VLSI Circuit Design, International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

[11] S.S.Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A Implementation of Vedic Multiplier For

Digital Signal Processing, International conference on VLSI communication & instrumentation (ICVCI) 2011.

[12] Asmita Haveliya, A Novel Design for High Speed Multiplier for Digital Signal Processing Applications (Ancient Indian Vedic mathematics approach), International Journal of Technology and Engineering System (IJTES), Vol.2, No.1, Jan-March, 2011.

[13] Prabha S., Kasliwal, B.P. Patil and D.K. Gautam, Performance Evaluation of Squaring Operation by Vedic Mathematics, IETE Journal of Research, vol.57, Issue 1, Jan-Feb 2011.

[14] Aniruddha Kanhe, Shishir Kumar Das and Ankit Kumar Singh, Design and Implementation of Low Power Multiplier Using Vedic Multiplication Technique, (IJCSC) International Journal of Computer Science and Communication Vol. 3, No. 1, January-June 2012, pp. 131-132 .